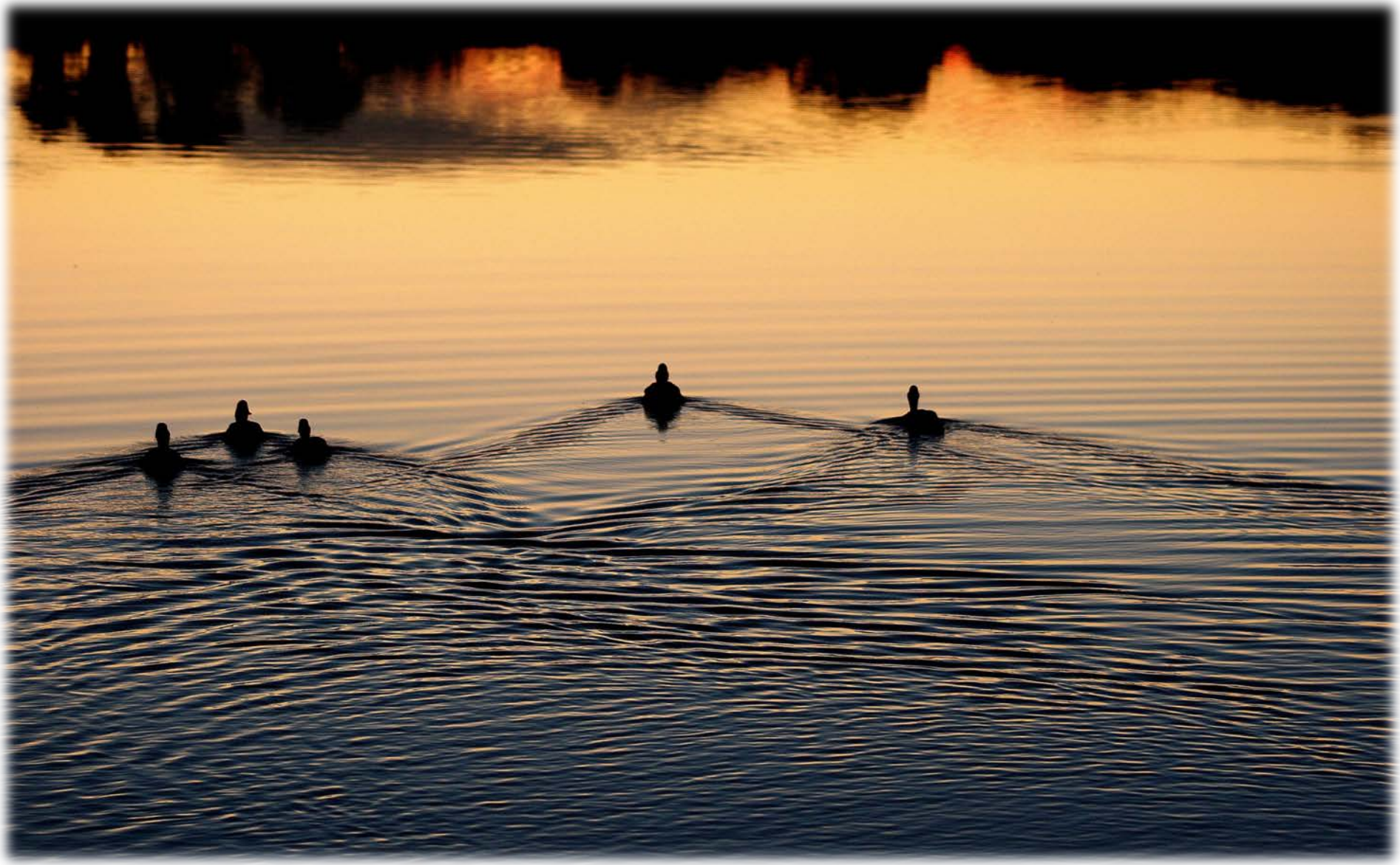
European Space Agency

High pin count packages. General update and tutorial

Liam Murphy – TEC-QTC

High pin count packages. General update and tutorial

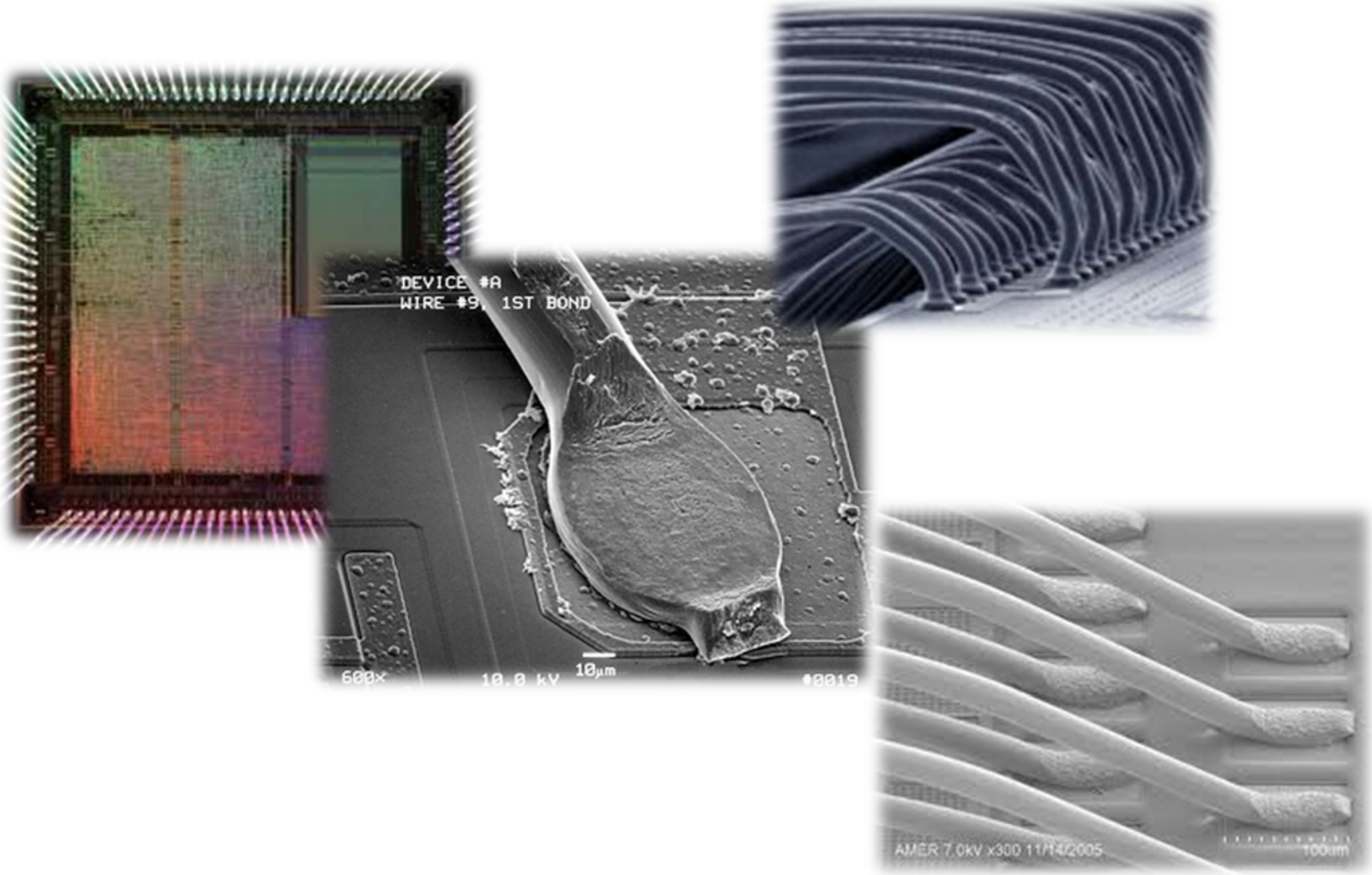
European Space Agency



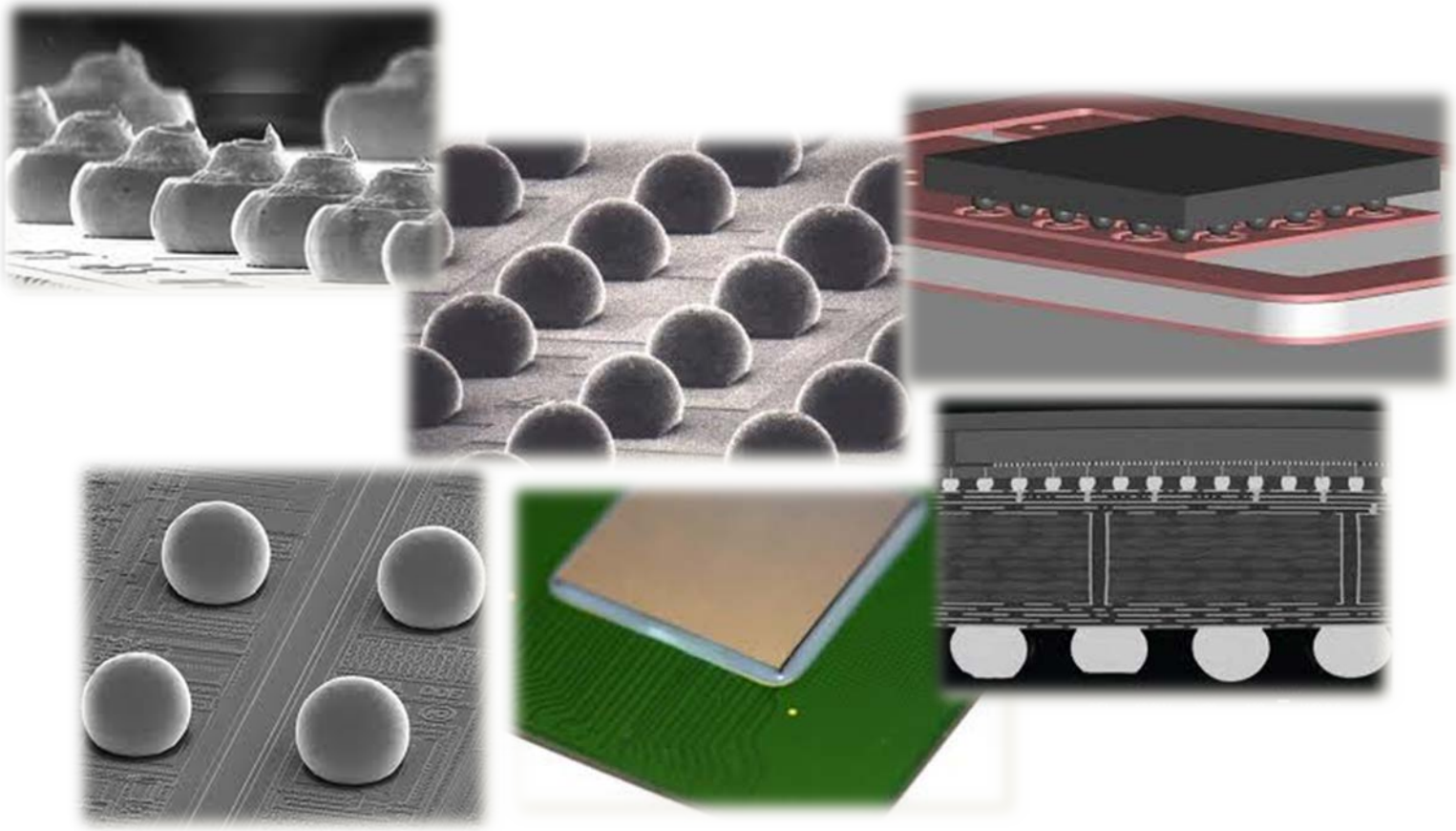
Risk of Going From This

To This!

In Technology terms….
From This…..



To This….



Could lead to this!

Then, The result could look like this!

Trends in Large Silicon Devices and Packaging

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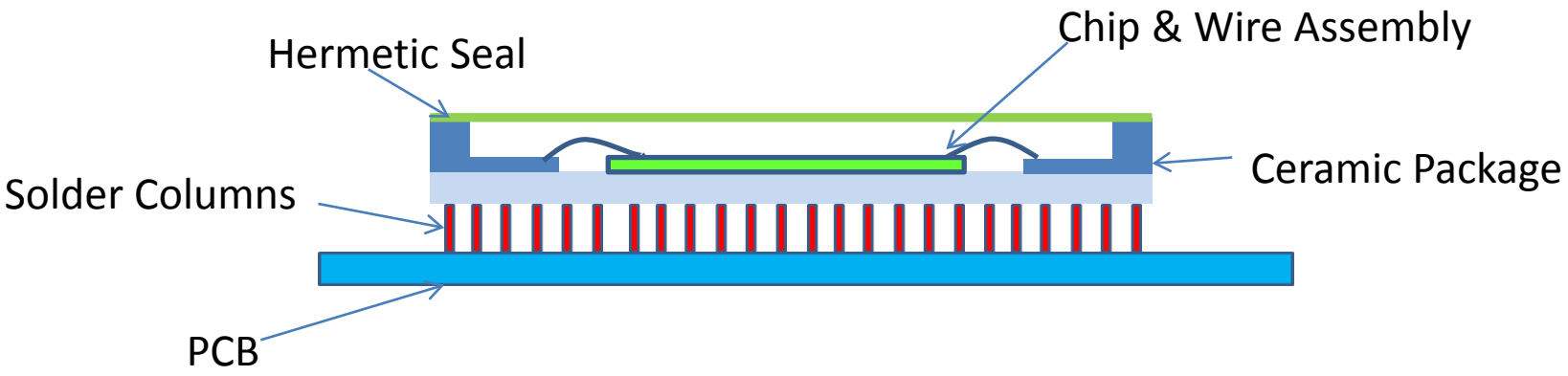
- Greater:
  - Gate count
  - Size
  - Speed (higher frequency)
  - Power & Dissipation
  - I/Os
- Less / Lower
  - Feature size
  - Cost?

Emerging Gaps with Current Packaging Solutions

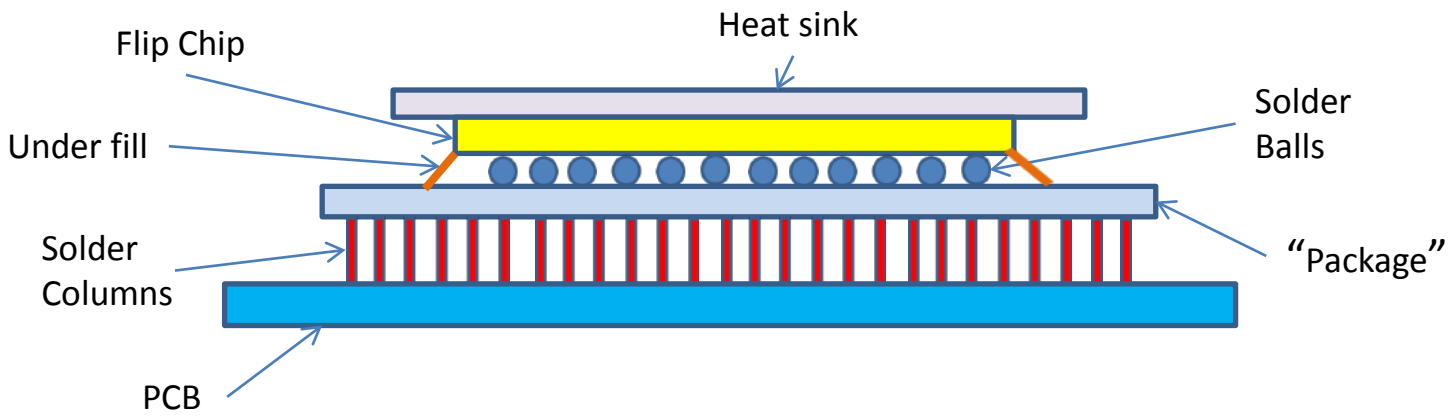
- Too many I/O for wire bond solutions
- High Power dissipation (more than PCB thermal plane solution can manage)
- Larger I/O (from Package) than current “qualified” capabilities

Current Packaging Solution



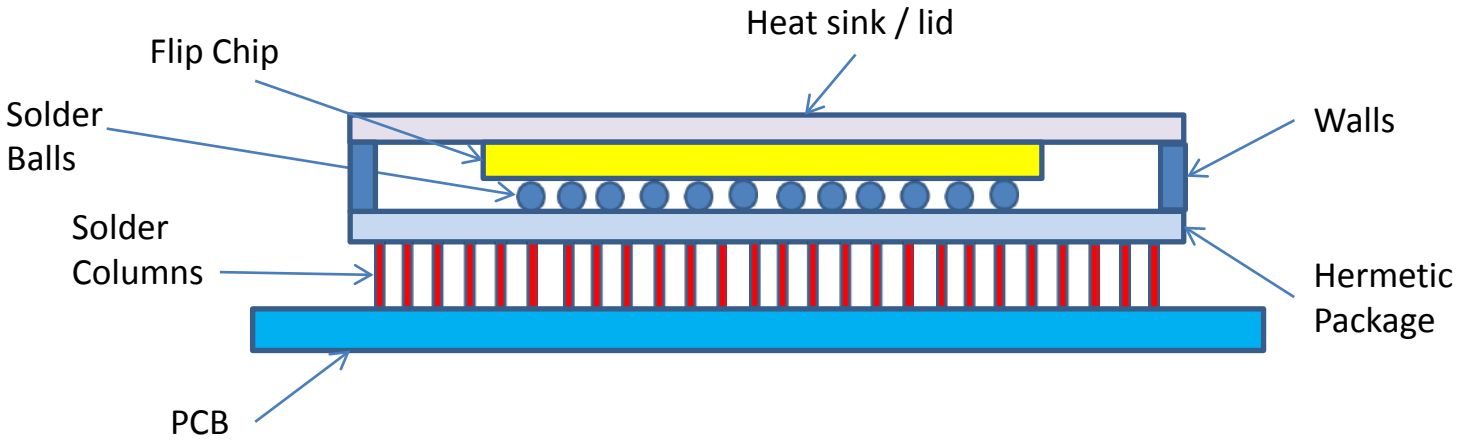
Hermetic Package – Ceramic
Wire bonded – single or staggered rows
Soldered / Column mounted

Emerging Technology Solution



Non- Hermetic Flip Chip Package

Or Maybe……



Hermetic Flip Chip Package

Hermetic or Non Hermetic – The Debate

Hermetic Benefits:

- Possibility to dissipate some heat into PCB
- No Need to use under fill
- Possibly more mechanically robust
- Possible to apply most current standards

Non Hermetic Benefits:

- Simpler thermal management
- Simpler PCB (lighter – reduced thermal planes)
- Possibly fewer / less critical mechanical tolerance issues
- Fewer manufacturing steps

Hermetic or Non Hermetic – The Debate

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Hermetic issues:

- Precision required on more materials/processes
- Too much thermal flux to control by conventional method
- Effects of lid attached to chip unknown

Non Hermetic issues

- More susceptible to mechanical damage
- No Heritage for flight use
- Few applicable standards
- New materials and test methods required?

Common Issues for Flip Chip for Flight – Hermetic or not

- Much larger area array than currently qualified
- Current PA /QA inspection and validation methods do not / can not apply
- Extremely high value components (€ or $)
- Many new materials, methods and processes
- Thermal dissipation challenges!

Qualification?

- Not Currently Qualified (Generic)

Class Y ? (Class Y is non-hermetic specifically)

It is coming! Current Status:

DLA-VA has completed the EP study. They have released the draft of MIL-PRF-38535 (Rev. K) with Class Y added.

– Short falls still apparent
  - Qualification & Screening tests maturing but still questions…
    – Eg DPA methods…..how to disassemble…solvent test….etc.
  - Sample size requirements may have cost implications
  - Process controls and validation methods, Pre cap etc. are slow to resolve….

ESA developments in the field

- Development of Flip Chip packaging Technology
  - Lead by E2V, complementing new high speed die development
- Packaging for highly dissipating dies on PCBs
  - Solderless mounting methods
- HDI, high speed PCB development
- Novel high efficiency thermal management methods
- High thermal conductivity packaging materials
- European Column attachment development

A note of Caution!

Despite extensive testing – problems still occur!

A note of Caution!

DH Comet – First Commercial Jet Airliner

Several “in flight” catastrophic failures.

All (at the time) tests and qualifications passed & repeated- passed again!

Brand new methods of investigation found and developed to uncover failure mode.

A note of Caution!

A note of Caution!

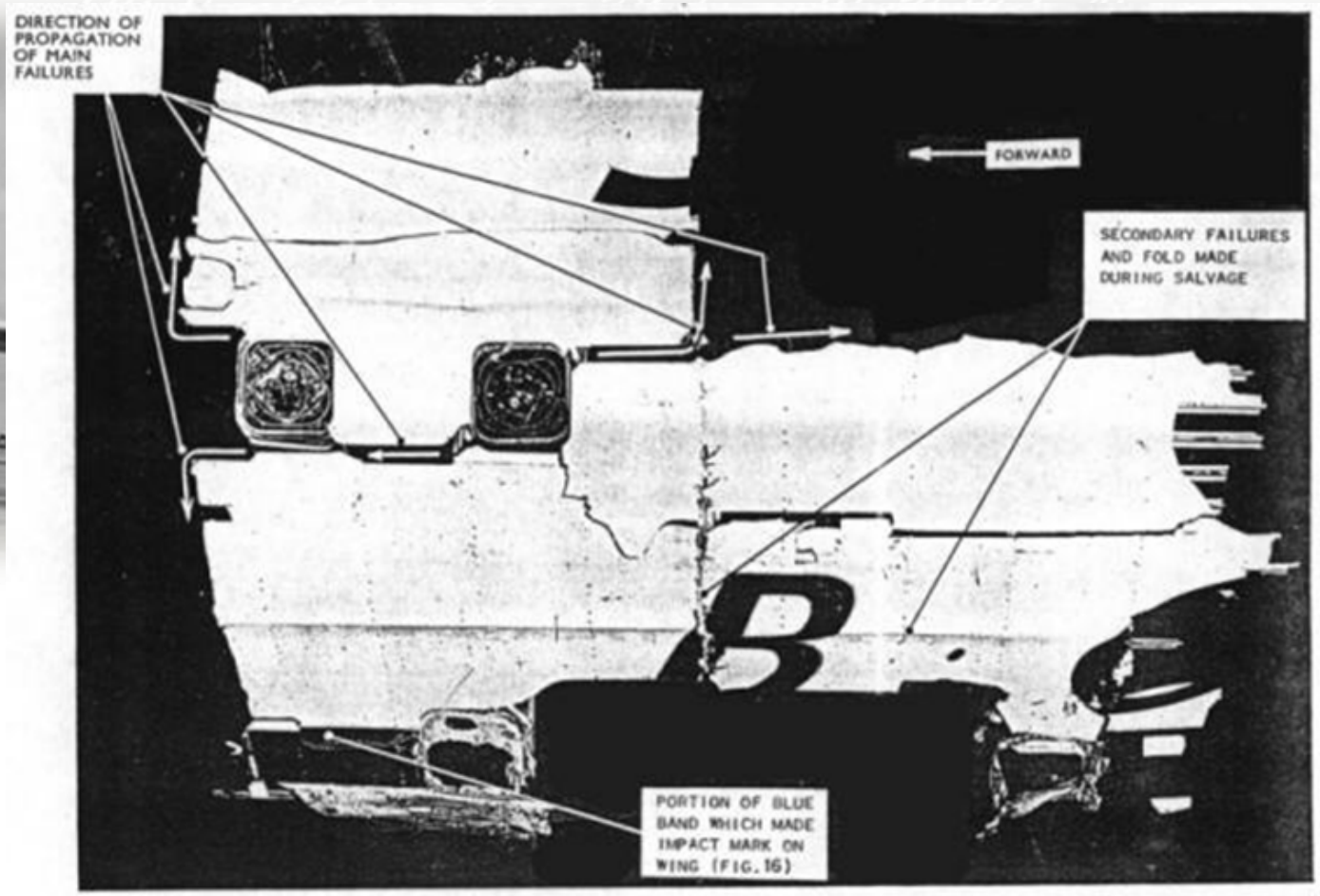

FIG. 12. PHOTOGRAPH OF WRECKAGE AROUND ADF AERIAL WINDOWS—G-ALYP.

In Summary 1

No stability or base line for flip chip established…..

- European solutions currently under development, but early days.
- Major FPGA Supplier (delivering non hermetic flip chip) keeps changing……
  - 2012, announced changes to heat spreader sizes…
  - 2013, announced changes to only supply LGA (no columns attached)
    - Also another change to heat spreader!
  - All project quals will now be invalid or at least require Delta

In Summary 2

- The Non-Hermetic potential is much greater than just the Flip chip products discussed herein……..
  - Encapsulated Memory Devices
  - Optronic devices
  - Sensors

- The scope for Flip Chip is much larger!
  - RF GaAs MIMIC
  - Other Silicon devices (not just large ASIC s or FPGA)
  - GaN Transistors?

In Summary 3

Customer desires for “more” are driving this disruptive requirement. Agencies & Industry are responding…..

- Many facets to be addressed
- Techniques and control methods still developing (more may be required).
- ESA concentration on developing European solutions for space market customers.
- Certification agencies are working to facilitate solutions into market place.

- The clock is ticking

Questions?

Thank you for your attention