# *ESTEC: European Space Components Conference (ESCCON)*

## BCD and discrete technologies for power management ICs development

Antonio Imbruglia
IMS R&D / Power & ICs Rad-Hard
IMS Space Coordinator

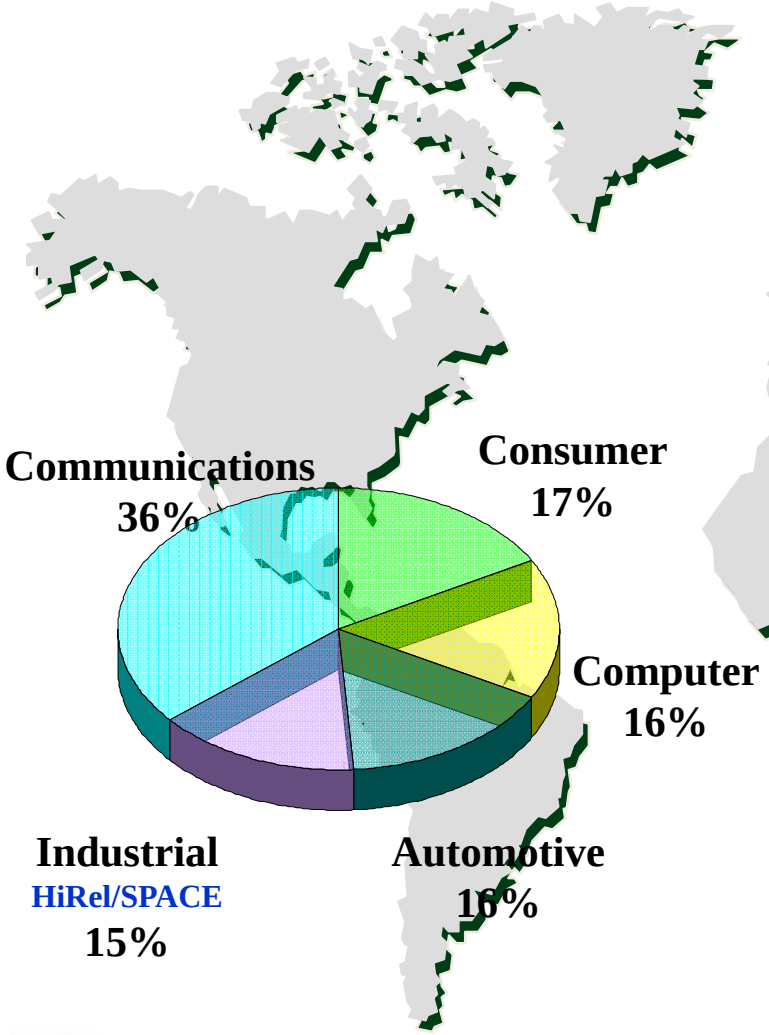
March 14,2013

life.augmented

# STMicroelectronics

oducts

## A Global Semiconductor Company




Approximately ~42,000 employees

15 main production sites

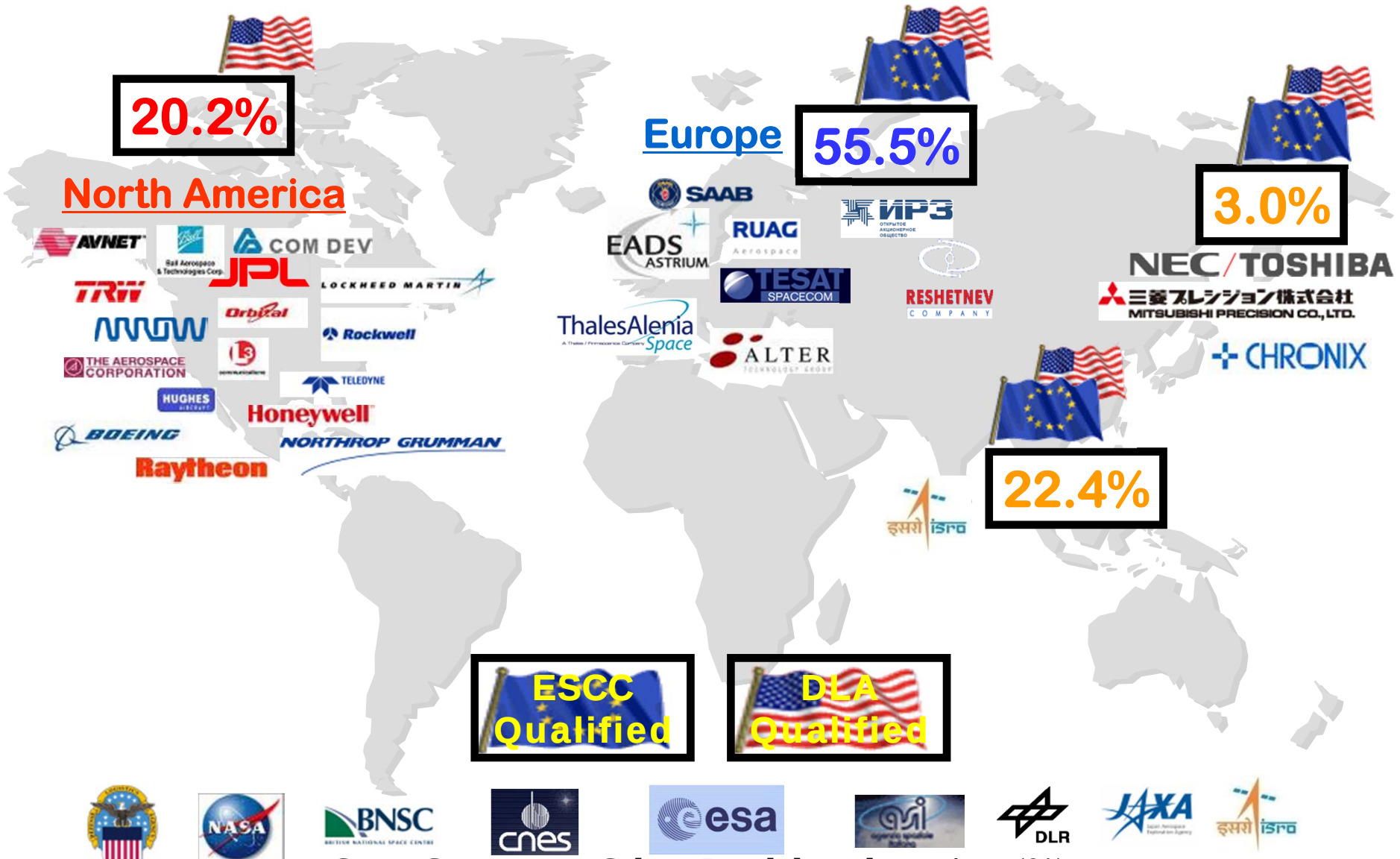
16 advanced R&D centers

39 design and application centers

78 direct sales offices in 36 countries

life.augmented

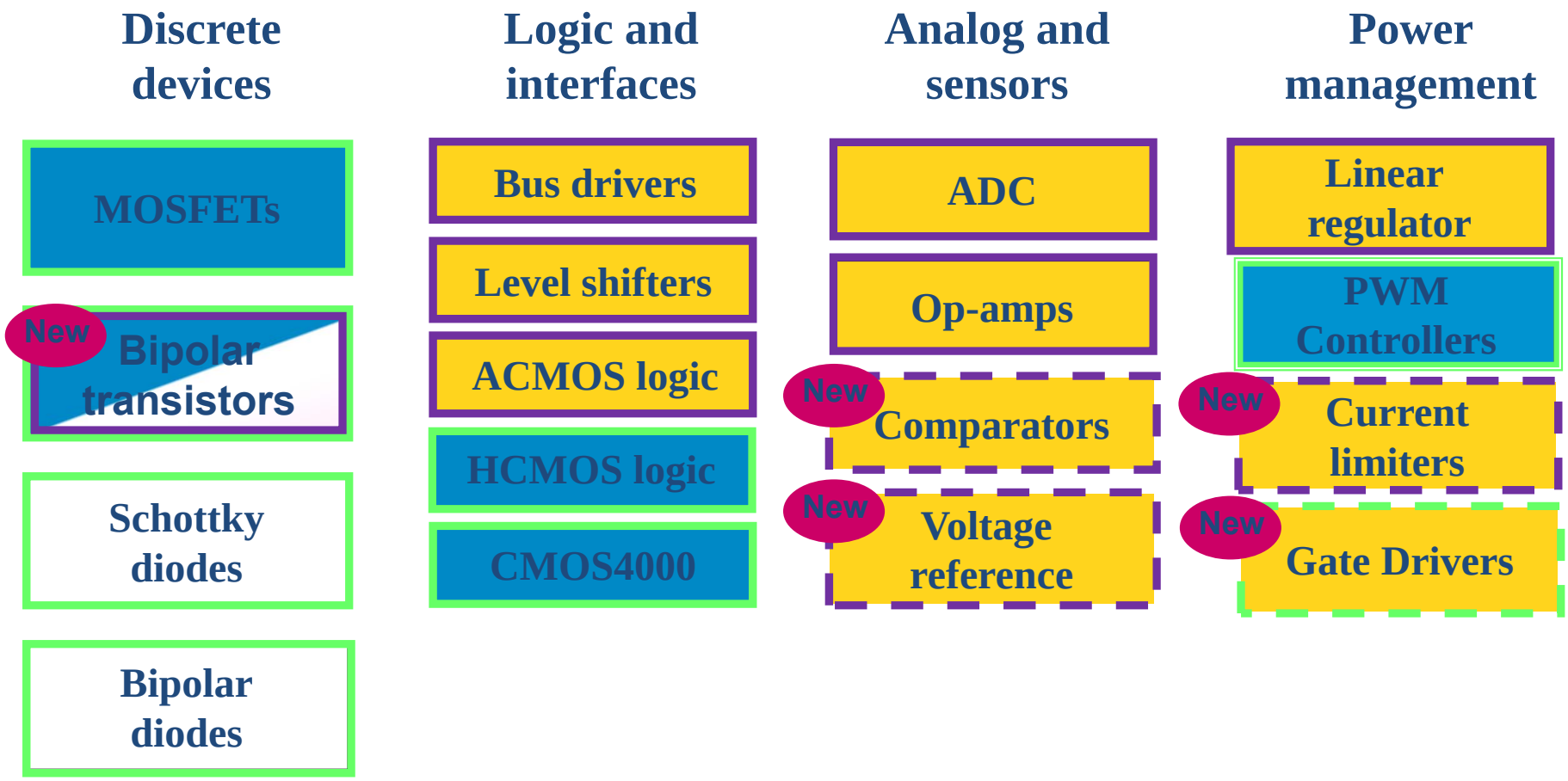
# ST Aerospace - 2012 Key Figures



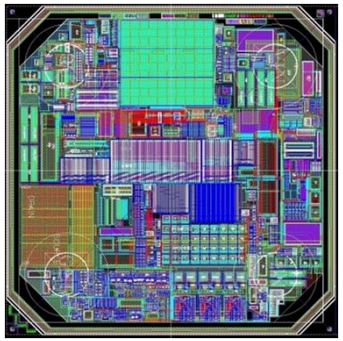

**Space Components Sales – Breakdown by regions (%)**

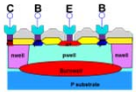
life.augmented

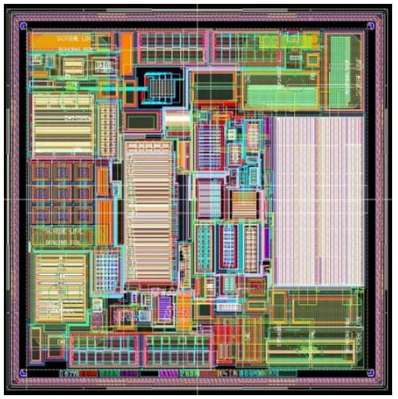
# ST portfolio for Aerospace



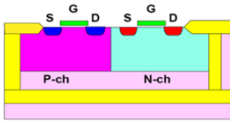

life.augmented

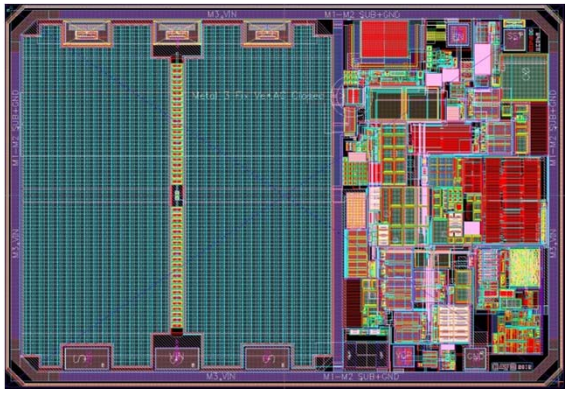


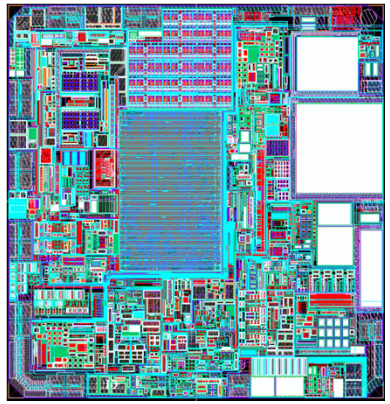


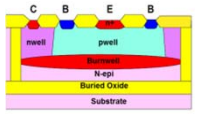



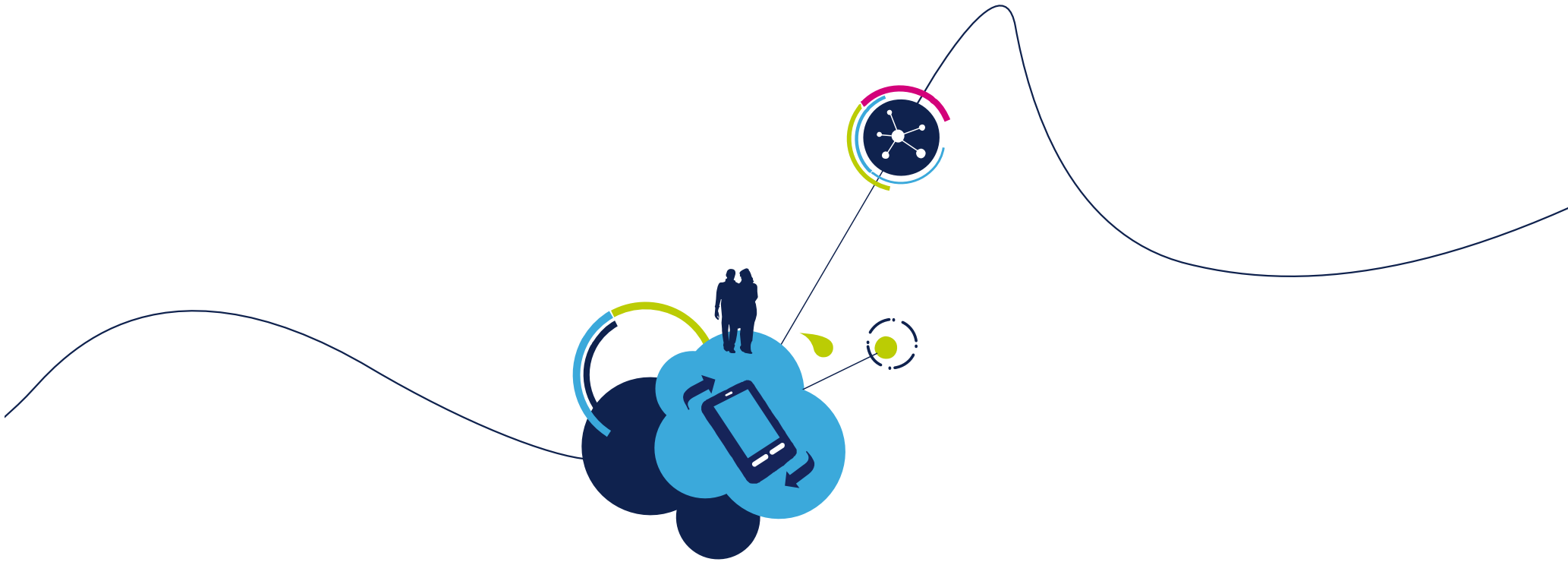
# BCD TECHNOLOGY OVERVIEW









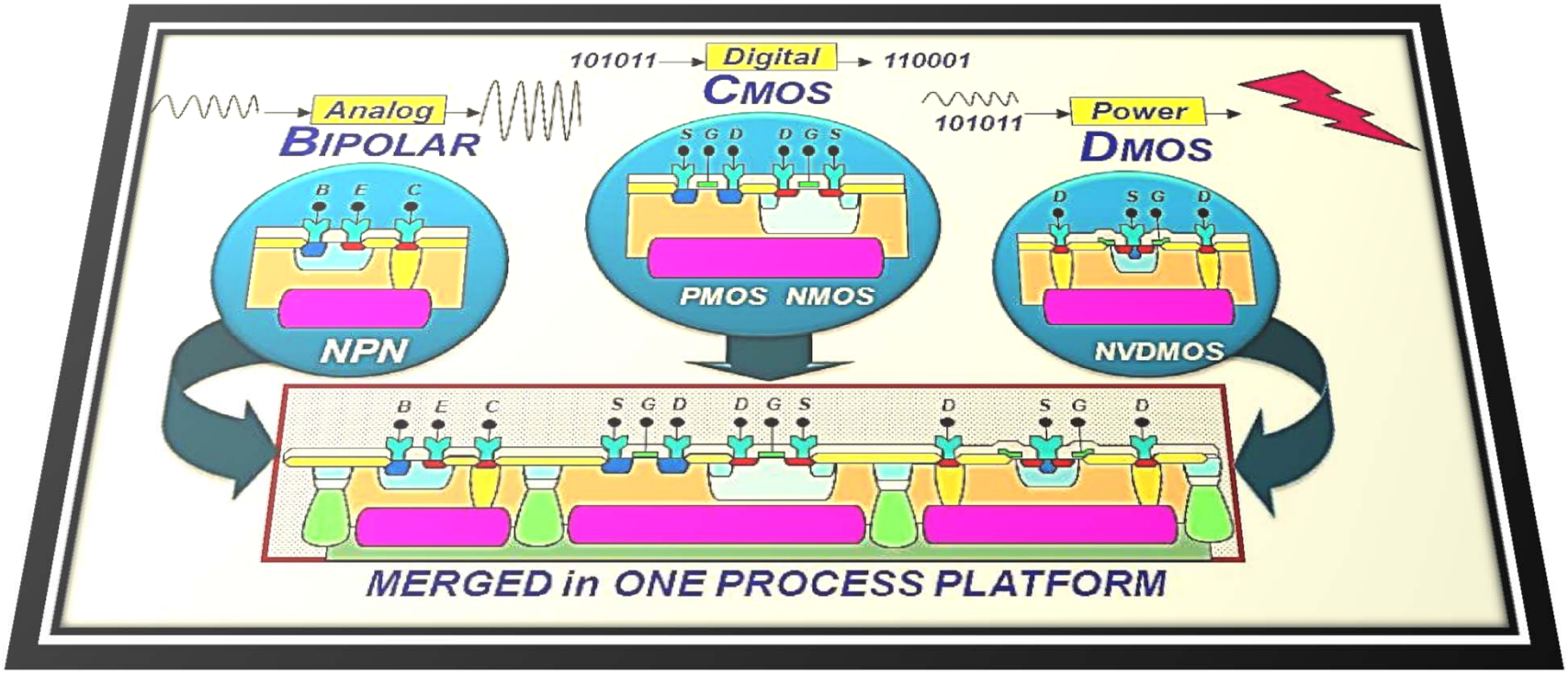
# BCD Smart Power Introduction

life.augmented

# BCD Smart Power



A concept invented by *ST* in the mid-80s [1][2][3] widely used today in the industry



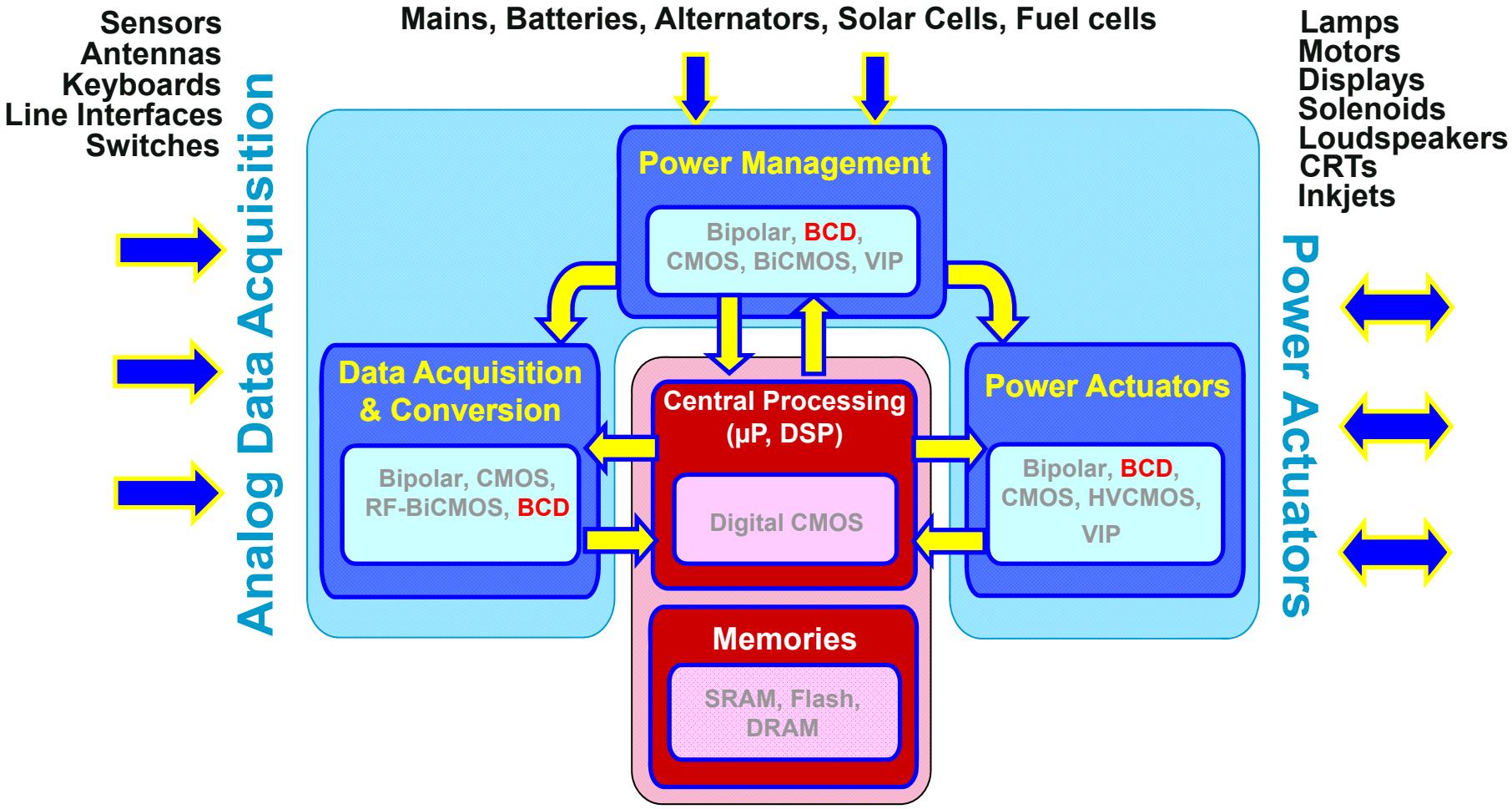

*[1] Single Chip Carries Three technologies,* **Electronics Week, December 10, 1984**

***[2] C. Cini, C. Contiero, C. Diazzi, P. Galbiati, D. Rossi, "A New Bipolar, CMOS, DMOS Mixed Technology for Intelligent Power Applications",* ESSDERC '85 Proceedings, Aachen (Germany), September 1985**

***[3] A. Andreini, C. Contiero, P. Galbiati, "A New Integrated Silicon Gate Technology Combining Bipolar Linear, CMOS Logic and DMOS Power Parts",* IEEE Transactions on Electron Devices, Vol. ED-33 No.12, December 1986**

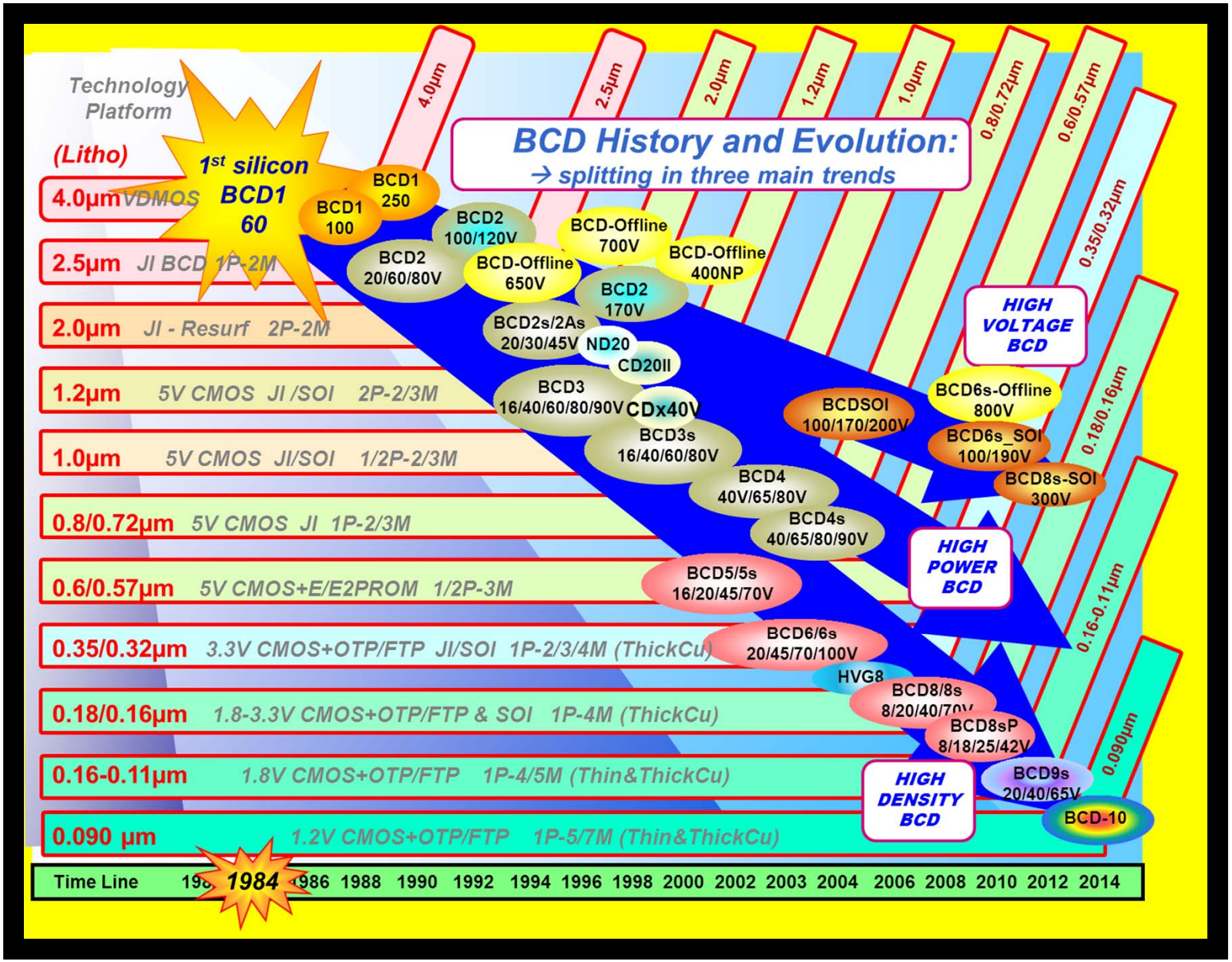
# BCD in Electronic System Partitioning



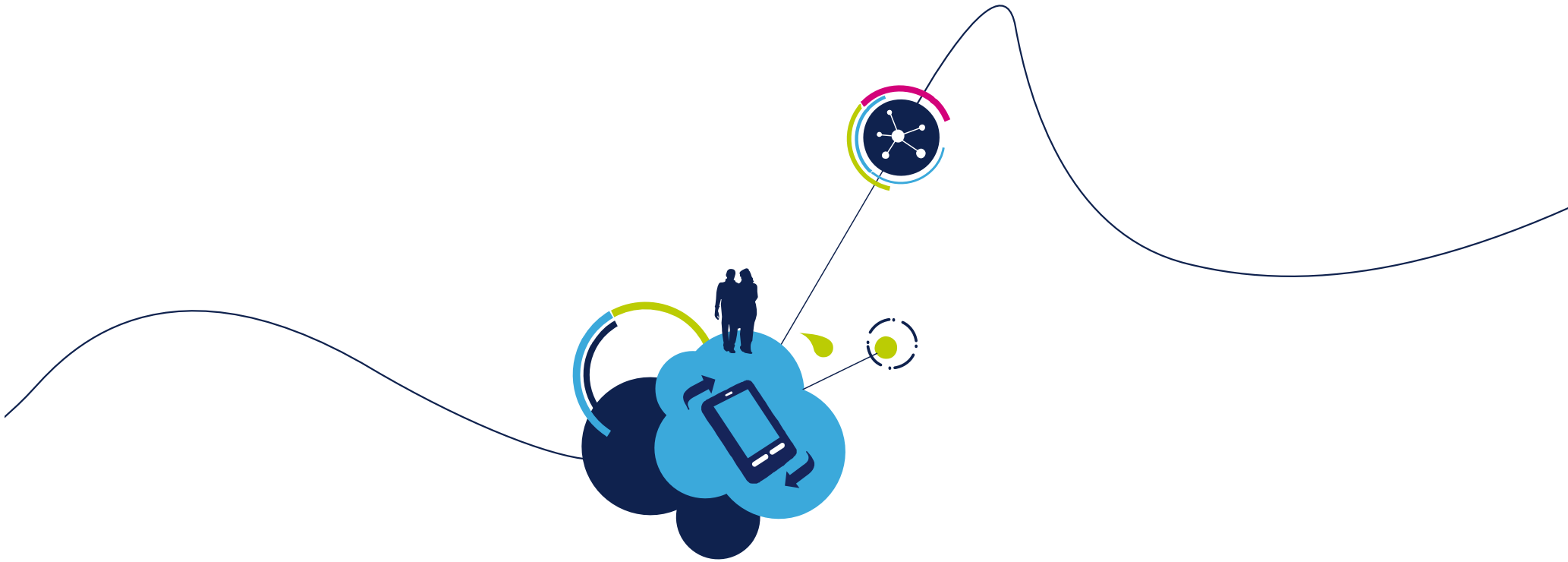


# 30 years ST BCD Roadmap (from 1984 to 2014)






life.augmented



# Smart Power Technology Roadmap

life.augmented

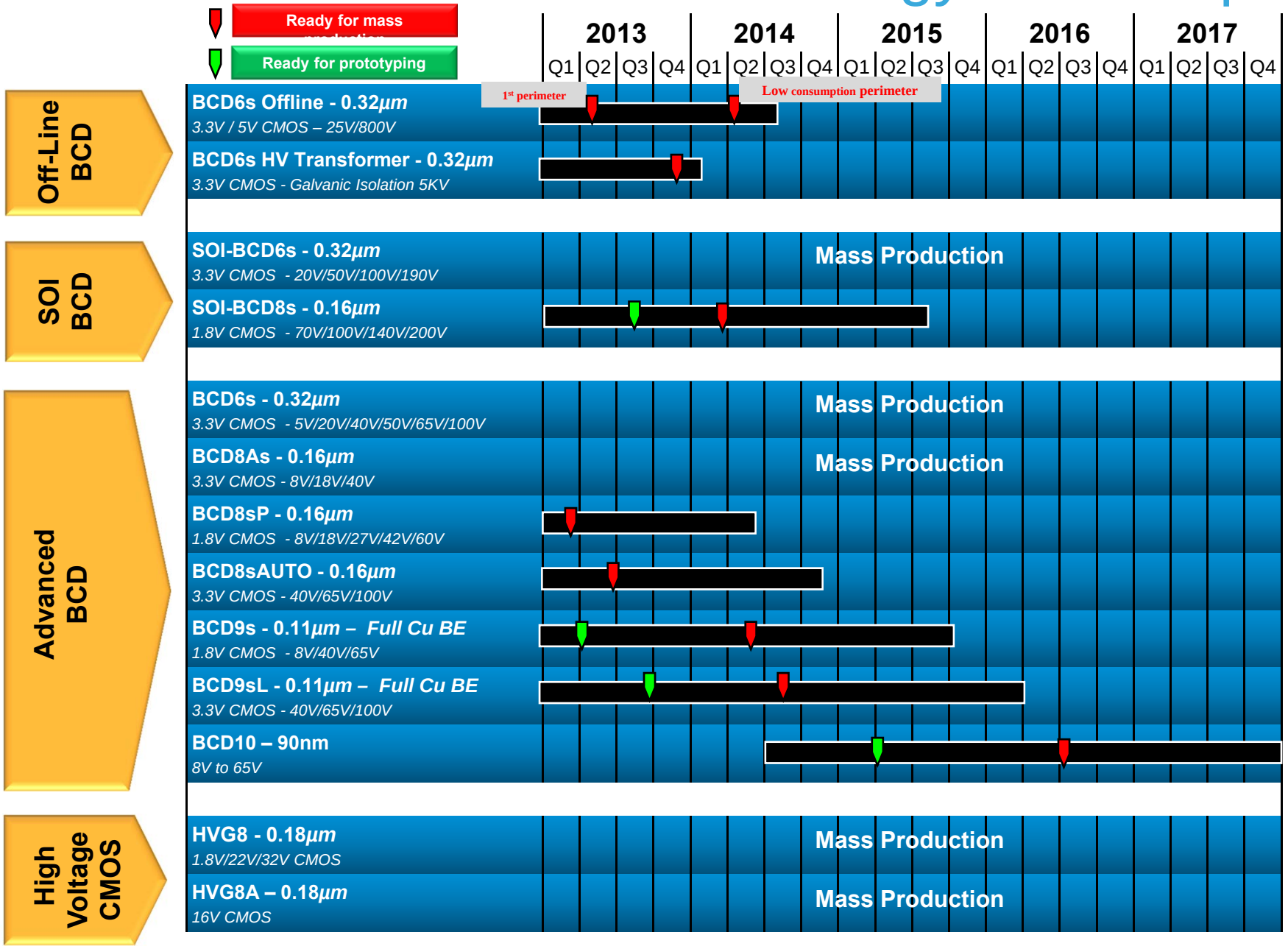
# Smart Power Technology Segments

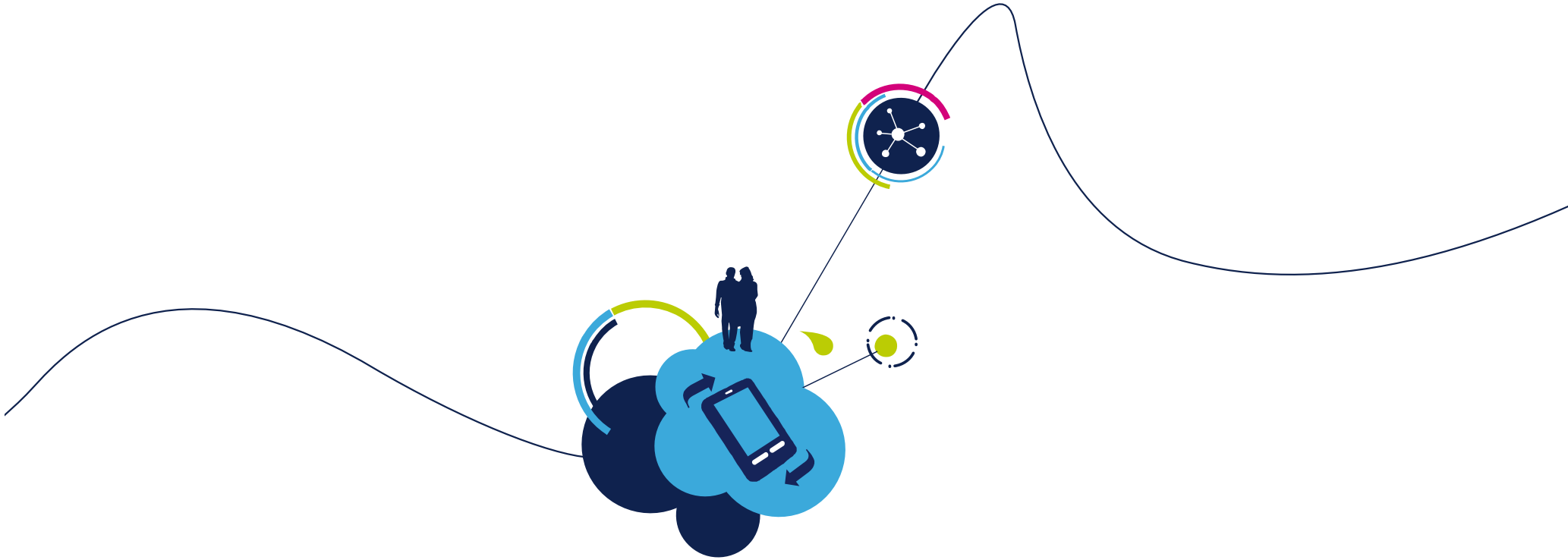


| Segment | Technology Platform | Application Fields |
|---|---|---|
| Off-Line BCD | **BCD6s Offline - 0.32µm**<br>*3.3V / 5V CMOS – 25V/800V*<br>**BCD6s HV Transformer - 0.32µm**<br>*3.3V CMOS - Galvanic Isolation 5KV* | Lighting, Motors, Electrical Car |
| SOI BCD | **SOI-BCD6s - 0.32µm**<br>*3.3V CMOS - 20V/50V/100V/190V*<br>**SOI-BCD8s - 0.16µm**<br>*1.8V CMOS - 70V/100V/140V/200V* | Full digital amplifier, Ecography, AMOLED, Pico-projector |
| Advanced BCD | **BCD6s - 0.32µm**<br>*3.3V CMOS - 5V/20V/40V/50V/65V/100V*<br>**BCD8As - 0.16µm**<br>*3.3V CMOS - 8V/18V/40V*<br>**BCD8sP - 0.16µm**<br>*1.8V CMOS - 8V/18V/27V/42V/60V*<br>**BCD8sAUTO - 0.16µm**<br>*3.3V CMOS - 40V/65V/100V*<br>**BCD9s - 0.11µm – Full Cu BE**<br>*1.8V CMOS - 8V/40V/60V*<br>**BCD9sL - 0.11µm – Full Cu BE**<br>*3.3V CMOS - 40V/65V/100V*<br>**BCD10 – 90nm**<br>*8V to 65V* | HDD, GDI, Airbag, Audio amplifier, Power Line modems, Printers, Body, ESP, ABS, Automotive, Power Supply, Power Management for portable |
| High Voltage CMOS | **HVG8 - 0.18µm**<br>*1.8V/22V/32V CMOS*<br>**HVG8A - 0.18µm**<br>*16V CMOS* | Bio Medical, Advanced Analog |

# Smart Power Technology Roadmap







# BCD6s

life.augmented

# BCD6s Overview



***BCD6s is a 0.32µm Technology Platform dedicated to Smart Power applications with the following main features:***

- **Baseline 3.3V CMOS**
- **Power devices from 5V to 100V**
- **Dual gate oxide process: 3.3V CMOS, 5V CMOS & Power Devices**
- **4 Metal Levels with Thick Power metal**
- **Available memory: OTP, FTP (EEPROM), RAM/ROM**

***Application examples:***

- **Hard Disk Drivers Power Combo**
- **Motor Drivers**
- **Printer**
- **DC-DC converter**
- **Power Management**
- **Automotive**

# BCD6s Device Portfolio

**Low Voltage**

- 3.3V CMOS
- 5V CMOS

**High Voltage**

- 5V/7V/12V/20V/30V/40V /65/100 NLDMOS
- 40V/50V NLDMOS Low Side
- 40V/52V NLDMOS High Side
- 5V/16V/20V/30V/40V PLDMOS
- 50V/65V/75V/100V PDEXT MOS
- 20V N/PDrift MOS
- 30V PDrift MOS
- 20V NLDMOS Collection Free

**Bipolars**

- 5V NPN
- 20V LPNP

**Diodes**

- 5V Zener
- 5V Floating Zener
- p+/Nwell, p+/HVnwell
- n+/Pwell, n+/Hvpwell
- 40V Low Leakage diode

**Capacitors**

- 3.3V/5V poly capacitors
- 12V poly-poly cap. (LL/HH

**Resistors**

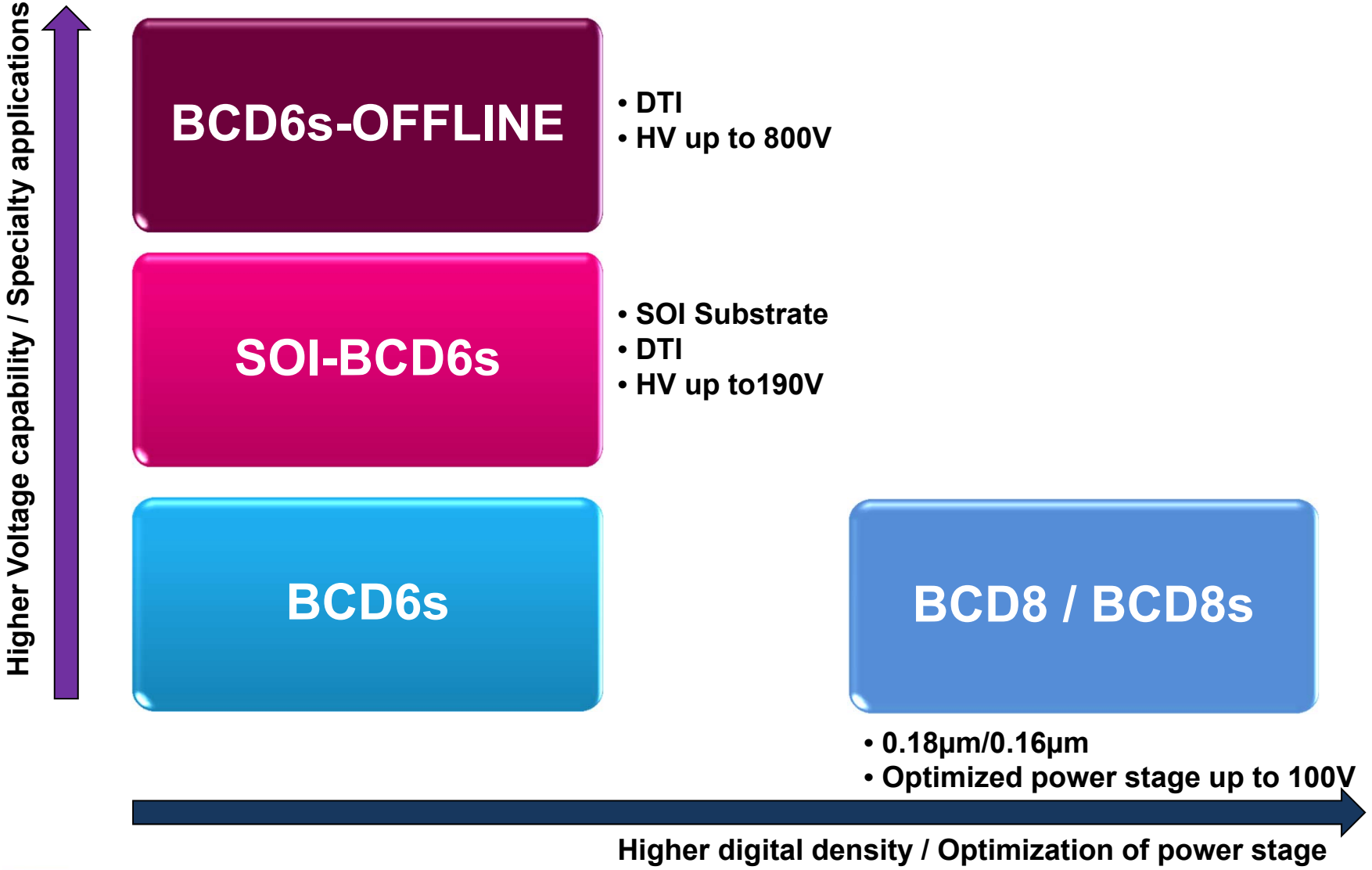
- Poly resistors, including HIPO resistor
- Diffused resistor

**ESD & IPs**

- Antifuse
- FTP
- SRAM / ROM
- ESD Macrocells

# BCD6s Evolution



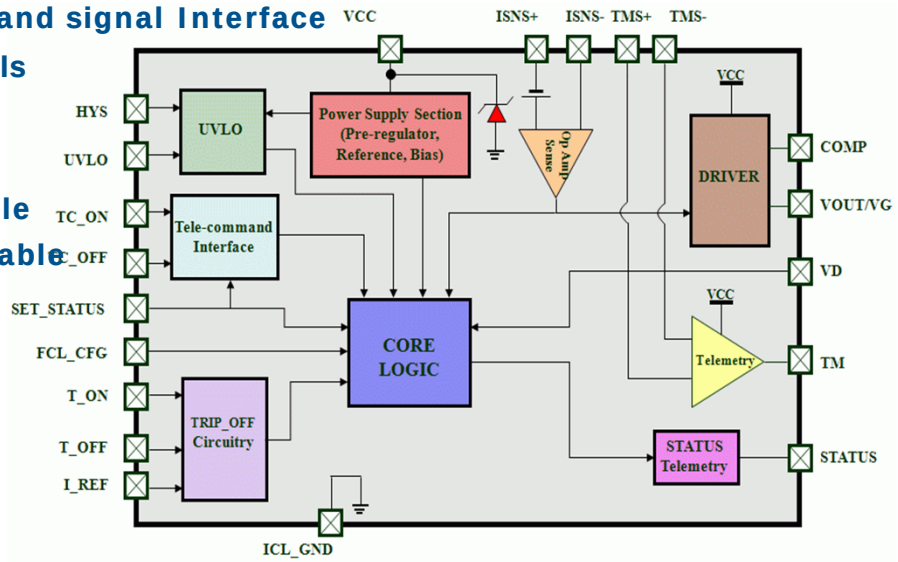



life.augmented

# STMicroelectronics: ESTEC Contract 22049-09-NL-AT
# Integrated Current Limiter

## MAIN FEATURES

- Wide Supply Voltage range (from 7.5V up to 52V DC)
- Very Low DC consumption (total SSP system < 3mA)
- ON/OFF SSP functionality by means external Tele-command signal Interface
- Immunity Noise Filter (~ 10ms) for Tele-command signals
- Current Limitation externally programmable
- Trip-Off Functionality in Current Limitation
  - $T_{ON}$ time (trip-off function) externally programmable
  - $T_{OFF}$ time (recovery function) externally programmable
- 3 different Operation Mode (hardware selection):
  - Latched (ON or OFF @ Start-up)
  - Re-triggerable
  - Fold-back Current Limiter
- Under Voltage Lock-Out detection:
  - $V_{TH\_ON}$ threshold externally programmable;
  - $V_{HYS}$ hysteresis independently and externally programmable
- Telemetry (analog current, digital status)
- Floating Ground Compatibility (20V Zener Diode Chain embedded)




**PROCESS: BCD6s – 70V option**

life.augmented

# ESTEC Contract 22049-09-NL-AT
# Integrated Current Limiter
## Project Coordinator: S.Pappalardo

***MAIN APPLICATION:***

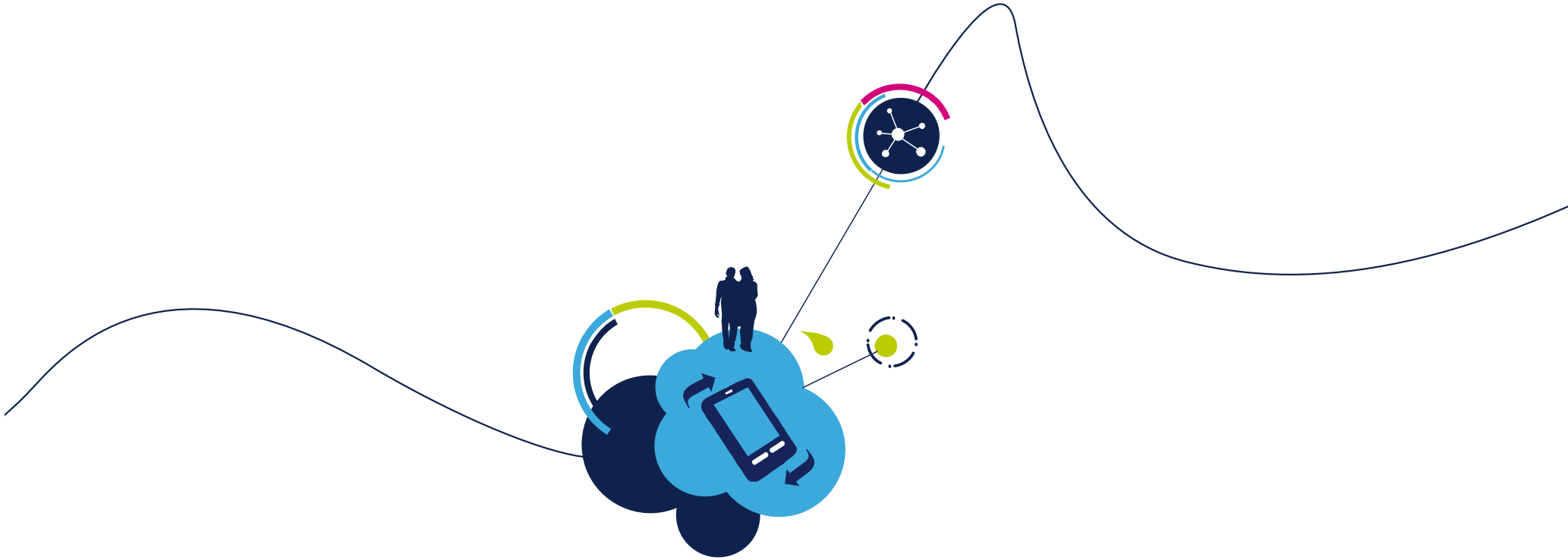
***Main Bus Protection from excessive current demands in Space Application***

- *ESA* Aerospace Science missions with $V_{MB}$ = 28V;
- LEO & GEO missions with $V_{MB}$ = 22V up to 40V;
- TELECOM with $V_{MB}$ up to 50V

***(even if for this application at present a fuse approach is preferred respect to a current limiter one)***

**WORKING PLAN & TIMELINE**

| Phase/Task | Title | Contractor | Timing | Completion |
|---|---|---|---|---|
| Phase I | Product Definition and Preliminary Design | | T1-T11 | 100% |
| Task 1 | Technology and Market Study | ST | | |
| Task 2 | Technology Feasibility Assessment and Preliminary Design | ST | | |
| Phase II | ICL Design Completion, Samples Production and Test | | T12-T20 | 100% |
| Task 3 | Detailed Design Completion | ST | | |
| Task 4 | IC Development Sample Manufacturing & Test | ST | | |



# SOI-BCD6s

life.augmented

# BCD on SOI History



- BCDSOI200:
  - 1 um minimum lithography
  - Up to 200 V operating voltage
- SOI-BCD6s:
  - 0.32 um minimum lithography
  - Up to 190 V operating voltage
- SOI-BCD8s:
  - 0.16 um minimum lithography
  - Up to 200V operating voltage
  - Development started within ENIAC – SmartPM funded project
  - Now is part of BCD technology roadmap

# SOI-BCD6s Overview



***SOI-BCD6s is a 0.32µm Technology Platform dedicated to High Voltage applications on SOI substrates with the following main features:***

- **Baseline 3.3V CMOS**
- **Power devices 5V-40V n/p LDMOS**
- **High Voltage Module including 50V/100V/190V N-ch and P-ch MOS**
- **Dielectric Isolation on SOI**
- **3 or 4 Metal Levels with last Thick Power metal**
- **Available memory: OTP, FTP (EEPROM)**

***Application examples:***

- **Display drivers: Plasma and OLED drivers**
- **Consumer and Automotive Audio Amplifier**
- **Automotive Sensor Interface ICs**
- **3D Ultrasound (ecography)**

# SOI-BCD Highlights



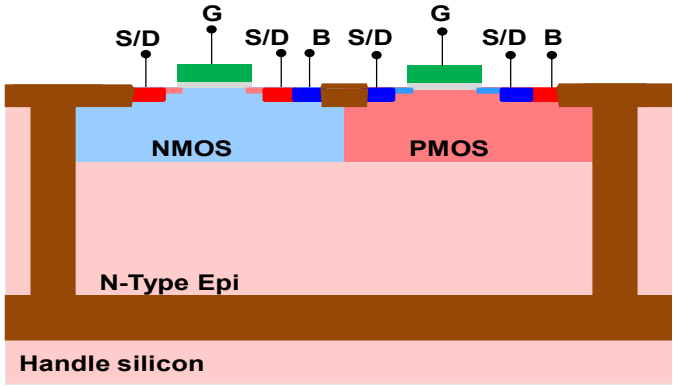
## SOI Isolation versus Junction Isolation

**Advantages**

- Parasitic bipolars elimination
- Reduced isolation distance
- **Below Ground capability**
- EMI robustness

**Drawbacks**

- Higher cost of substrate
- Parasitic capacitance
- Thermal effect




Example of CMOS devices fully isolated pocket

## *SOI BCD is **convenient** or even **mandatory** in case of:*

Ultrasound Probe ASIC

Amoled Power Supply

High Voltage

Noise Immunity

Below Ground pins

Low Consumption

Car Radio – Full digital amplifier

Automotive Sensor ASIC Airbag

life.augmented

# SOI-BCD6s Device Portfolio

**Low Voltage**

- 3.3V CMOS
- 5V CMOS

**High Voltage**

- 5V/12V/20V/30V/40V nLDMOS
- 5V/16V/20V/30V/40V pLDMOS
- 50V/100V/190V nDrift MOS
- 55V/100V/190V pDext MOS
- 150V/190V nLIGBT

**Bipolars & JFET**

- 5V NPN
- 20V LPNP
- 5V VPNP

**Diodes**

- 5V Zener
- p+/Nwell, p+/HVnwell
- n+/Pwell, n+/Hvpwell
- 50/100/190V diode

**Capacitors**

- 3.3V/5V poly capacitors
- 12V poly-poly cap. (LL/HH)
- 100/190V MOM

**Resistors**

- Poly resistors, including HIPO resistor
- Diffused resistors

**ESD**

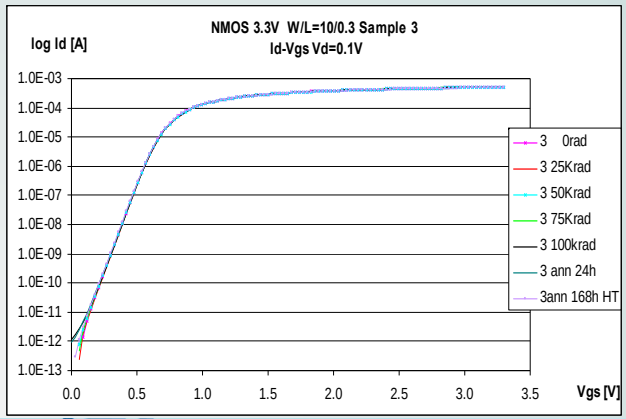
- 3.3V/5V/12V/20V/50V/100V/ 190V ESD protection

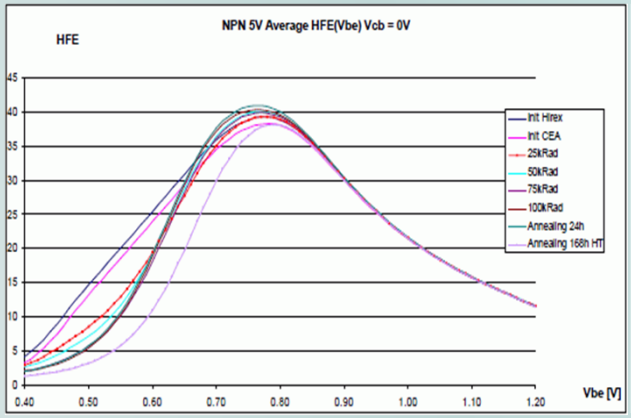
# BCD6s - Preliminary Radiation Campaign

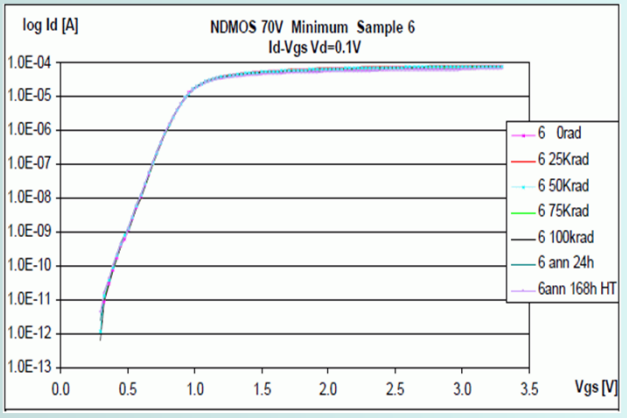
- **GOAL:** preliminary radiation hardness evaluation of BCD6s main elementary component
- **ACTIVITY: BCD6s** analysis of the RH performance of the main parameters and of the relative characteristic curves of main elementary component
- **BCD6s RADIATED ELEMENTARY COMPONENTS:**
  5V NPN, 3.3V NMOS, 3.3V PMOS, 100V Drain Ext. PMOS, 30V Drift PMOS, 20V NLDMOS, 30V NLDMOS, 45V NLDMOS, 70V NLDMOS, 90V NLDMOS, 100V NLDMOS (for all DMOS both min and power structures)

**RADIATION CAMPAIGN SETTING**

- **Irradiation Plant:** Pagure, CEA-Saclay (Paris)
- **Irradiation Contractor:** HIREX – France, ALTER-ITALY
- **Irradiation Source :** $Co^{60}$ gamma ray
- **Irradiation Type :** Total Ionizing Dose (TID)
- **Irradiation Dose Rates:** 30rads/sec
- **Irradiation Dose Steps:** 0rad, 25Krads, 50Krads, 75Krads, and 100Krads
- **Annealing Step Condition:** 24hours @room temperature + 168 hours @ 100°C



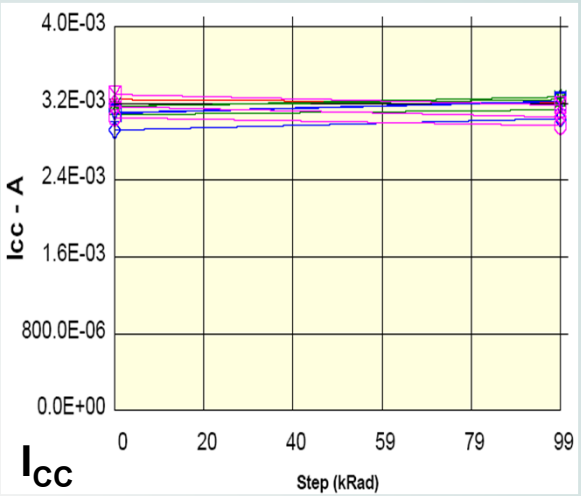
# BCD technology overview

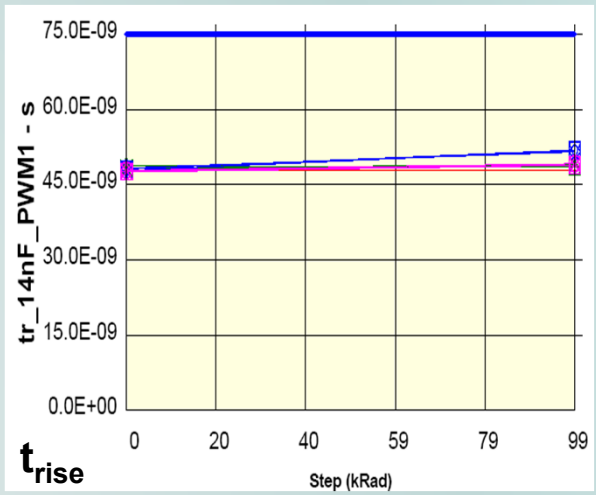
## TID RESULTS

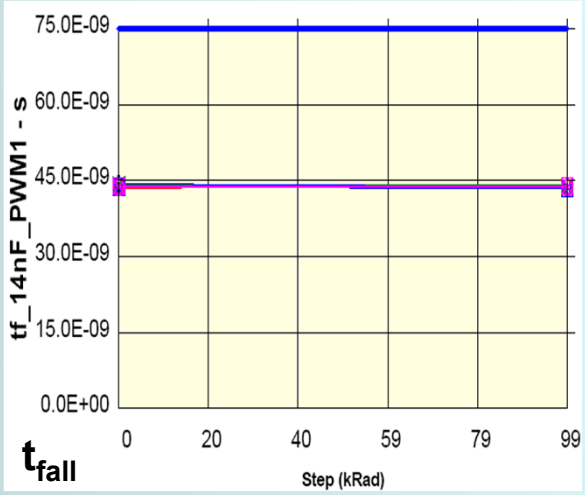
- ✓ **5V NPN:** Hfe degradation decreasing very slowly with the increase of the dose accumulate. Probable progressive saturation of the interface state creation on the base region, also if the accumulate dose
- ✓ **CMOS (3.3V Nch & Pch):** Negligible threshold voltage shifts and no leakage current until up to TID=100Krad for 3.3V
- ✓ **NLDMOS** → 30V signal structures are OK (only weak rebound after ageing)
  → signal structures ≥ 40V & all power Structure highlights in addition:
  - Leakage current due to overlap of the metal heating and of the radiation effect (It disappears after the annealing steps).
- ✓ **Pdrift MOS 30V** → regular behaviors for both Signal & Power Structures
- ✓ **PMOS Drain Extension 100V** → negligible variation of the $V_{TH}$; progressive increment of $R_{DSon}$ respect its value at 0rad;

**TID test have been performed with positive results also on a standard commercial product in BCD6s:**

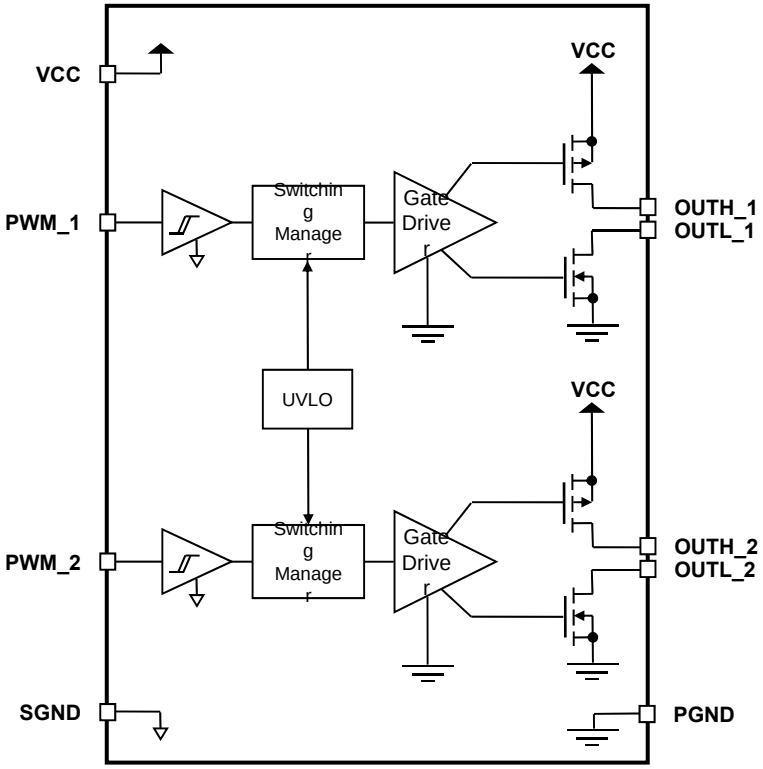
- ✓ **PM8834 Dual low side MOSFET driver**
  **Gamma ray Co60 radiation test, TID=100Krad, Dose rate 10rad/sec**



# ESTEC Contract 4200022783/10/NL/CP
# Low-side MOSFET Driver
## Project Coordinator: T.Signorelli




### *FEATURES*

- **Dual independent low-side MOSFET driver with 4A sink/source capability**
- **Wide input supply voltage range: 5 V to 18 V**
- **Driver output parallel ability to support higher driving capability**
- **Matched propagation delays**
- **CMOS/TTL compatible input levels**
- **Embedded driver anti-shoot-through protection**
- **Low bias switching current**
- **Short propagation delays**
- **Wide operative temperature range:**
  **-40°C to 105°C → (-55°C to 125°C AMR)**
- **Hermetic ceramic package qualified for space applications**
- **Two independent ground path (signal and power)**

**TECHNOLOGY:** **ST in-house Multipower BCD**
***fully operative up to 20V AMR with bipolar, CMOS & DMOS components available***

life.augmented

# ESTEC Contract 4200022783/10/NL/CP
# Low Side MOSFET Driver
## Project Coordinator: T.Signorelli

***MAIN APPLICATION:***
**spacecraft systems**
***DC-DC and DC-AC conversion and distribution where low power dissipation is required***

**WORKING PLAN & TIMELINE**

| Phase | Title | Contractor | Timing | Completion |
|---|---|---|---|---|
| **Phase 1** | *Feasibility Study, choice of in-house technology, definition of preliminary specification* | **ST** | **T1-T13** | **100%** |
| | TASK 1100: Analysis of Current Offer<br>TASK 1200: Characterization of Commercial Technologies<br>TASK 1300: Feasibility Study and Definition of the Target Device Datasheet | | | |
| **Phase 2** | *Technology Radiation Hardening, Design & Prototype Development and Manufacturing of Low Side MOSFET Driver, Full Characterization over the Mil-Temperature Range & Radiation Characterization* | **ST** | **T8-T22** | **100%** |
| | TASK 2100: Development Plan<br>TASK 2200: Manufacturing and Characterization<br>TASK 1300: Feasibility Study and Definition of the Target Device Datasheet | | | |
| **Phase 3** | *Production, Internal Qualification and ESCC Evaluation & Qualification Plan of RH Low Side MOSFET Driver* | **ST** | **T19-T36** | **30%** |
| | TASK 3100: Manufacturing and Characterization & Internal Qualification<br>TASK 3200: Radiation Testing<br>TASK 3300: ESCC Evaluation<br>TASK 3400: Eurocomp Newsletter and Commercial Evaluation<br>TASK 3300: ESCC Qualification Plan | | | |

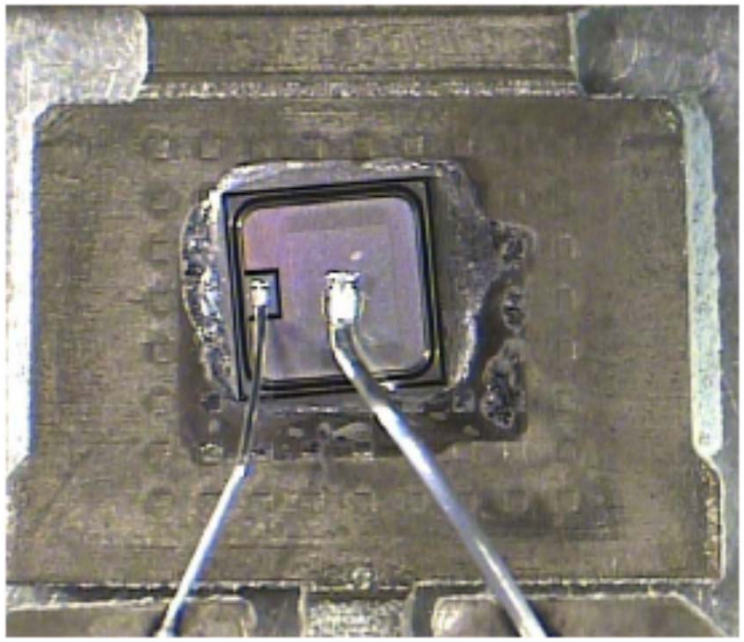
# STMicroelectronics: Rad-Hard enabling technologies for Power Management and Distribution for Aerospace

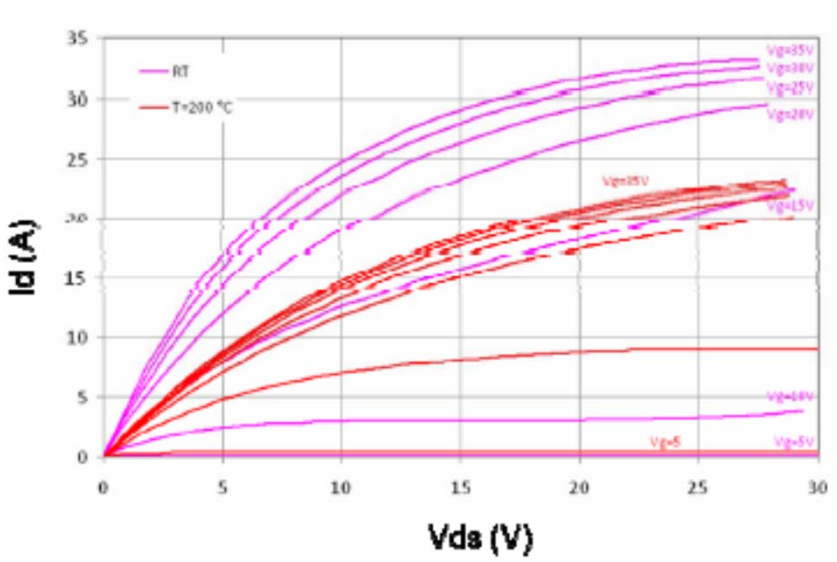
- **Used in Automotive :**
  - High Volume  -High Quality – Over 10 years availability
- **Best in Class Electrical Feature for Power**
- **Rad robustness demonstrated with several Radiation Trials**
- SEE : Dedicated Library under design
- ST Will widely use this Technology for Rad-Hard Power ICs
  - To be Qualified soon : Integrated Current Limiter – Low Side Driver

life.augmented

# SiC commercial PowerMOSFET








**Commercial samples by 2013**

**Main target**
**BVDss > 1200V**
**Id = 15A**

# Thank you