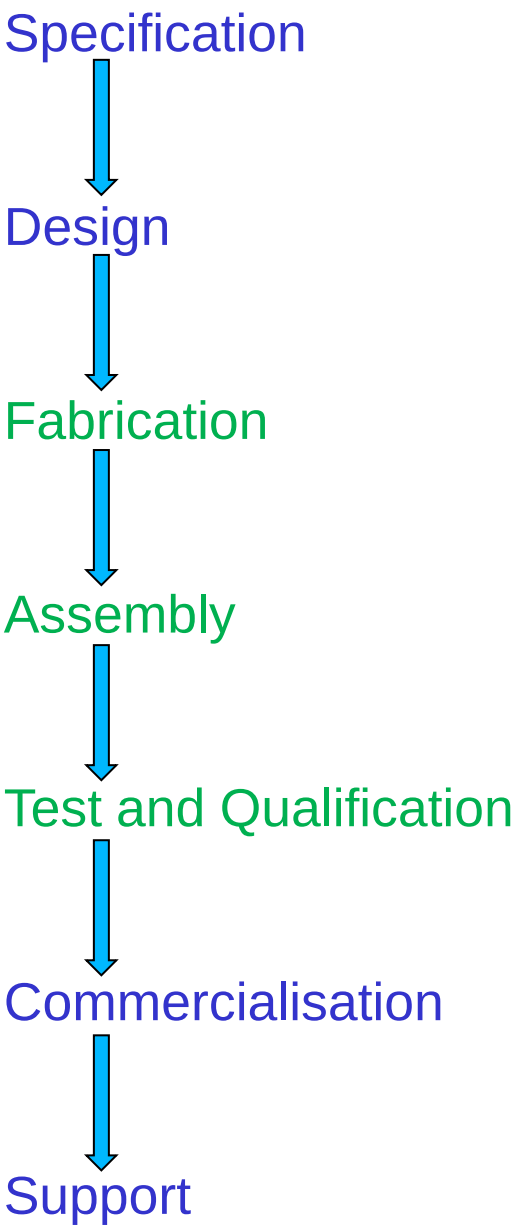
Aeroflex Gaisler Component Roadmap

ESCCON, March 14, 2013

Aeroflex Gaisler

- Design house since 2001 focused on microprocessors (LEON)
- Rich IP portfolio with 80 IP cores (GRLIB)
- The IP is provided with test benches, tools, SW drivers and support
- Business model:
  - To license customers IP for inclusion in ASICs and FPGAs.
  - To provide customers with radiation tolerant FPGAs pre-programmed with our IP.
  - To act as an fab-less supplier of space components
  - To provide customers with tools, SW environment and support

Aeroflex Gaisler Fab-less Model



- Aeroflex Gaisler has the capabilty for Specification, Design, Commercialisation and Support

- Aeroflex Gaisler relies on partners for Fabrication, Assembly and Test/Qualification

- Specification to test/qualification must be done outside the US to not be affected by ITAR. If a component designed for space enter the US it can not re-exported outside the US without DoD approval

Fabrication, Assembly and Test

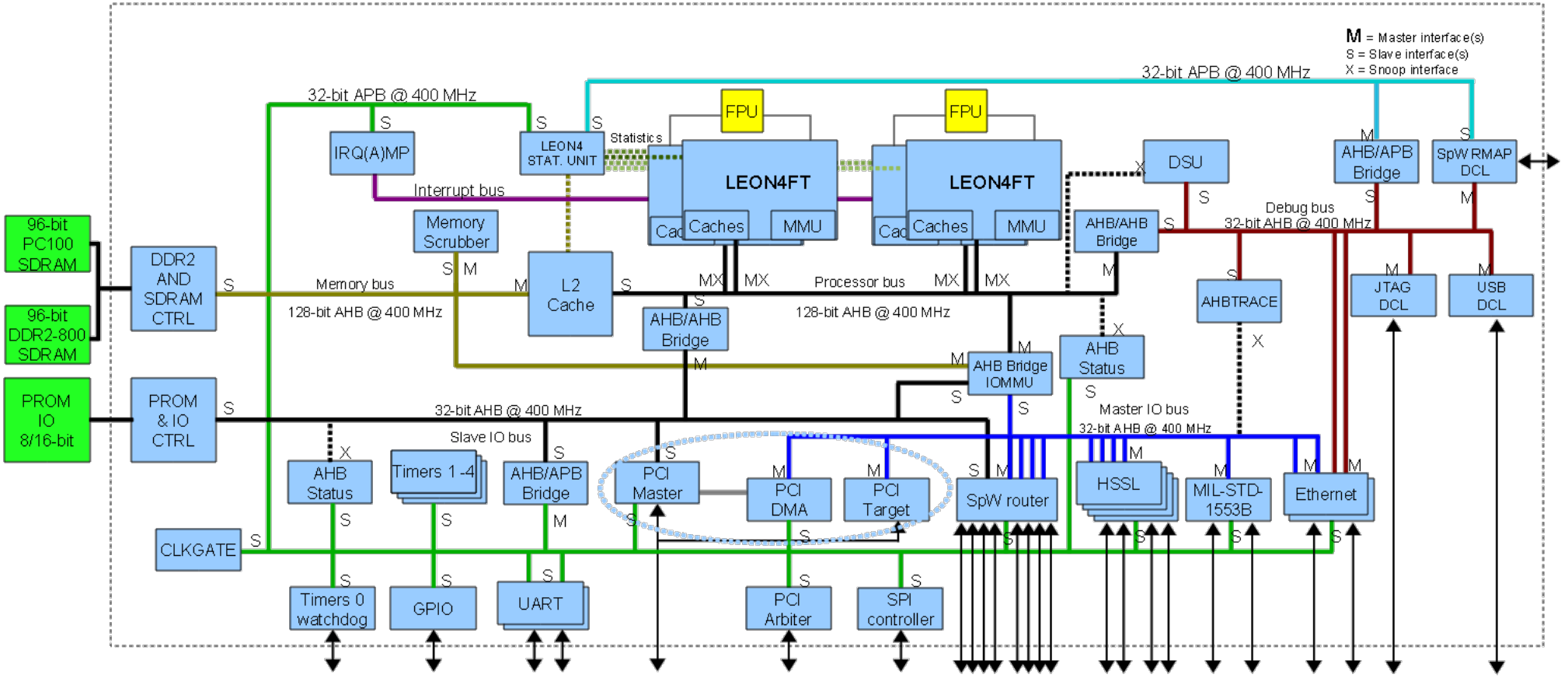
- All our IP is technology independent and can be synthesized to any ASIC or FPGA technology. Thus Aeroflex Gaisler can use any foundry.
- Radiation hardened ASIC cell library is a must.
- Today there are (non-US) libraries available from: Atmel, IMEC, Ramon Chip and ST Microelectronics (under preparation)
- Possible (non-US) foundries are: Atmel, ST Microelectronics, Tower, UMC
- Several options available within Europe for Assembly and Test

GR712RC

- The GR712RC is a high-performance (100 MHz) dual core microprocessor for a wide range of space applications
- Developed in co-operation with Ramon Chips and Tower (Israel)
- Features:
  - High-performance dual-core LEON3FT (250 DMIPS, 200 MFLOPS)
  - Radiation-hard (300 krad)
  - On chip peripherals: SpaceWire, 1553, Can, I2C, SPI, Eth, TM/TC
  - Software compatibility with LEON family
  - Robust packaging: CQFP-240
  - Class-S (tested according to Mil-std-883)
  - Now available
  - Designed into 12 new projects

NGMP – quad-core LEON4FT

- NGMP is an ESA activity to develop a multi-core system with higher performance compared to earlier generations of European space processors
- Targeting 65 nm ASIC technology

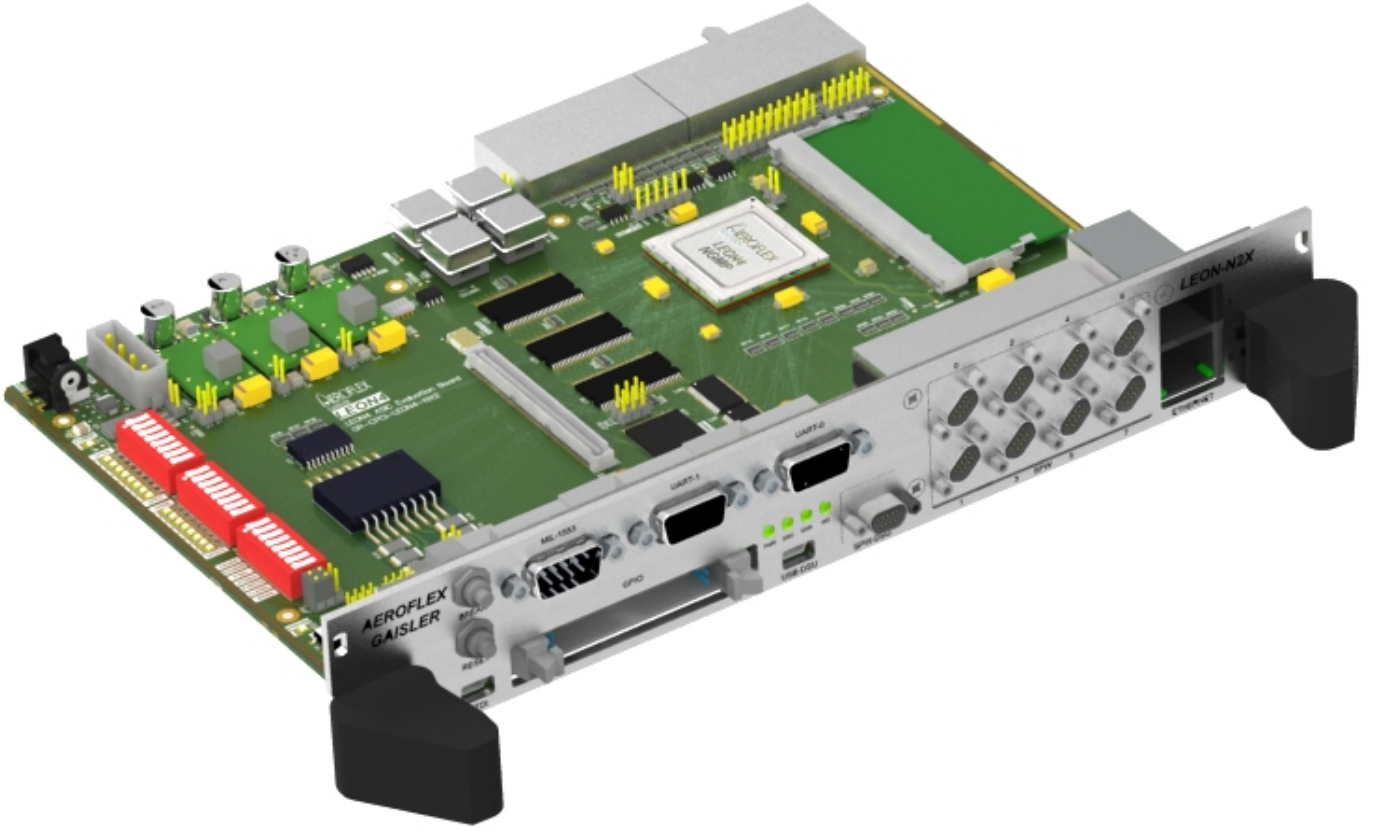


NGMP architectural summary

- Quad-core LEON4FT with two shared FPUs
- 128-bit L1 caches connected to 128-bit AHB bus
- 256+ KiB L2 cache, 256-bit cache line, 4-ways
- 64-bit DDR2-800/SDR-PC100 SDRAM memory interface
- 32 MiB on-chip DRAM
- 8-port SpaceWire router with four internal AMBA ports
- 32-bit, 66 MHz PCI interface
- 2x 10/100/1000 Mbit Ethernet
- 4x High-Speed Serial Links
- Debug links: Ethernet, JTAG, USB, SpW RMAP target
- 16x GPIO, SPI master/slave, MIL-STD-1553B, 2 x UART

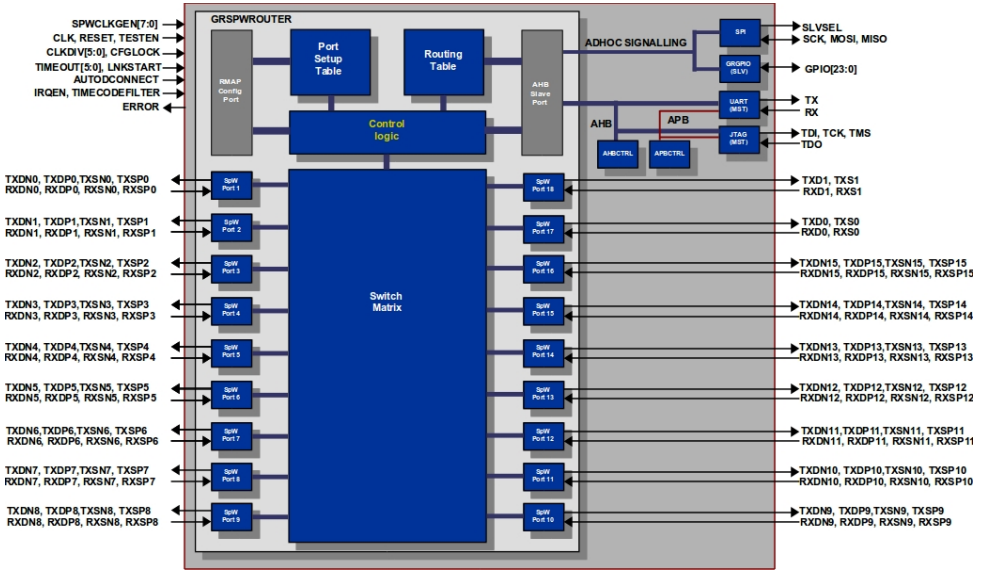
NGMP EVALUATION BOARD

- NGMP evaluation board and prototypes available now (non rad hard)
- Interfaces: CPCI, Dual RJ45 Ethernet, MIL-STD-1553B, 8 SpW ports, SpW debug comm. Link, 16 GPIO, USB-to-serial i/f providing access to UART and JTAG
- Flight parts available 2014 -2015 TBC

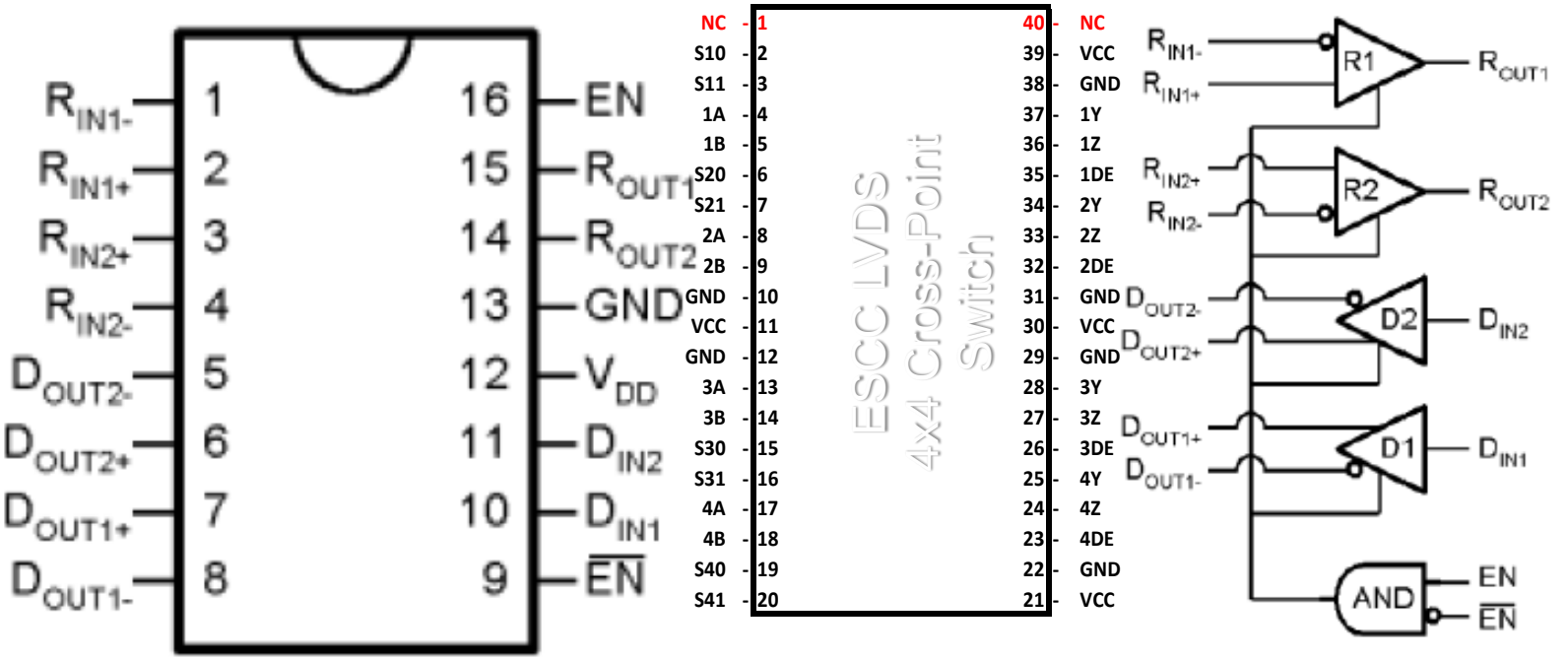


16 port SpW Router

- Based on existing SpaceWire router IP
- 16 SpW ports with on-chip LVDS and 2 SpW ports with LVTTL signaling
- 64 character deep SpW FIFOs
- RMAP configuration port
- Developed in co-operation with IMEC using the DARE 180nm library
- Robust packaging: CQFP-256
- Prototypes available 2013, qualified (ESCC) flight parts in 2014



LVDS Transceivers



- LVDS dual transceiver and cross-point switch
- Developed in co-operation with IMEC using the DARE 180nm library
- Robust packaging: FP-16 and FP-40
- Prototypes in 2013
- Qualified (ESCC) flight parts in 2014

Challenges

- To get a ESCC approved process (from design to qualified chip)
- Access to (non-US) radiation hard libraries for new processes (90, 65, 40 nm)
- Qualified high density packages. Today we are limited to 352 pin quad flat package. Next generation microprocessor will require 600+ pins and flip-chip technology