Development Status of JAXA EEE Parts

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(ESCCON)
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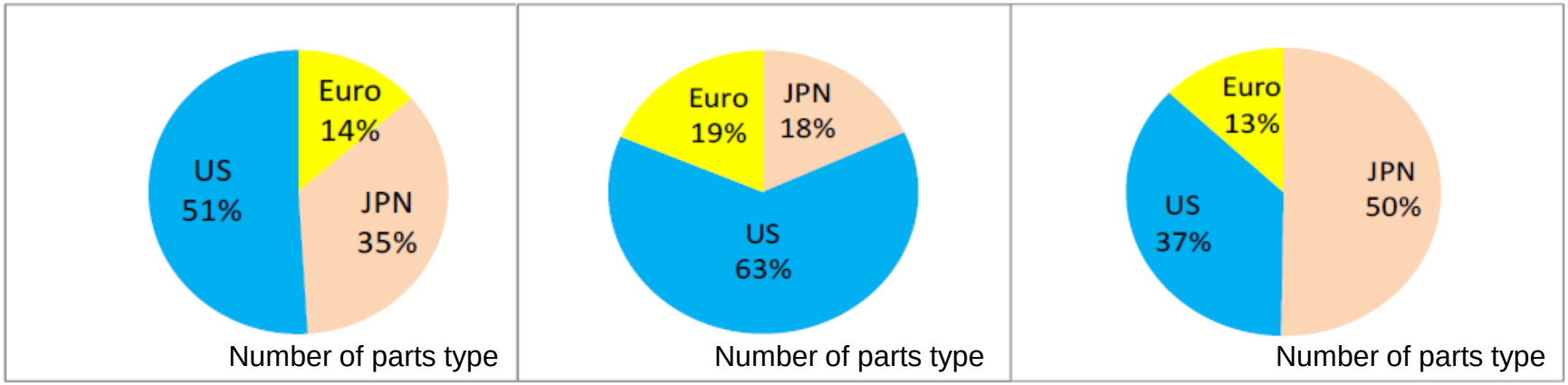
Norio Nemoto
Electronic Devices and Martials Group
Aerospace Research and Development Directorate

JAXA

Background

The surveillance report of parts occupation of JAXA spacecraft shows deep dependence of imported parts.



Total | Semiconductor | Passive Parts

Quality and procurement of imported parts is critical for JAXA space systems development.

Strategy of JAXA parts program

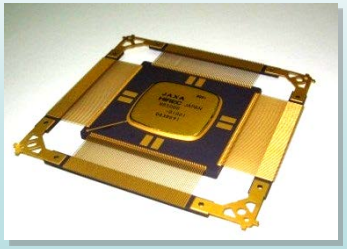
(1)Development of strategic EEE parts. (strategic EEE parts : the high- function and high-intensity IC, etc.)
(2) Cooperation with foreign entities
Improving independence of ITAR by cooperating with European countries
(3) Improvement of imported parts procurement
(ensuring the quality of the imported parts)
(4) Promoting utilization of JAXA Qualified parts
(5) R&D for the advanced technologies
(challenging for the breakthrough)

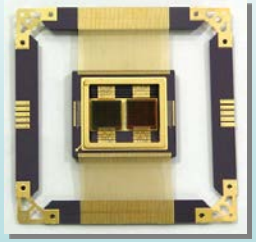
Strategic parts in satellite

Using domestic technologies, maintain independence and ensure acquisition of necessary performance of the space system.

Observation and attitude control equipment etc.

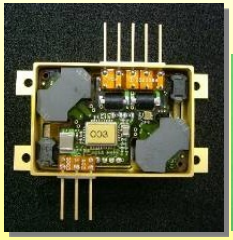
MPU, SRAM, FPGA etc.

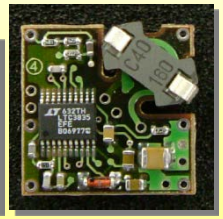




Power devices

DC/DC, MOSFET, POL



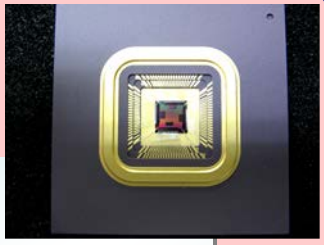


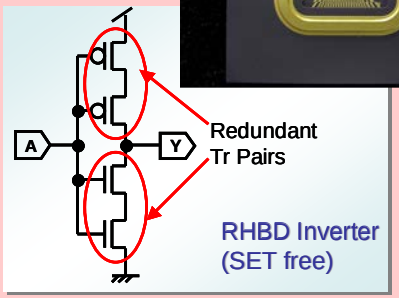
1. SOI-ASIC

(FPGA, Analog–Digital Mixed AISC)

Research and Development Based on 0.15um SOI Technology

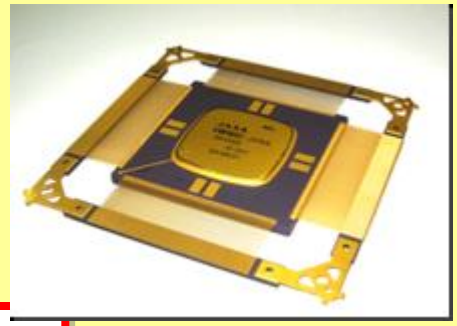
Radiation hardness ASIC was developed based on SOI and RHBD technology



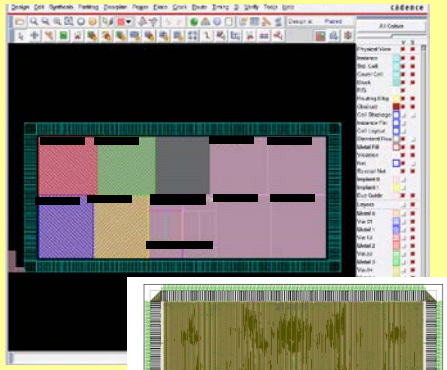


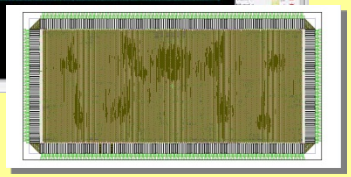
Research of RHBD circuit

SOI Device Development



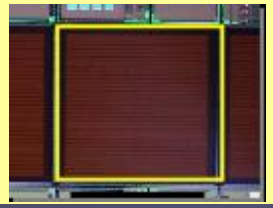
64bit MPU HR5000S





SOI-ASIC

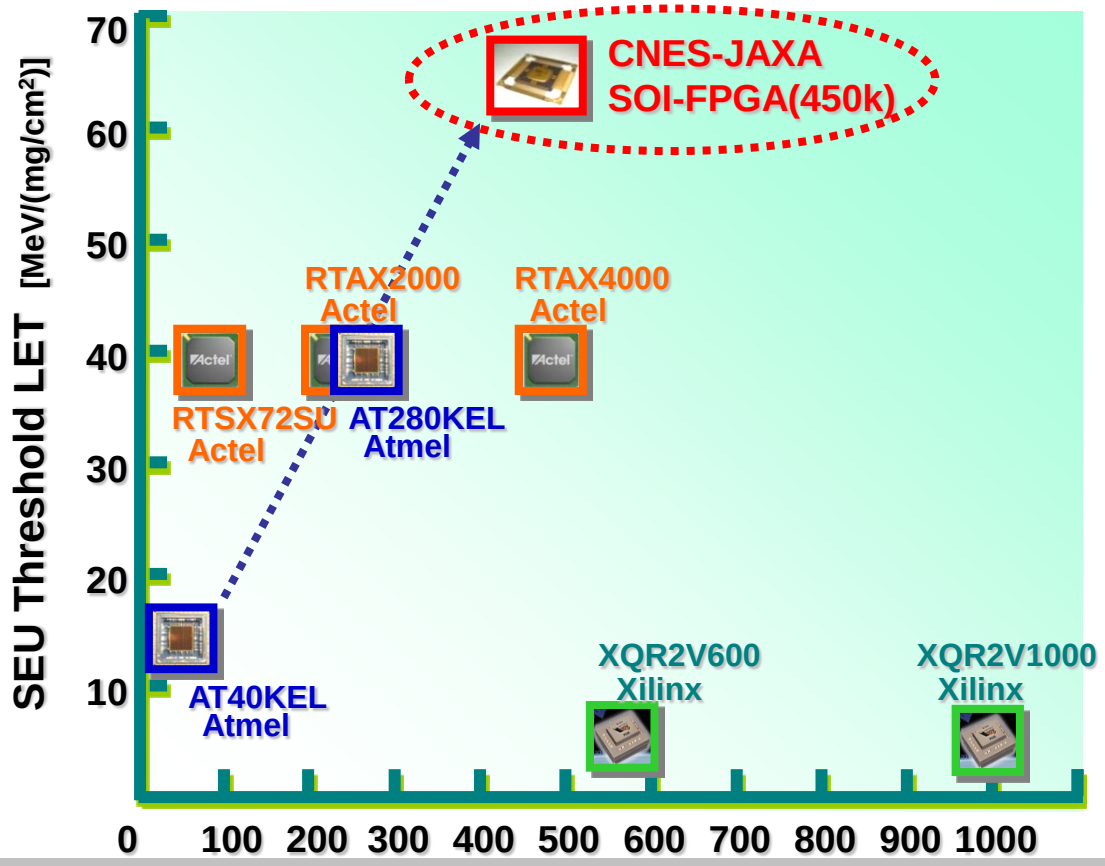
SOI-FPGA (developing: JAXA-CNES)



Applying to science and earth observation satellite

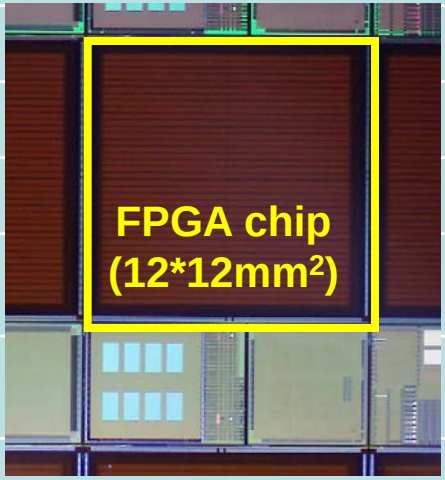
SOI-FPGA Development

FPGA is one of important device for recent space application.
But FPGA for space application is dominated by oversea company.
To reduce the risk such as failure, long read time etc., high reliability and high performance SOI-FPGA was developed.



450k SOI-FPGA Features

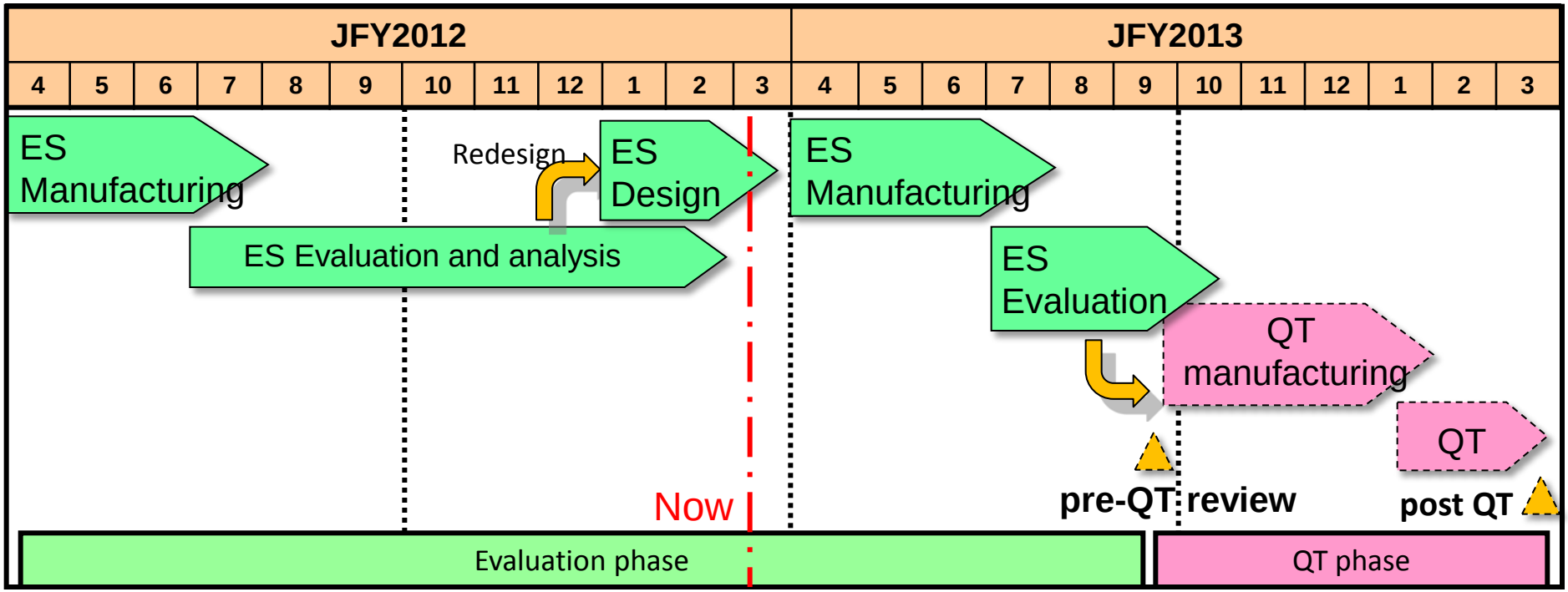
Term	General outline
1. Features	450k gate SRAM based FPGA designed for space use (FPGA chip and 4Mbit EEPROM (ESCC) assemble in same package(MCM))
1-1. Package	352 pin CQFP (Multi-Chip-Module)
1-2. Usable I/O pin	234 pin
1-3. Supplied voltage	1.5 V / 3.3V (FPGA chip), 3.3V (EEPROM chip)
2. FPGA chip	
2-1. Architecture	Atmel SRAM based FPGA Architecture
2-2. Process	0.15um CMOS SOI process for space use
2-3. Gate	450k ASIC gate (152 x 152 Corecell* block)
2-4. Internal performance	120 MHz
2-5. Power dissipation	600nW / core cell / MHz
2-6. Radiation performance	TID: 1 [kGy(Si)], SEU: LET_{th} > 64[MeV/(mg/cm^2)] SEL: free (SOI)



*Corecell : Atmel FPGA architecture, two 3-input LUT or one 4-input LUT, one DFF

SOI-FPGA Development Status

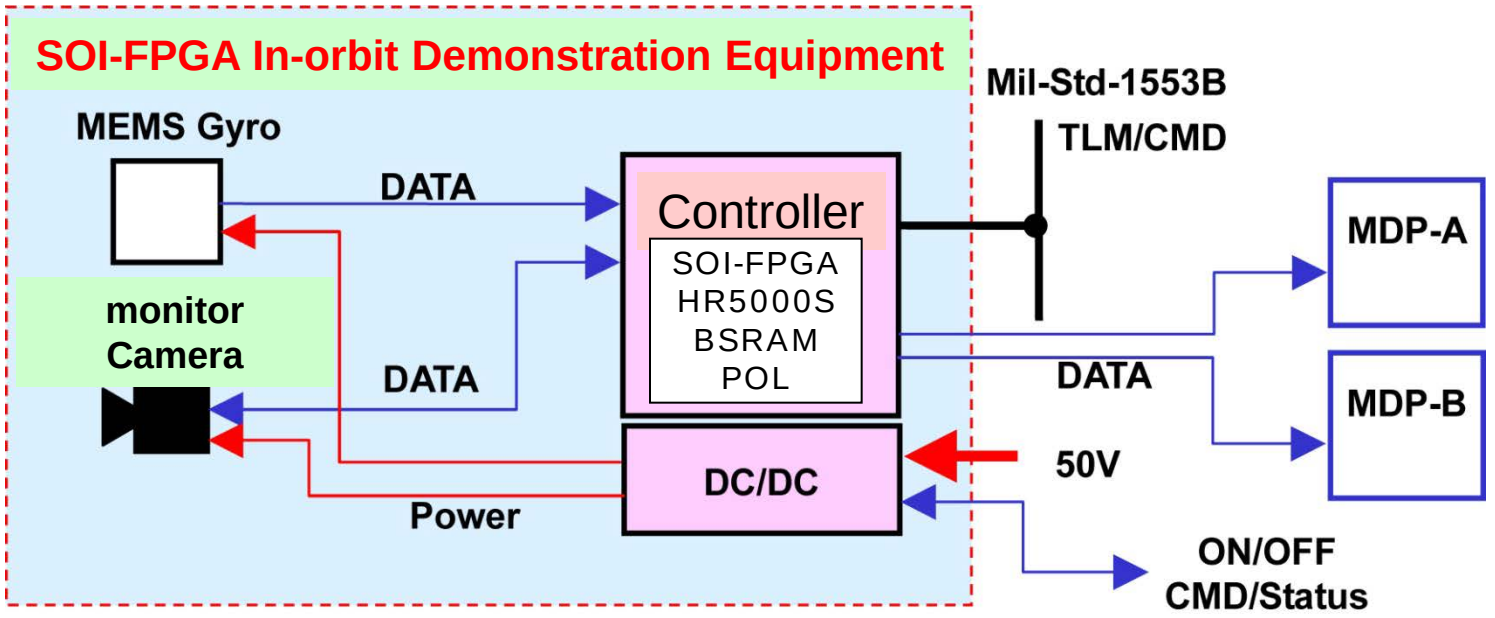
- Engineering Sample (ES) had some problems in designing such as read-back functional errors which are used only during the Evaluation phase. Any other basic functions have been confirmed to operate properly.
- A solution for the design problems was developed and ES is currently re-designed.
- ES evaluation will be completed by the end of September
- QT of SOI-FPGA will be completed by the end of March
- SOI-FPGA will be apply to EPPL



SOI-FPGA In Orbit Demonstration

SOI-FPGA In-orbit Demonstration Equipment(SOFIE) was in-orbit demonstration equipment of FPGA and strategy devices. Purpose of this equipment is to evaluated of radiation immunity and re-programing of FPGA in LEO.

SOFIE consists of Controller, MEMS Gyro and monitor camera. SOI-FPGA and strategy devices (HR5000S, DC/DC, POL and BSRAM) were used in the controller.



SOFIE Development Status

2011 : BBM design, manufacture, evaluation
2012 : PFM design, manufacture, evaluation
2013-Jan. : Assembled in ALOS-2
2013 : launch and data analysis

On-orbit data shared with ESA and compare with ground radiation test data.

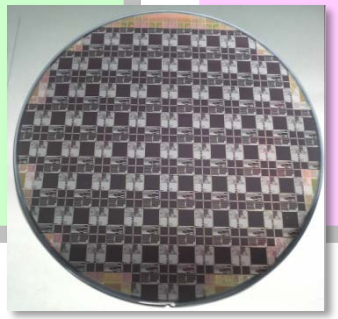
SOI-ASIC Future Plan

Expanding the use of 0.15um SOI device to space application, JAXA started to prepare IP library and basic evaluation.

IP Library for space application

Developed (～September 2012)

- **High-speed I/O buffer**
- **high-speed RHBD SRAM**
- **PLL (Phase locked loop)**

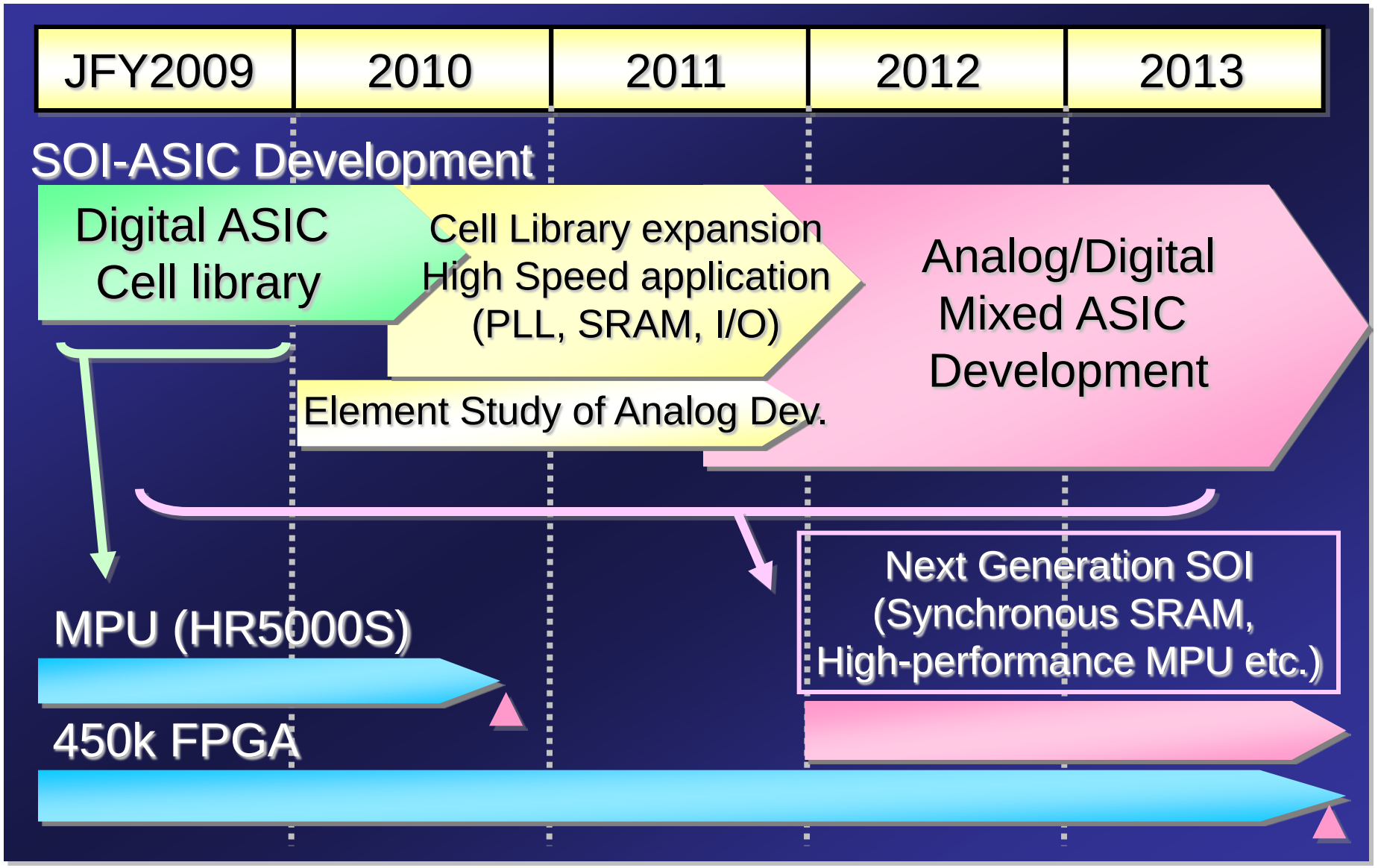


Digital and Analog Mixed ASIC process

Basic evaluation (2011~)

Test sample evaluation was started from 2011. 12bit 50Msps ADC evaluation sample will be evaluated by the end of September 2013.

0.15um SOI-ASIC Development Road Map



2. Power Device

(DC/DC converter controlled H-IC,
Next generation Power-MOSFET)

Background of Power control HIC development

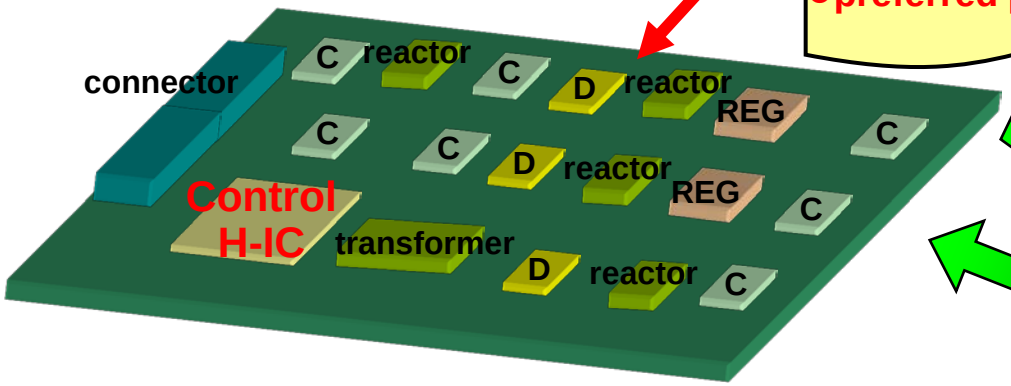
- Small size and lightening of the application system by sharing power supply
- Power voltage mainly used in space application is +5V, +-15V, +29V
- It is difficult to assemble those four output in single H-IC because of their size

A part of the control circuit is made in H-IC and sharing system

- ☑ Control IC and other passive parts are packaged in single H-IC package (control H-IC)
- ☑ Control IC is developed based on JAXA qualified POL device.
- ☑ Control H-IC and other passive parts is assembled on Printed Circuit board (see next page figure)

Plan of DC/DC converter Circuit Board

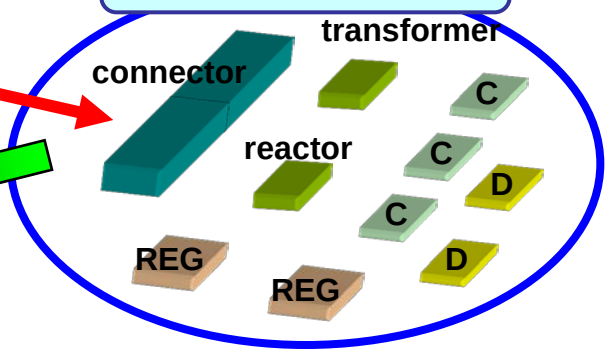
Power Board



Design Guideline

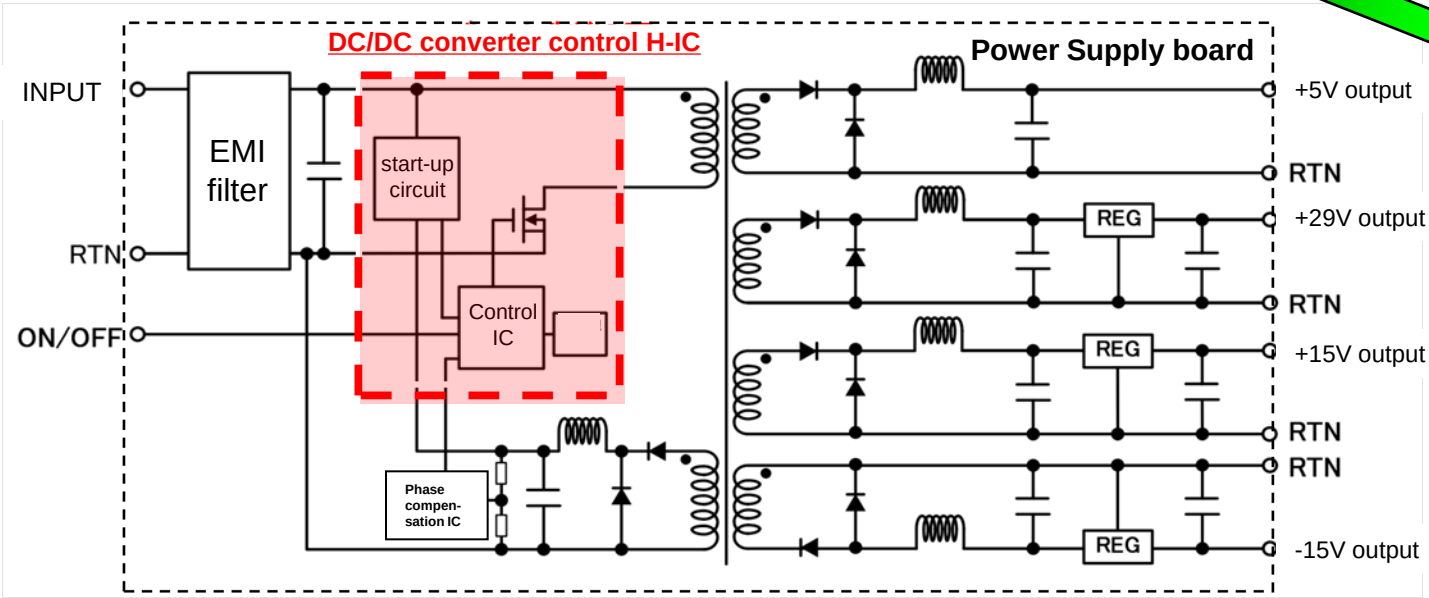
- reference pattern
- preferred parts list

Discrete Parts



Hybrid-IC (Qualified part)

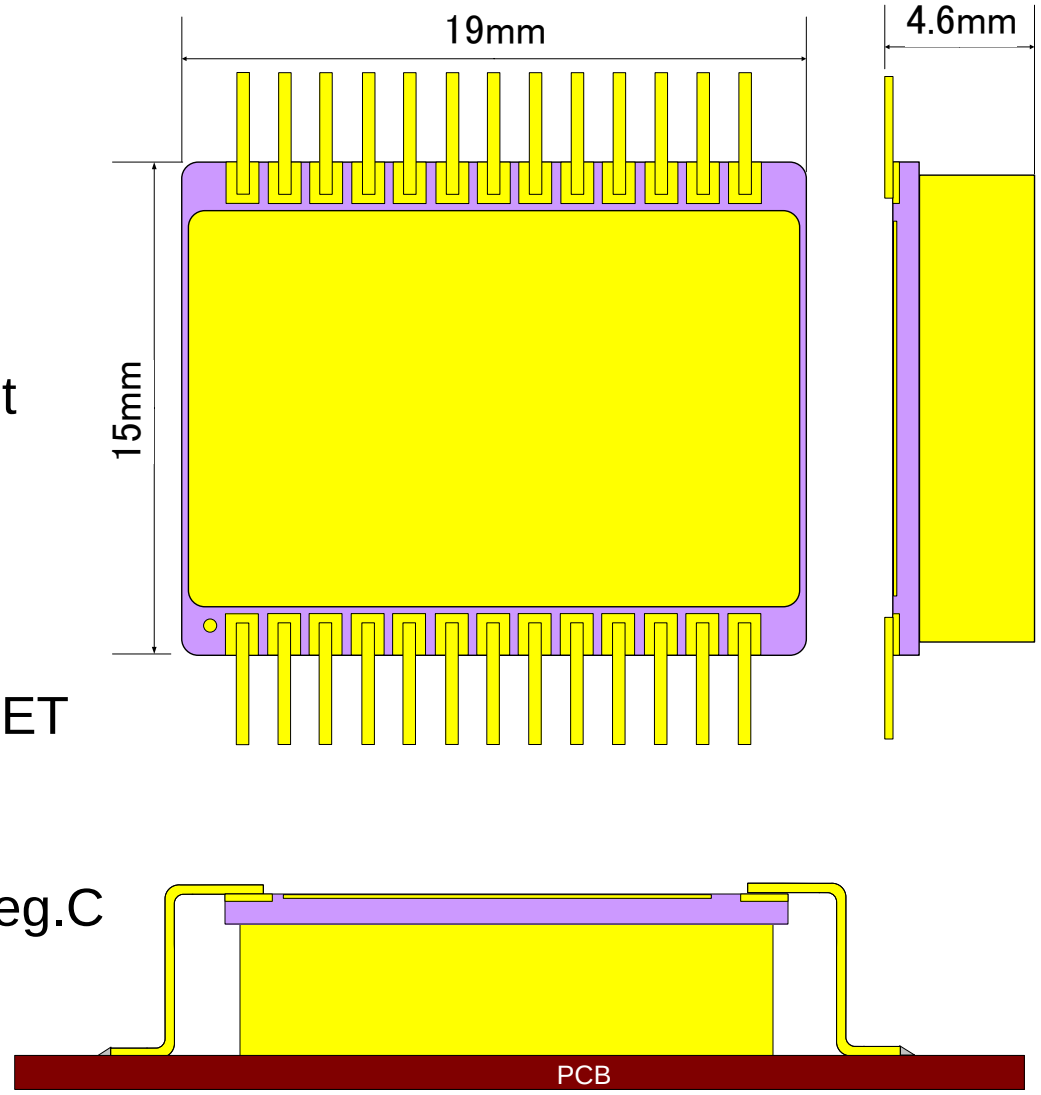
Control H-IC



Power Control H-IC Specification (tentative)

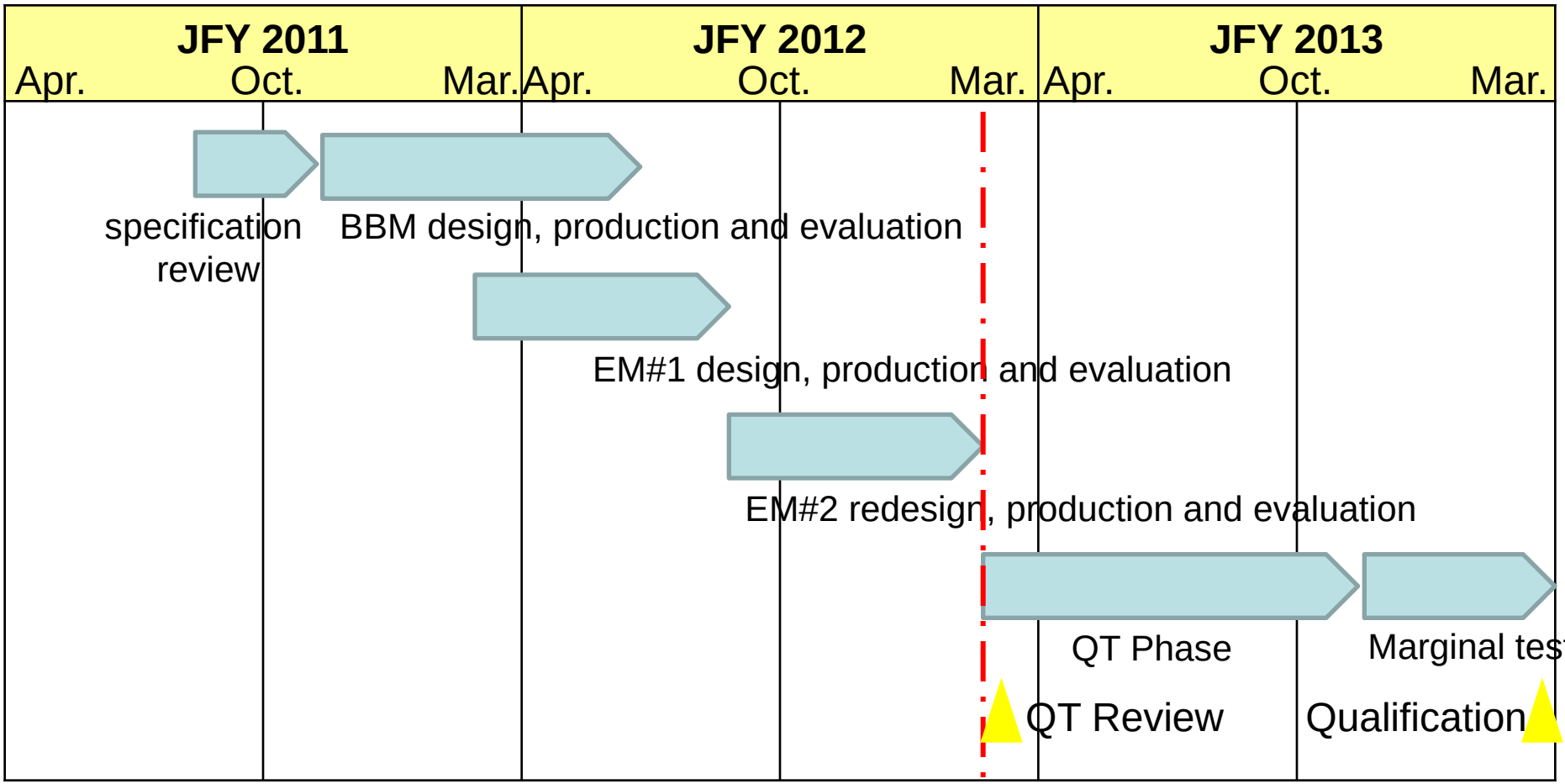
[Tentative Specification]

1.Channel: 1ch output
2.Control method: PWM
3.Control mode: voltage and current
4.Input voltage: 28V to 52V, 100V
5.SYNC input voltage: 5.5V
6.Switching freq.: 100 to 300kHz
7.PowerMOSFET drive capability:
All JAXA qualified PowerMOSFET
8.TID : 1kGy(Si)
9.SEE : 64 MeV/(mg/cm^2)
10.Operating Temp. : -55 to +125 deg.C



H-IC Package

DC/DC converter control H-IC schedule



Background of Next Generation PowerMOSFET

- ✓ In 2007, n-ch PowerMOSFET was qualified and registrated in EPPL in 2010. Approximately 7000 were already shipped to European
- ✓ In 2010, p-ch PowerMOSFET was qualified and is under coordination for registration on EPPL.

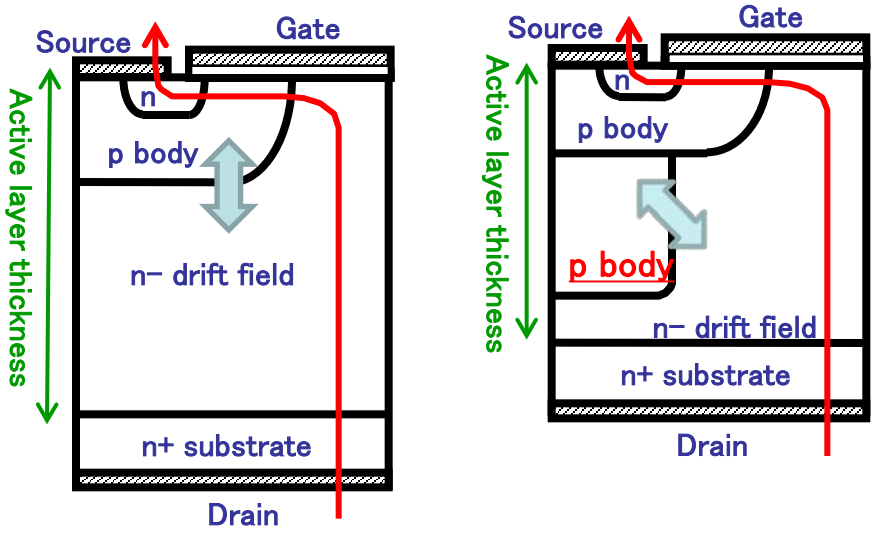
Next Generation PowerMOSFET targets as follows;

- ➢ Increasing SEGR tolerance
- ➢ Reducing static drain-to-source on-state resistance($R_{DS}ON$)

Qualified Parts technology
(SEGR tolerance)

+

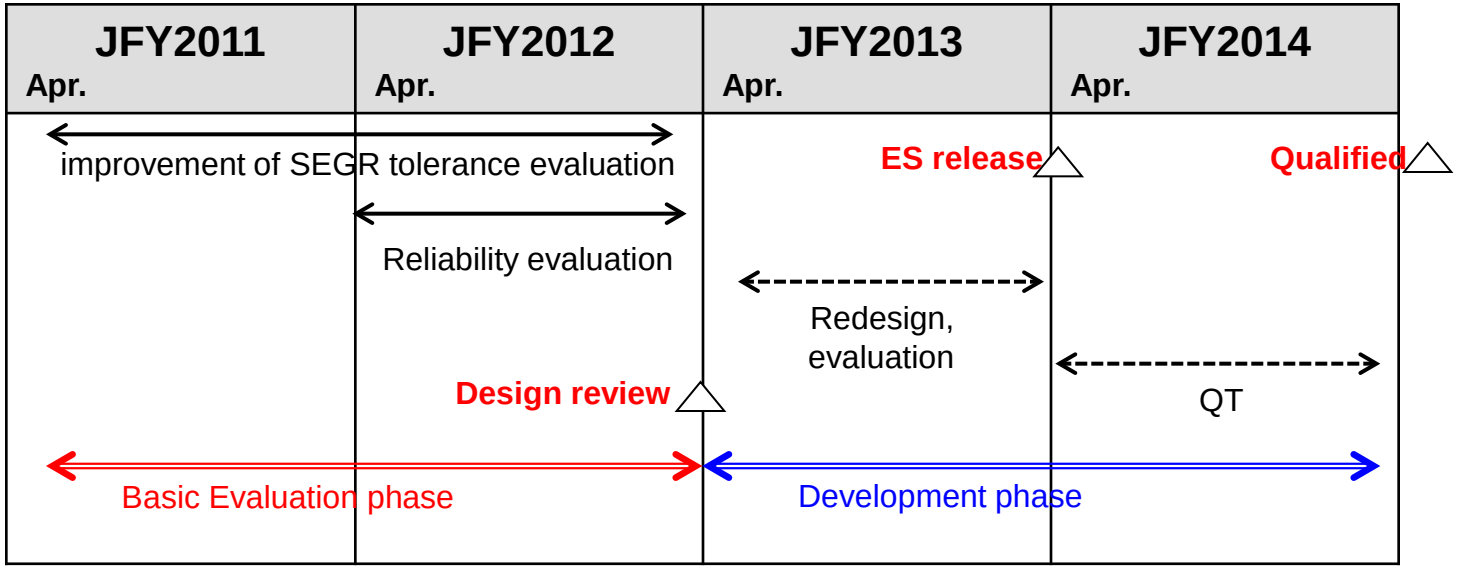
Commercial Technology
(Super-junction structure)



Past structure SJ structure

Development Schedule

- Basic characteristics will be evaluated until March 2013.
- Improvement of SEGR and ES device evaluation will be completed until the end of March 2013.
- Development phase will start after design review at the end of March 2013.
- Qualification will be completed by the end of March 2015.



Conclusion

The strategic parts are developed as follows;

- Development
  - 450k gate SOI-FPGA ：CNES-JAXA joint development

- Basic evaluation
  - SOI ASIC (include analog-digital mixed ASIC)
  - Power control H-IC
  - Next generation Power-MOSFET

These strategic parts will be applied to EPPL for European customer.

If European customers are interest in any of these parts, please contact JAXA. Specification could be adjusted by discussion between ESA and JAXA.


Thank you for your attention!!