ESCCON 2013

CNES activities status on EEE parts development

Michel Labrunée,
Jean Louis Venturin, Florence Malou, David Dangla, Jean Luc Roux,
Jean Paul Bussenot

Quality Assurance Sub Directorate Department CNES Toulouse, France

March 14th 2013

OUTLINE

- Introduction
- CNES Development program status
- AQP and MoQ in France
- Future challenges/ Conclusion

Introduction

CNES orientations

- Strong implication on **Space Components** (Development, Eval, Qual …)
  - è For all space projects,
  - è Strategic for Europe, independence, …
- **And**, on the use of **COTS components**
  - è Complementary approach (Myriades, Pleïades, …)
  - è with appropriate methodology already developed and under ECSS “standardization”
- **Harmonize** our activities through strong **cooperation** with:
  - è ESA, other European Agencies, Primes and manufacturers in the frame of **European Space Component Coordination (ESCC)**
  - è French primes and equipment makers within the **French Components Multi-partnership** for CNES programs (in particular for COTS components use)
  - è JAXA through the general **CNES JAXA collaboration** (FPGA’s co-development, Joint in flight radiation experiments, …)
- As far as we can, create synergies and partnerships between all space actors to **obtain a viable component supply chain**
  - è Product specifications, Design,
  - è Industrial processes (Front end, Assembly, Test, Product life time, obsolescence management, …)
  - è …
- **Improve the Competitiveness** of the space Industry (Component manufacturers, Equipment makers, Primes, …)

OUTLINE

- Introduction
- **CNES Development program**
  - **Objectives**
  - **Main activities**
- AQP and MoQ in France
- Future challenges
- Conclusion

Objectives of the CNES Development program

- To Develop key space components and contribute to the European effort on :
  - è Advanced Digital components (ATMEL, e2v, STm, Lfoundry,…)
    - » Sub micron CMOS technologies, ASIC's, FPGA, microcontrollers, processors, memories, high speed converters, …
  - è Standards components (STm, …)
    - » Fast logic IC 's, Converters, Linear, Transistors, diodes, …
  - è RF components (MMIC's, …) UMS, OMMIC, …
  - è Passive components (RED, Vishay, Eurofarad, …)
  - è …

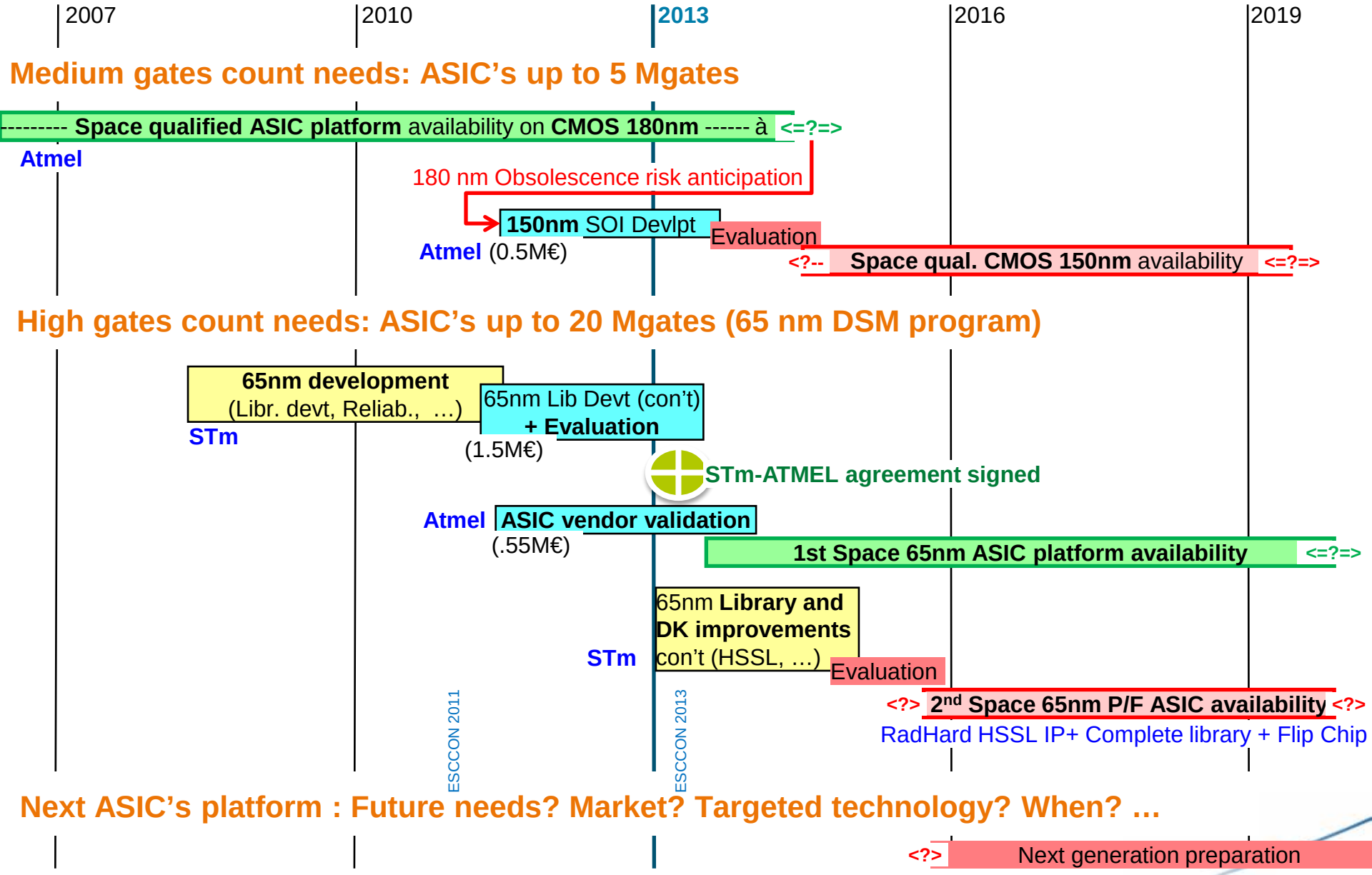
- Program harmonized through the ESCC/CTB and coordinated with ESA

- Budgets : Approx. 2.5M€ per year - CNES funding participation target : 50 %

- Only main activities are presented hereafter ("Roadmaps" form) :
  - è Digital ASIC's and FPGA's,
  - è High pin count packages,
  - è RF,
  - è Standard components,

*Notes : *The following slides are an update of the presentation done @ ESCCON 2011.*
**Detailed activity descriptions are given hereafter (See Back up slides section)*
**Passives activities of CNES are included within the presentation done by ESA on:*
"Passive component status and trends for Space applications"

Digital ASIC's

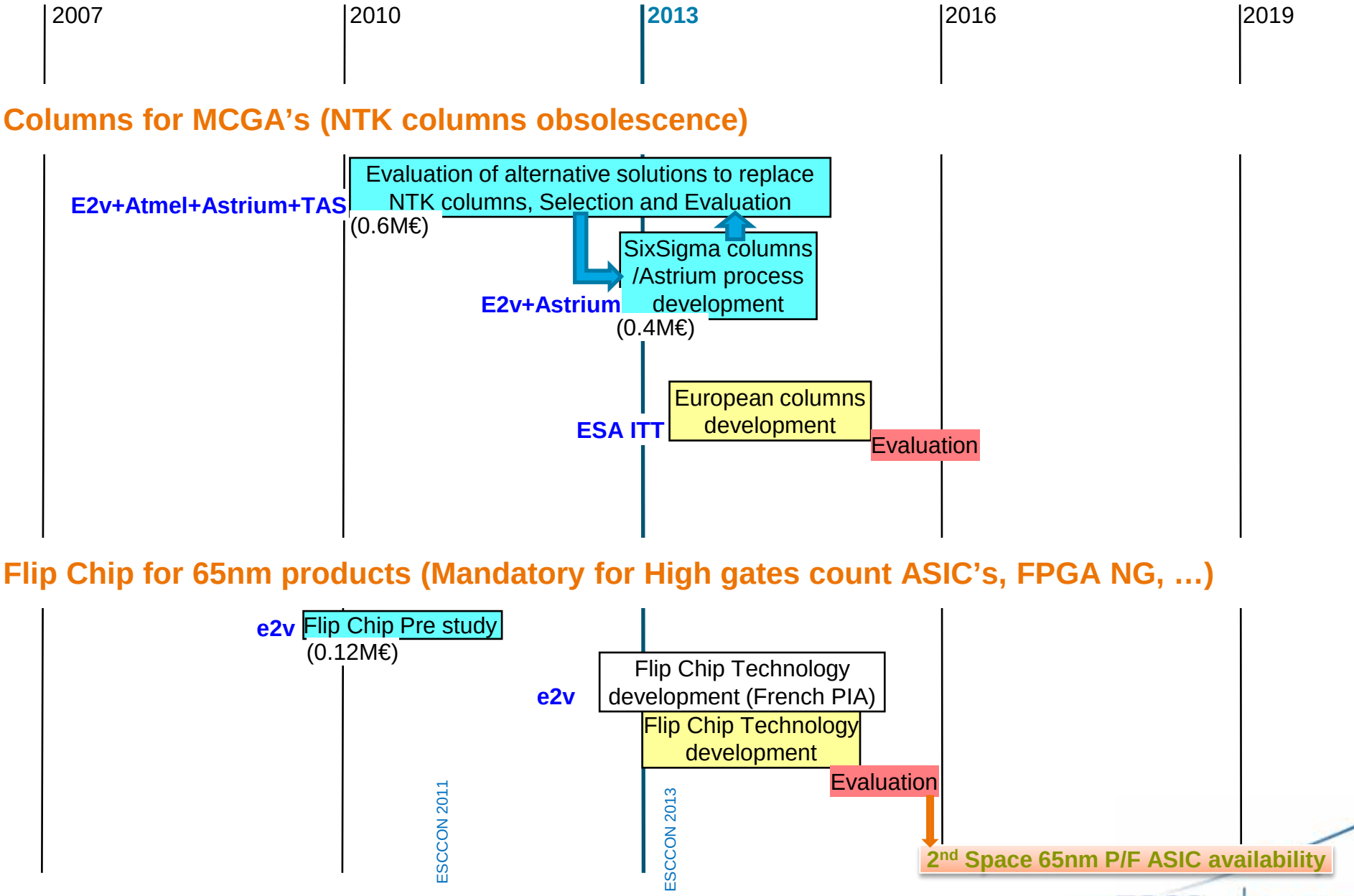


CNES	CNES/ESA
ESA	CNES/JAXA

Not yet funded

Budgets identified in () are CNES

High pin count packages

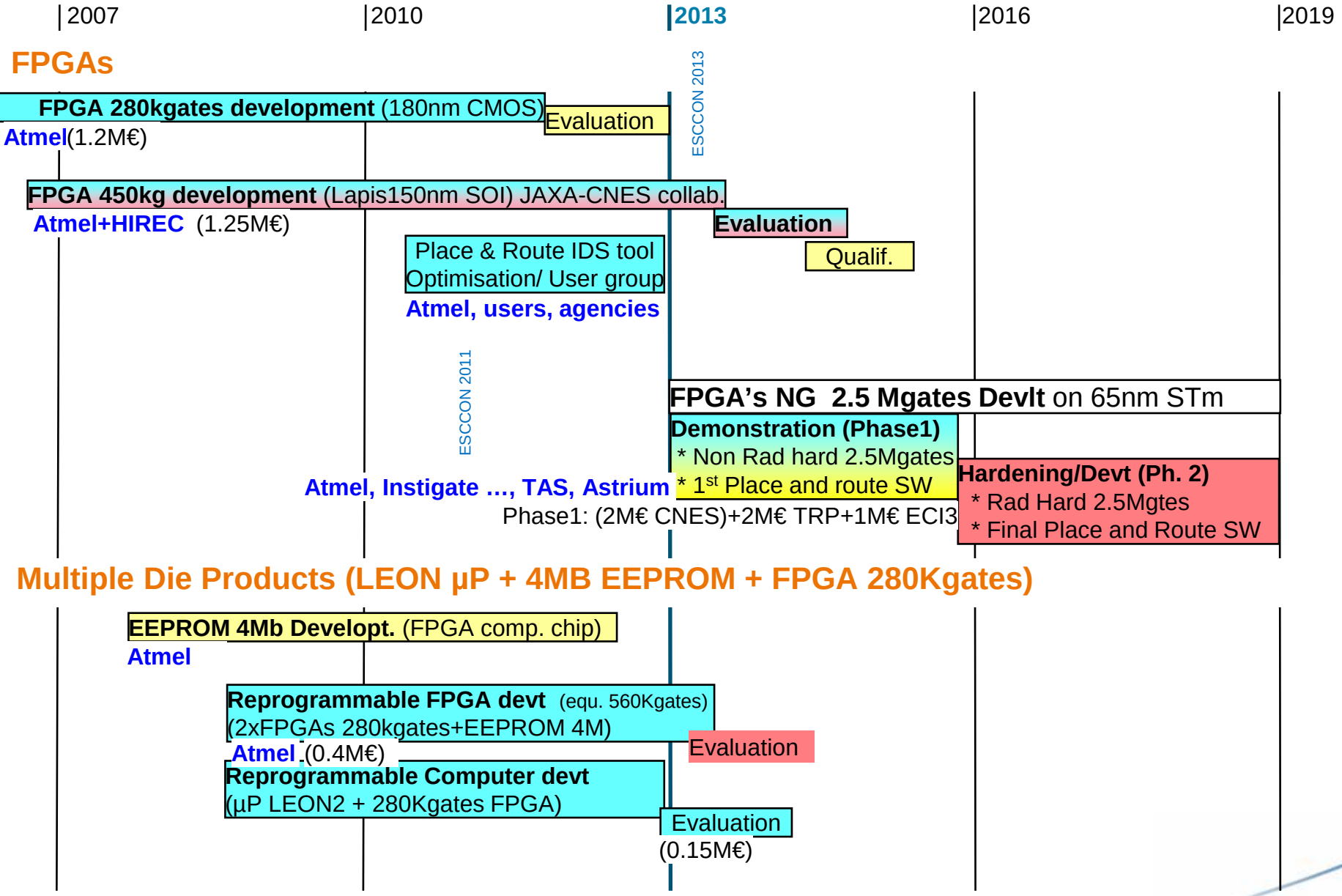


CNES	CNES/ESA
ESA	CNES/JAXA

Not yet funded

Budgets identified in () are CNES

FPGA's and associated products

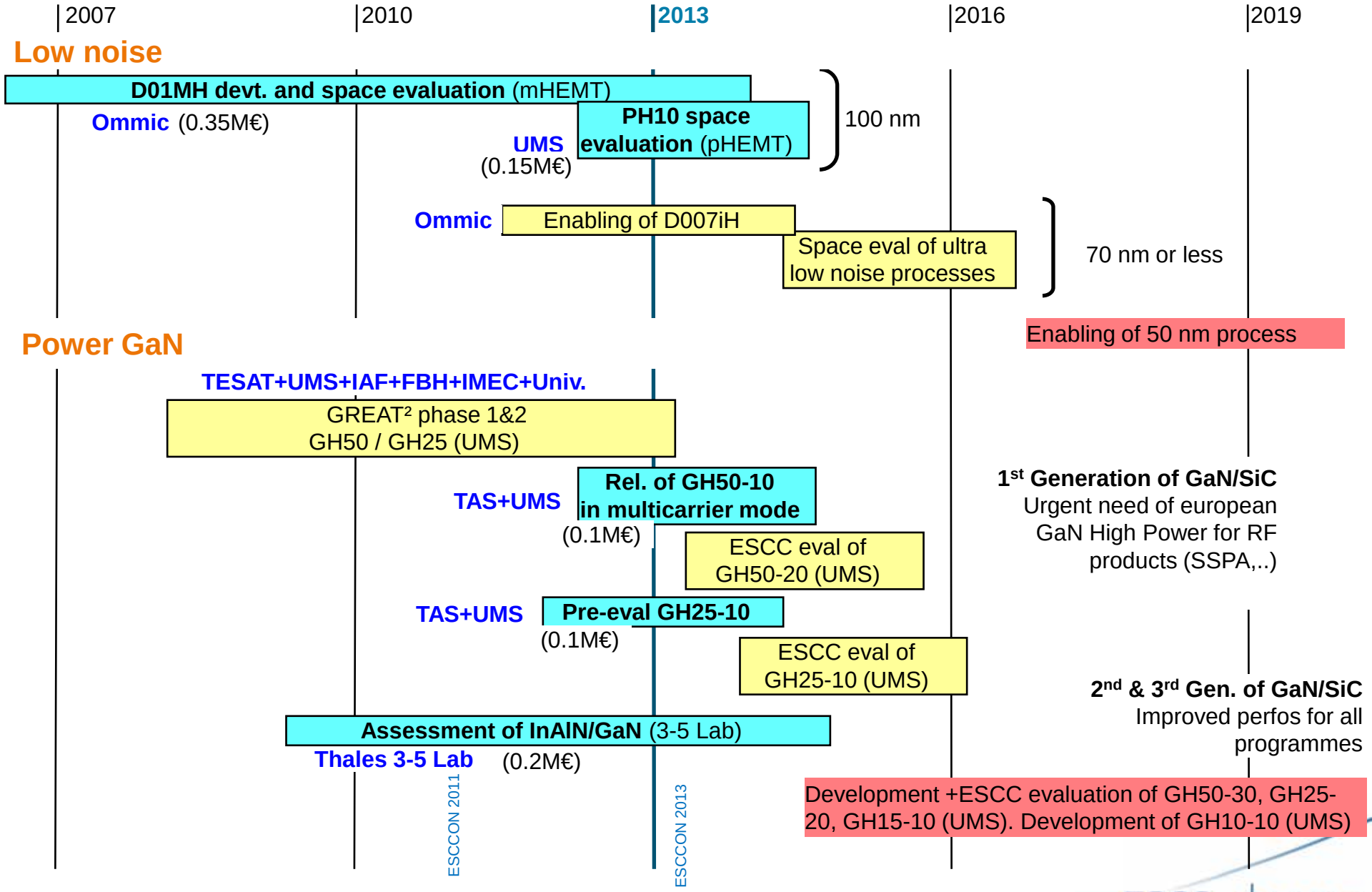


CNES	CNES/ESA
ESA	CNES/JAXA

Not yet funded

Budgets identified in () are CNES

RF

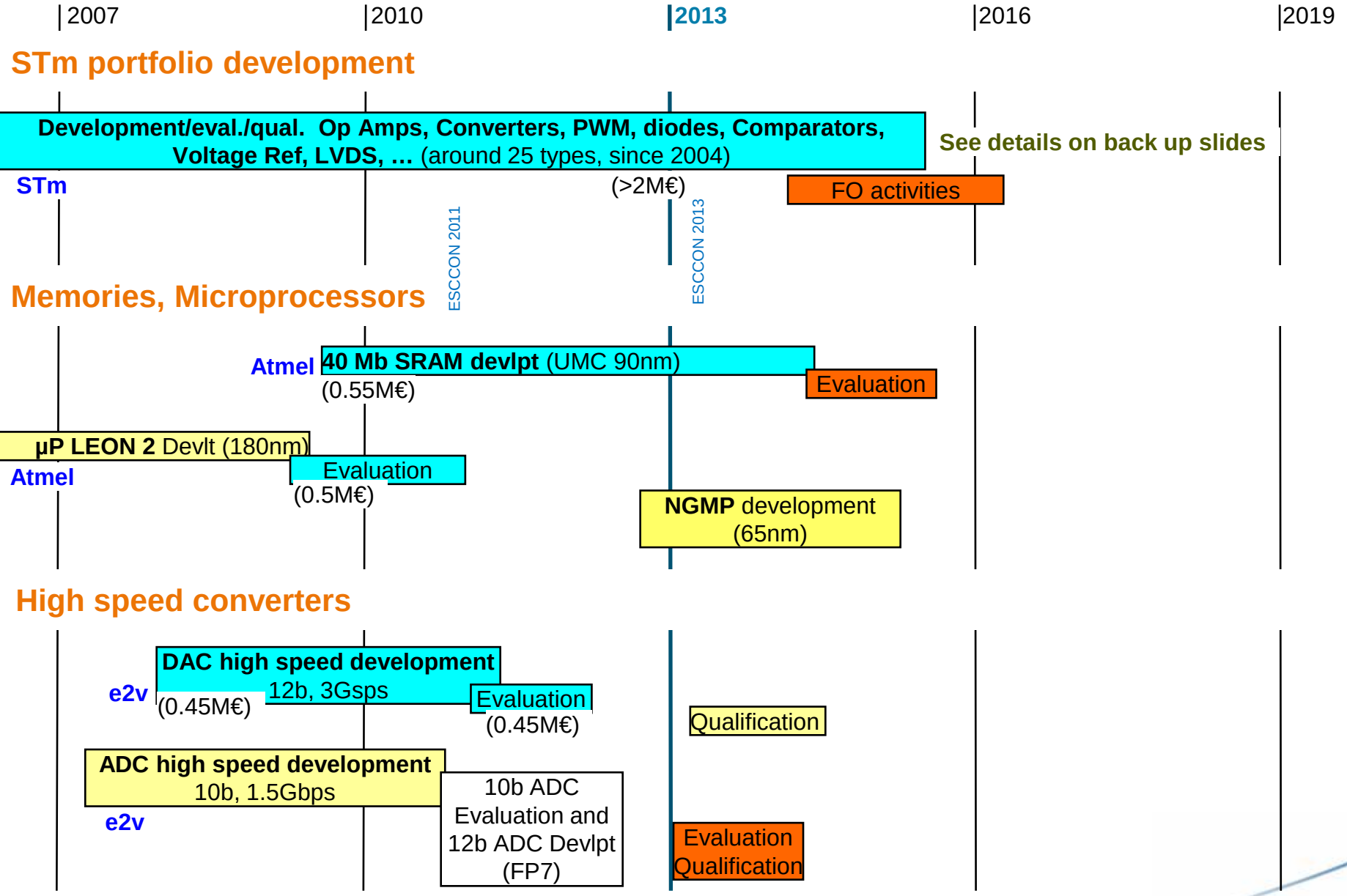


CNES	CNES/ESA
ESA	CNES/JAXA

Not yet funded

Budgets identified in () are CNES

Standards components



CNES	CNES/ESA
ESA	CNES/JAXA

Not yet funded

Budgets identified in () are CNES

OUTLINE

- Introduction
- CNES Development program status
- **AQP and MoQ in France**
- Future challenges/ Conclusion

Annual Qualification Program and Maintenance of Qualification in France

Strong implication of CNES on the ESCC Evaluations and Qualifications

- Participation and coordination with the ESCC Executive
- CNES experts are running the majority of the evaluations, qualifications and MoQ's activities in France :
  - è Around 15 components families covered (ASICs, FPGAs, Standard logic, Op Amps, Discretes, Passives, Connectors, RF, …)
  - è Around 20 French manufacturers covered,
  - è Around 100 components types/series under AQP and/or MoQ
- AQP and MoQ status done by CNES to ESCC bodies 3 to 4 times per year
- Details will be presented by ESA (see ESCC Executive presentation this afternoon)

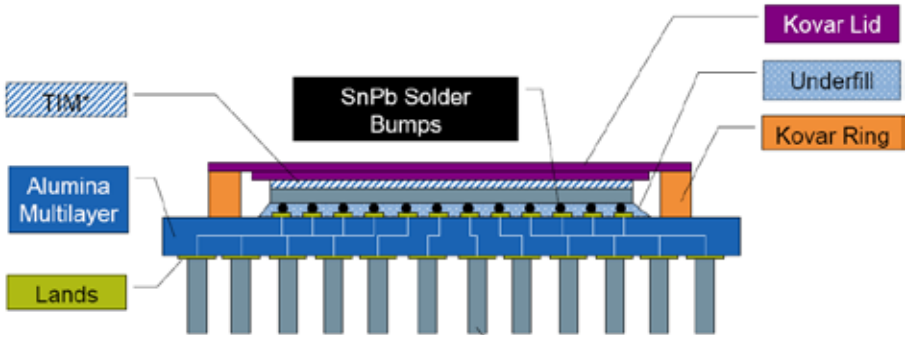
OUTLINE

- Introduction
- CNES Development program status
- AQP and MoQ in France
- **Future challenges/ Conclusion**

FUTURE CHALLENGES …

Flip-Chip package for space mandatory (2015-2016)

- **Limited time to develop and evaluate Flip-Chip capability for 65nm digital components & ASIC**
- **Evaluation/Qualification to be funded**



Reprogrammable FPGA NG (2.5 Mgates)

- **Very complex Hardware and Place and Route Software (Only Phase 1 funded)**
- **Big technical challenge for all space actors** (Manufacturer, End users, Agencies)

After 65nm :

- **Needs and market to be analysed asap,**
- **Process to be selected**
- **Radiation and Reliability capabilities versus space requirements to be assessed**
- **…**

FUTURE CHALLENGES …

GaN

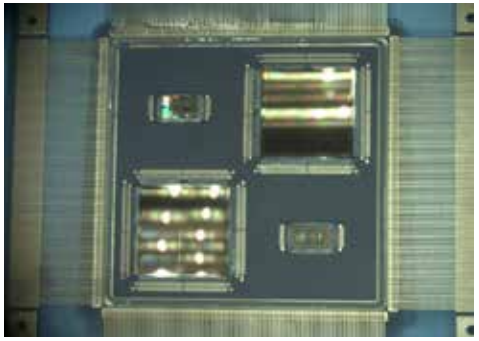
- **RF GaN : Validation of European SiC substrate and European GaN epitaxial wafer source**
- **Switching GaN components for power applications**
  - **Reliability,**
  - **Radiation tolerance,**
  - **Thermal management/Packages**
  - **Electrical signals control (very high Frequency, dV/dt, dI/dt)**
  - **Possible European source ?**
  - **Develop companion components (Drivers, Inductors, Capacitors, …)**

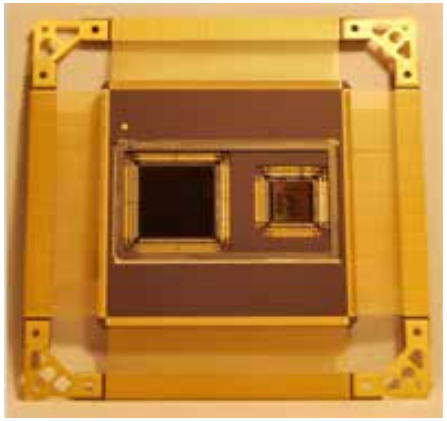
CONCLUSION

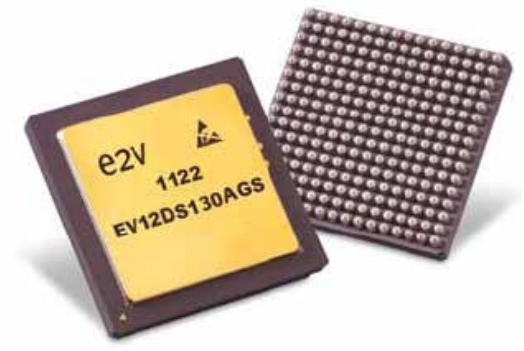
- Good collaboration/coordination (ESCC/CTB, CNES-ESA, CNES-JAXA, …)
- Very particular binding conjunction for the next 5 years :
  - Strong needs for New generation **ASIC's AND FPGA's** with **Flip Chip technology**
  - While **current standard ASICs platform (up to 5Mgates)** has to be secured
  - Next generations to be prepared: advanced digital components **(After 65nm), GaN, …**
  - **Current crisis** will certainly have major **impacts** on the sales and consequently on the private RandD activities
  - **Public RandD budgets too low** and not committed after 2015 (ECI 4 FO ? Horizon 2020?...)

- However, CNES is confident. Europe can take up the challenge
  - Major WW satellite/equipment makers need state of the art and competitive components,
  - Limited but viable space market with Involved manufacturers in Europe,
  - Back end capacities available,
  - European Strong expertise,
  - …

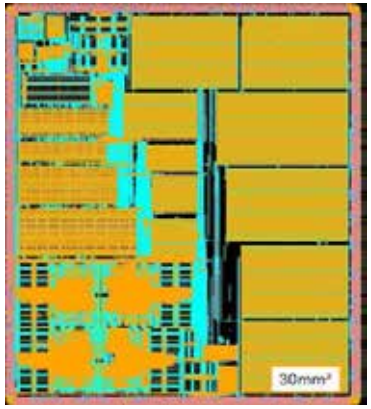
- To find at the European level the associated funding needs implies close coordination between Industry, ESA, National agencies and EU with common Roadmaps (FPGA NG is the first case to implement this scheme)

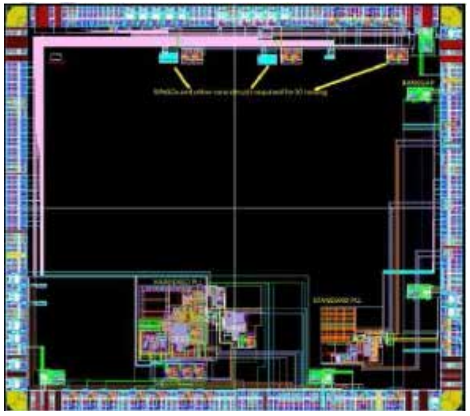


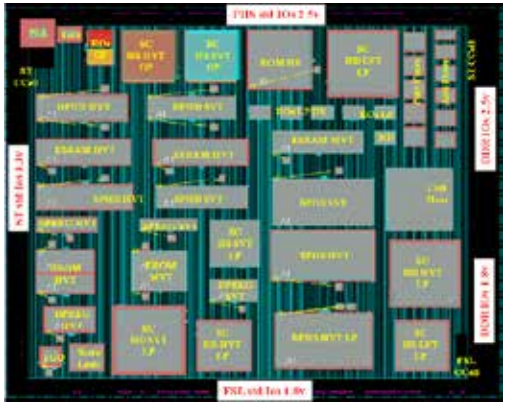




Thank you!!







Back up slides :

Main CNES activity descriptions

High gates count ASIC's from ATMEL / STMicroelectonics on CMOS065 LP process

Objectives :

- DSM technology is required for next generation flexible Telecom payloads :
  - Higher ASIC complexity : 20 to 30 Millions gates, Clock data path ≥ 400 MHz , Power dissipation per ASIC ≤ 15 Watts, HSSL 6.25 Gbps
- Process candidate : ST 65nm LP CMOS (F)
- ATMEL-ST agreement: ST will be technology provider and ATMEL will be the ASIC vendor

65nm Space platforms specification :

- **1st ASIC platform** (Q3/13):
  - Dedicated Libraries versus standard Design Platform 65nm
  - IO Libraries : I2C, CMOS IO and LVDS with cold spare feature
  - PLL
  - New Memories for SPACE+ BIST/ECC
  - Extension of boundary condition to support 20ys Life time
  - 100 krads
  - No SEL at 70meV/mg.cm², SEU hardened DFF's

+

- **2nd ASIC platform** (2015?):
  - Flip-Chip package
  - HSSL IP
  - PLL for Delay compensation
  - CAD Flow

Status :

- 1st ASIC offer design completed with systematic application of ST Design in Reliability (DiR) methodology focusing HCI and NBTI with dedicated tools for ageing simulations
- ESCC evaluation in progress by ST à end Q3/13
- In parallel ATMEL is initiating the 65nm ASIC offering with DK tools validation and design support to 1st telecom ASIC
- 2nd ASIC Platform preparation :
  - Flip Chip package development started (French funding + ESA funding)
  - CAD Flow, HSSL IP hardening (ESA funding) To be started soon.

Medium gates count ASIC's from ATMEL on 0.15µm SOI

Objectives:

- Manage near obsolescence of digital .35µ and .18µ digital technologies for "small" (500Kg-1Mg) and "medium" (5Mg) ASIC's needs
- Process candidate : LFoundry 0.15µm SOI (F)

0.15µm SOI offer specification :

- Digital radHard library
- 5V IO compatibility
- 1.8V Low voltage
- Processes with 3.3V I/Os logic devices
- PLL IP
- EEPROM blocks
- Analogl devices
- No Single Event Latch-Up below an LET Threshold of 80 MeV/mg/cm² at ambient & high temperature
- SEU hardened DFF's
- Tested up to 300 Krad (Si). Radiation Level is 100 KRads.

Status :

- Design completed
- Digital & Analog Test Vehicles available
- Electrical characterization, Radiation and reliability tests in progress
- Alpha tests by TAS: circuit with analog blocks under design

FPGA from ATMEL

ATF280F

- Main features :
  - SRAM-based FPGA
  - 280K equivalent ASIC gates
  - 14,400 cells (two 3-input LUT or one 4-input LUT, one DFF)
  - Unlimited reprogrammability
  - 300krads
  - No single event latch-up below a LET of 80 MeV/mg/cm2
  - SEE-hardened (Configuration RAM, FreeRAM, DFF, JTAG, I/O buffers)
  - RHBD no need for mitigation techniques during design
  - MQFP-256/352, MCGA-472, LGA-472
  - 0.18µm CMOS techno (F)

- Status:
  - Design completed
  - IDS Tools Release 9.1.2a available
  - ESCC evaluation tests completed under ESA contract. Data-Package & EPPL application to be issued by ATMEL
  - SMD number : 5962-12225

ATFS450E

- Joint ATMEL and HIREC development with CNES and JAXA respective support
- Based on the ATMEL AT40K FPGA architecture and HIREC radiation hardening by design techniques

- Target specification:
  - SEU/SET hardened SRAM based reprogrammable FPGA
  - 450K equivalent ASIC gates organized in an array of 152x152 core cells
  - SEE-hardened (Configuration RAM, FreeRAM, DFF, JTAG, I/O buffers) RHBD no need for mitigation techniques during design
  - 100krads
  - Lapis 0.15µm SOI (J)

- Status:
  - Design completed
  - 3rd silicon prototypes available
  - Some bugs have been discovered on configuration memory read-back. Feasibility of a silicon fix on-going
  - Reliability tests for Electro Migration and Stress Migration done on Lapis 0.15µm SOI

VLSI from ATMEL

LEON2 AT697F µP

- Dvlpt Supported by ESA and ESCC eval supported by CNES
- Main features :
  - è 32-BIT SPARC PROCESSOR
  - è 1 W at 100 MHz
  - è Fault Tolerance by Design
  - è 86 MIPS (Dhrystone 2.1)
  - è 23 MFLOPS (Whetstone)
  - è 300 krads
  - è SEU error rate better than 1 E-5 error/device/da
  - è No SEL below a LETth of 70 MeV.cm2/mg
  - è MQFP256 and LGA349 packages
  - è 0.18µm CMOS techno (F)
- Status :
  - è ESCC evaluation completed in November 2011 : All results are satisfactory
  - è ESCC Detail Specification No. 9512/004 approved
  - **à Product listed in EPPL**

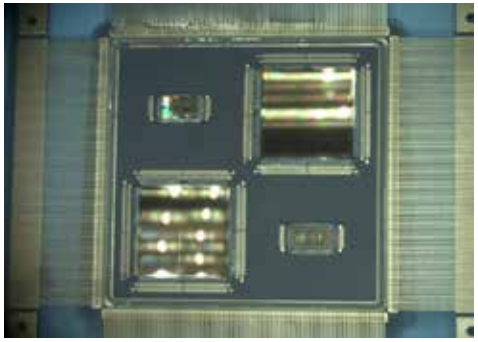
40Mb Asynchronous SRAM

- Target specification :
  - è 2 config : 4Mbx10b or 1Mbx40b with no embedded EDAC
  - è 2 options core: 1.2V std speed and 1.4V high speed. 3.3V IOs
  - è Packages: x10bit in FP42 (tbc), x40bit in CQFP132
  - è UMC 90nm Low Leakage CMOS technology (TW)
- Status :
  - è 1st silicon available (x40bit 1.2V version)
  - è Electrical characterization have shown some bugs at IOs level
  - è Design fix under investigation
  - è 2nd Si expected in Q1/14

VLSI modules from ATMEL

Reprogrammable FPGA module

2 FPGA ATF280F + 2 EEPROM AT69170E in one package

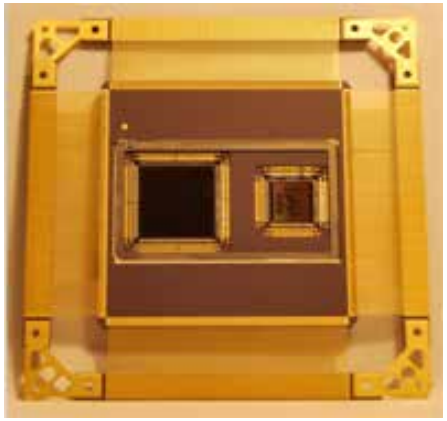


Atmel Reprogrammable FPGA module : open package

- Main features:
  - è 2x ATF280F FGPA + 2x AT69170E Configuration Memory
  - è MQFP352 package
  - è ATMEL 0.18µm CMOS techno (F)
- Status:
  - è Design completed
  - è Interconnections pbs between FPGAs
  - è Package re-design started
  - è New prototypes, Starter Kit, User guide and Application Note expected Q3/13

Reprogrammable Computer :

1 FPGA ATF280F + 1 LEON2 AT697F in one package



Atmel Reprogrammable computer : open package

- Main features:
  - è 32-bit SPARC V8 Reconfigurable with Embedded FPGA
  - è 90MIPS @SYSCLK=100Mz
  - è MQFP352 package
  - è ATMEL 0.18µm CMOS techno (F)
- Status:
  - è Design completed
  - è Electrical Characterization Completed à targeted spec reached
  - è Prototypes, Starter Kit, User guide and Application Note are available
  - è ESCC evaluation in progress à end Q3/13

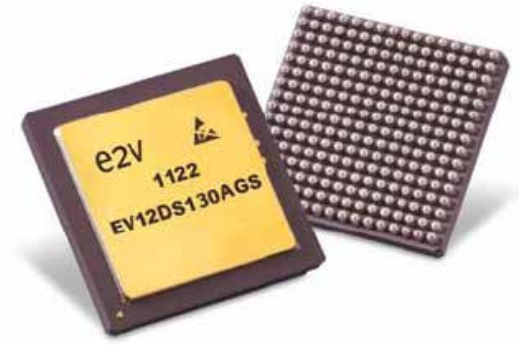
HIGH SPEED CONVERTERS from E2V

EV10AS180 ADC

- Dvlpt. in the frame of ESA program and ESCC eval in the frame of European Community's (CNES within FP7 consortium)

- ADC Main Features :
  - 10-bit resolution
  - 1.5 Gsps Conversion Rate
  - LBand
  - Selectable 1:1/2/4 DEMUX
  - 1.7 W Power Dissipation
  - 100 krads
  - CI-CGA255 Package
  - B7HF200 SiGeC techno. from Infineon (G)
- Status :
  - Design Completed à Reach target spec.
  - ESCC evaluation in progress

    à end Q1/13



EV12DS130 MUX-DAC

- Dvpt. and ESCC eval. in the frame of CNES program

- DAC Main Features :
  - 12-bit resolution
  - 3 Gsps Conversion rate
  - 6 GHz analog output bandwidth
  - 4:1 or 2:1 built in MUX (selectable)
  - 1.3 W Power Dissipation
  - NRZ, Narrow RTZ, 50% RTZ, RF modes
  - 100 krads
  - Ci-CGA255 Package
  - B7HF200 SiGeC techno. from Infineon (G)

- Status :
  - Design completed à Very good performances
  - ESCC evaluation completed in Sept.12 : very good reliability and radiation results

    à EPPL submission in Q1/13

STANDARD INTEGRATED CIRCUITS from STMicroelectronics / Completed activities

ADC	RHF1201	RHF1401
# bit	12	14
Fs	50 msps	30 Msps
V_{CC}	2.5V	2.5V
Power	100mW at 50Msps	85 mW at 20Msps
TID	300 krads	
SEL & SEFI	Immune up to 120 MeV-cm2/mg at 2.7 V and 125° C	
SEU / SET	SET immune for a LET ≤20MeV.cm²/mg SEU saturated cross-section = 3x10-4 cm²@ LET =60MeV.cm²/mg	SET immune for a LET≤ 116MeV.cm²/mg SEU saturated cross-section = 4x10-4cm²@ LET =116MeV.cm²/mg
Package	KSO48	
Techno	0.25µm CMOS	

VCHX	162244	162245	162373	162374
fonction	16-bit Bus Buffer	16-bit bus transceiver	16-bit D-type Latch	16-bit D-type Flip-Flop
TID	300 krads			
SEL	Immune up to 110 MeV-cm2/mg at 125° C			
SEU/SET		SET immune up to a LET of 110 MeV.cm²/mg		SEU saturated cross-section = 1.2x10-5cm²@ LET =110MeV.cm²/mg
Package	FP48			
Techno	0.35µm CMOS			

à Products listed in EPPL

STANDARD INTEGRATED CIRCUITS from STMicroelectronics / Completed activities

Op-amps	RHF43B Precision	RHF310 High-Speed	RHF330 High-Speed
V_{CC}	4 to 14V	4.5 to 5.5V	4.5 to 5.5V
I_{CC}	2.3mA	400µA	16.6mA
-3dB Bandwidth	2MHz, A_V=+5	120MHz, A_V=+2	1 GHz, A_V = +2
Slew Rate	2.85V/µs	115V/µs	1800 V/µs
TID	300 krads ELDRS free		
SEL	Immune at 125° C, LET up to 110MeV.cm2/mg		
SET	SET saturated cross-section ~ 2,5x10-3cm², LETth < 3.3 MeV/mg/cm²	- Immune in Inverting config. -Very low sensitivity in Non-Inverting config.(σsat ~ 1E-6cm²). -Low sensitivity in Subtracting config.(σsat ~ 1E-5cm²).	Low sensitivity in the three config.
Package	FP8		
Techno	Bipolar	0.25µm BiCMOS	

PWM	ST1843	ST1845
Duty cycle	100 %	50 %
V_{CC}	15V	
I_{CC}	17 mA max	
TID	50 krads	100 krads
SEL	Immune up to 120 MeV-cm²/mg at 30V, at 125° C	
SET	SET saturated cross-section = 1x10-2cm², LETth = 1.5 MeV/mg/cm²	SET saturated cross-section = 9x10-3cm², LETth = 1.5 MeV/mg/cm²
Package	FP8	
Techno	Bipolar	

Voltage regulator	RHFL4913
Output currents	2 and 3 A
Output voltages	2.5 V, 3.3 V, 5.0 V
TID	300Krads ELDRS free
SEL	Immune LET up to 110MeV.cm²/mg
SET	SET sensitive
Package	FP16, SMD.5, TO-257
Techno	Bipolar

à Products listed in EPPL

STANDARD INTEGRATED CIRCUITS from STMicroelectronics / Dvpt & ESCC Evaluation in progress

Fast Comparator

- Main features :
  - Propagation time of 5 ns
  - Rise/fall time: 1.4 ns on 10 pF
  - Low consumption: 1.4 mA
  - Single supply: 3 V to 5.5 V
  - FP8 package
  - ST 0.25µm BiCMOS techno (F)
- Status :
  - Design completed
  - Electrical Characterization Completed à Very good Electrical Results
  - Radiation Test in progress
  - ESCC evaluation in progress à end Q2/13.

Differential amplifier

- Target specification :
  - Slew rate: 780 V/µs min.
  - Input voltage noise: 2.8 nV/√ Hz
  - High input impedance
  - 4.5V to 5.5V operating power supply range
  - Rad-hard
- Status :
  - Design in progress on 0.25µm BiCMOS techno (F)
  - Si expected in Q4/13

Voltage reference

- Main features :
  - Reference voltage = 1.2V
  - High Precision: ± 0.1% @ 25 ° C
  - Low Tempco:< 30ppm/ ° C
  - FP10 package
  - ST 0.25µm BiCMOS techno (F)
- Status :
  - Design completed
  - Electrical Characterization Completed à Very good Electrical Results
  - Radiation Test in progress
  - ESCC evaluation in progress à end Q2/13.

16 bit DAC

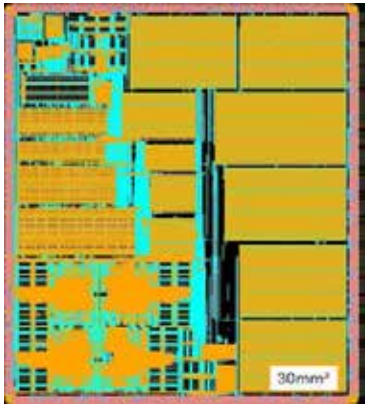
- Target specification :
  - 16-bit resolution at 5kHz bandwidth
  - 20-bit resolution at 250Hz bandwidth
  - 3.3 V analog supply
  - Rad-hard
- Status :
  - Design in progress on 0.13µm CMOS techno (F)
  - Si expected in Q1/13

Evaluation Test Programme of ST CMOS065LP

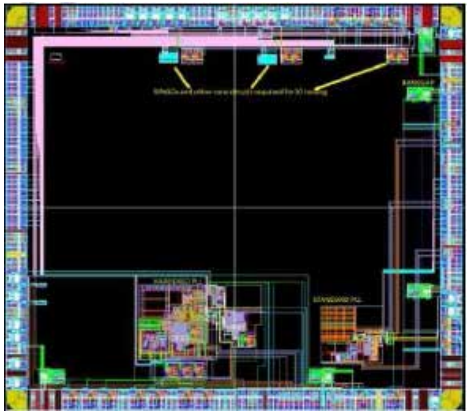
Evaluation Test Programme :

- **Representative Test chips manufacturing of the 65Space platform**
- **Electrical characterization of representative Test chips in -55°C/+125°C temperature range**
- **Construction analysis on TC1**
- **Reliability tests addressing NBTI and HCI to confirm life time of 20 years @ Tj=110°C with temperature & voltage accelerations on TC1, TC2 & TC4**
- **Radiation tests : TID, SEE under heavy ions and protons on TC1 and TC2**

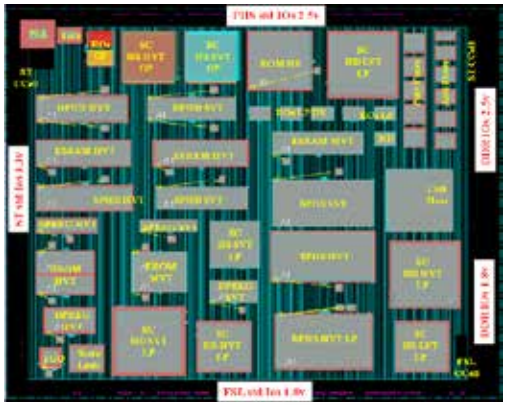
TC1 (Rad hard library):



TC2 (Rad-hard PLL + cold spare IOs)



TC4 (commercial library subset):



FPGA NG

Atmel 2.5Mg RH SRAM based FPGA :

- To Develop an High Reliability Radiation Hardened By Design SRAM based reprogrammable FPGA
- Process candidate: ST CMOS65LP (F)
- Architecture: NanoXplore

FRANCE GERMANY

- Target specification:
  - **SRAM-based FPGA**
  - **2.5M equivalent ASIC gates**
  - **324 clusters, 124'416 LUT**
  - **5'832Kb RAM**
  - **Unlimited reprogrammability**
  - **RHBD no need for mitigation techniques during design**
  - **Radiation performance:**
    - Heavy ions Latch Up susceptibility higher than a LET of 100 MeV/mg/cm² @ 85°C junction,
    - No configuration memory upset up to 100 MeV/mg/cm²
    - Heavy ion SEU and SET susceptibility higher than a LET of 40 MeV/mg/cm².
    - TID hardness successfully tested up to 300Krads
  - **Packages: FlipChip and Highly Dissipative Hermetic Ceramic Package up to 2000**

Instigate
Parallel Systems Development

- Status:
  - **CNES contract launched for the development of the first prototype.**
  - **Project duration: 27 months**
  - **Complementary ESA contracts for Hardware and Software will start soon**