

EEE Non-Dependence Presentation to ESCCON

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Why Non-Dependence?





The Technology Challenges



- Technology complexity/level of integration is continuously increasing, leading to higher cost of qualification and nonrecurring costs for ESA programmes.
- Supply chains are getting more complex, due to industrial outsourcing leading to supply chain interruptions for ESA programmes.
- Number of qualified technology providers for space is decreasing, due to limited space market and increased regulation/legislation (e.g. REACH, ITAR) leading to increased cost of technology qualification for ESA programmes.
- Trend for recurring equipment is increasing; emphasising the need to manage medium/long term obsolescence.
- Technology gaps that have previously existed (Europe/USA/Asia) can be reduced (e.g. GaN, Deep Sub Micron (<65nm)), but they still exist.







Timeline from R&D to Commercialization





Examples of qualified products in service:

AVX Type 1 capacitors since 1983, Infineon CFY66/67 GaAs HEMT since 1994....

European Space Agency

European Components Initiative : Non dependence



ECI Phase 1 (2004-2010) Addressing the growing ITAR concerns through European alternatives ECI Phase 2 (2009-2012) Providing competitive alternatives (cost and time to market)



e Agency

Source of EEE parts in typical European commercial satellite





Value-Chain





- European Component
 Initiative supports
 components suppliers
 who are at the base of the
 value chain
- These suppliers work for equipment suppliers (including several small and medium enterprises across ESA Members States)

Required key technologies (2013-2020)

- Space qualified supply chain for 65nm Deep SubMicron ASIC technology
 - ADC/DAC, Flip-chips, high pin count packaging.
- Space qualified Rad hard Large re-programmable European FPGA
- European space qualified Gallium Nitride (GaN) supply chain
- Space qualification of European Mixed Signal ASIC technology
- Extended range of **advanced VLSI** products
 - DC-DC Converters, MOSFETS, Pulse Width Modulators, Line drivers etc....
- Next Generation general purpose Micro-Processor (NGMP)
- Next Generation **Digital Signal Processor (DSP)**
- European high performance CMOS image sensor technology supply chain
- Space qualified European **RF MEMS process**.











Deep Sub Micron (DSM)

Why:

 The lack of space qualified DSM (65nm) technologies in Europe is leading to performance limitations and increasing the procurement risks for navigation/ telecommunication satellite applications.

Criticality:

 European space primes require unrestricted access to space qualified advanced digital technologies (ITAR free) to compete in the digital telecom payload market.

Objective by 2015:

- To develop and maintain a supply of space qualified advanced digital technologies based on the 65nm process starting with:
 - DSM radiation-hardened ASIC libraries.
 - High speed serial links (HSSLs) between components.

Achievements:

- Feasibility, ASIC library definition and first 65nm (STMicroelectronics) test vehicles completed in the context of KIPSAT Phase 1.
- ASIC library consolidation and release to 1st alpha customers in KIPSAT Phase 2 (TRP, ECI 3, GSTP funding) and LibEval (CNES).

What still needs to be done:

- ESCC Qualification of the 65nm Process and associated product lines (HSSL) (No funding identified).
- Note : Parallel development of flip chip high pin count packages is required for many devices such as telecom ASICs, NG FPGA, Microprocessor and DSP that rely as well on DSM.



100%





Radiation Hard FPGA (Field Programmable Gate Array)

Why :

- FPGAs offer shorter development times ,simpler, less expensive design and manufacturing phases than Application Specific Integrated Circuits (ASICs).
- Almost 100% of high performance FPGAs are ITAR controlled devices (Microsemi, XILINX).

Criticality:

FPGAs are required in all electronic units offering digital functionality across ESA missions in Science, Exploration, Earth Observation, Telecom and Navigation. (Identified on the EC-ESA-EDA Urgent Action List)

Objective by 2017:

• Development and qualification of a European product line of radiation hard FPGAs without export restrictions.

Achievements:

- European space qualified low gate capacity (40K, 280K) FPGAs. (CNES, ECI 3) •
- Development and qualification of a European medium gate capacity FPGAs (450Kgate) on SOI process (rad hard by nature), (CNES, ECI 3).
- Development started (2013) on a Large FPGA prototype with increased logic capacity and performance.(>2Mgate) (TRP, ECI 3, CNES).

What still needs to be done:

- ESCC space qualification 450Kgate FPGA (funding established in ECI 3).
- Rad hard design of the large FPGA and ESCC qualification (no funding identified).

TRL 9

TRL 8

TRL 7

TRL 2

TRL 1

System Test, Launch

System/Subsystem Development

& Operations

Technolo

Technology Development

Research to Prove Fe sibility

Basic Technology Research

AIMEL

Flip Chip & High Pin Count Technology (Requirement for DSM & FPGA)

Why:

 Both Flip chips and High Pin mounting solutions are required to package and mount the developing DSM and FPGA technologies. (Navigation/ Telecoms/ Science/Earth observation)

Criticality:

 Essential requirement to achieve all possible benefits from European DSM and large FPGA qualified processes.

Objective by 2015/16:

 Provide a qualified packaging and mounting solution for high pin count

Achievements:

- Identification of technical requirements and limitations (TRP, CNES, Industry).
- Contracts launched in 2012 for key critical developments (ECI 3 /4 Funding).

What still needs to be done:

- Completion of development activities (funding ECI 3 established).
- Proving of technology developments and ultimate qualification of packaging and mounting technologies (no funding identified).



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Gallium Nitride (GaN)

Why:

 GaN component technology offers disruptive performance capability for microwave payloads (Science, Telecoms, navigation, Earth Observation) and improved efficiency for operation in harsh environments (high temperature, radiation robustness).

Criticality:

 To avoid future dependence upon export restricted GaN processes . (Identified on the EC-ESA-EDA Urgent Action List).

Objective by 2016:

 To develop a European Supply chain for space qualified GaN component technology. Focusing on RF+microwave and then development into other critical areas such as DC-DC power conversion transistors.

Achievements:

- GREAT² Failure mechanisms identified and reliability improvements demonstrated.
- First European GaN demonstration: PROBA V transmitter IOD (TRP/ ECI/ GSTP).
- Foundry (UMS) process qualification completed and released for commercial applications (2 years earlier than planned) (GSTP).
- Established a commercial GaN epitaxy production facility in Europe (GSTP).

What still needs to be done:

- Space evaluation of UMS GH50 (ECI 4 funding).
- Space evaluation of GH25 processes (no funding identified).
- Development and qualification of Power GaN product lines (GSTP funding discussions on going).





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Mixed Signal

Why:

- Integration of diverse ("mixed") signal interfaces into single device solutions, is an essential contributor to the overall system miniaturization and performance increase (Earth Observation, Science and exploration, Telecoms, Navigation).
- Single device mixed signal solutions improve the total functionality, performance, weight, volume and power consumption.

Criticality:

 Very heterogenic subject due the large spread of end user requirements, resulting in the need to harmonise on a limited number of space qualified mixed signal processes. (Identified on the EC-ESA-EDA Urgent Action List)

Objective by 2015/16:

• Qualification of European mixed signal technology process for Space Applications to enable the development of new products (RF, Power, Telemetry, System on Chip...).

Achievements:

- Multiple European foundries already supplying mixed-signal ASICs for space: AMS(A), X-FAB(UK,D), Infineon(D), IHP (D), ON-Semi(B), ATMEL(F).
- Mixed signal process evaluations on going with ATMEL (CNES funding) and IHP (ECI 3),

What still needs to be done:

 ECSS qualification of a European mixed signal ASIC process (start late 2014) (no funding identified).

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Digital Signal Processor (DSP)

Why:

• High Performance Digital Signal Processors are more power efficient, and offer higher performance for signal processing, and real-time applications than general purpose processors (Earth Observation, Science and Exploration).

Criticality:

 The only existing European DSP is now completely out-dated, it provides less than 6% of the performance required today, consequently Europe is currently reliant upon using a combination of FPGAs from USA (ITAR) and US sourced COTS components with limited reliability and significant added mass / complexity / power consumption.

Objective by 2016:

 Development and Commercialization as a standard ASIC product (DSM process) of a space qualified rad-hard Digital Signal Processor with a performance of at least 1000 MFLOPS.

Achievements:

- European DSP tradeoff and definition study completed in 2012 (TRP)
- Low maturity R&D activity on floating point DSP IP on going (FP7)

What still needs to be done:

- Feasibility and design adaptation of the commercial IP (proposed to be launched under ECI phase 4).
- Engineering prototypes, flight models, and ASSP qualification and product commercialization (no funding identified).



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FUNDING



CMOS Image Sensor (CIS) Technology

Why:

- CMOS Image Sensors (CIS) are incorporated in most satellite for various functions.
 Science and Earth Observation satellite have CIS as their main core payload for observations.
- CIS will eventually replace CCDs and is already the preferred solution for its low noise, high level of integration, and radiation hardening.

Criticality:

• There is no Europe solution for a complete CMOS detector supply chain.

Objective by 2016:

 Through the EuroCIS, the objective is to develop a European end-to-end supply chain for image sensor.

Achievements:

- Phase 1 of the EuroCIS, (TRP) has been initiated with IMEC (B) and ESPROS (CH) to cov high flux applications (Earth Observation).
- Low flux (Science) activity (TRP) will be kicked off during 2013.

What still needs to be done:

- The second phase of EuroCIS covering the required enhanced technology features (no funding identified).
- ESCC space evaluation of complete working CMOS image sensor (no funding identified)







Micro Electro Mechanical Systems (MEMS)

Why:

 MEMS have extremely low mass and volume, low power consumption and allow the tight integration with other electronics. MEMS sensors ,switches and actuators can be used to reduce the size and mass of telecommunication, earth observation, navigation, launcher and science applications without sacrificing functionality.

Criticality :

 USA is already leading the development of MEMS for space applications (export restrictions apply). Although some European developments and testing activities have started, they lack the critical numbers (both volume and budget) to achieve a sufficient improvement on key issues, such as the reliability, understanding of failure modes and the development of packaging solutions.

Objective by 2017:

- Increased availability of space compatible European MEMS devices (RF, Gyros, Accelerometers, MOEMS, Pressure Sensors).
- Develop a standardization methodology and set of standards for reliability assessment of MEMS products.

Achievements:

• Project qualification of MEMS: Gyros (S3), Microshutters (JWST), Flow Sensors (GAIA)

What still needs to be done:

- Reliability evaluation and testing of MEMS devices (IMUs, RF Switches, Micro Mirrors Arrays, Magnotmeters, Interferometers) (Partly funded TRP, GSTP, ECI)
- MEMS Packaging, stacking and integration (No funding identified)
- Preparation of an ECSS standard on MEMS reliability. (Funding identified ECI)

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CID



Summary/ Messages (1/2)



- Developments are driven by component availability, their performance and reliability. Either we have the capabilities within Europe or we must look and spend elsewhere.
- European Non Dependence provides significant benefits for European designers, Component manufacturers, Equipment providers (often SMEs) and System integrators.
- **Time to market is critical**. Europe need to stay ahead of the competition by providing access to technologies free of any export restrictions, when it is required and at an affordable price.
- All ESA satellite programs require access to the on going key technologies covered in this presentation.
- Need to start looking further ahead, anticipate the future needs/requirements of the business, as well as, the problems arising from obsolescence issues (REACH/ RoHs), and the ability to manage the supply chain.

Summary/ Messages (2/2)



- Either invest the money within Europe or it must be spent outside of the ESA member states (USA/Asia) for the high value components and key technologies.
- Through current European strategic activities (TRP/ECI/GSTP/ARTES/NSA/EDA/EU), the technology gaps between Europe/USA/Asia can be reduced through investment with European suppliers (but technology gap still exist !).
- The required European components and technologies are well defined and agreed by ESA, National Space Agencies, Component suppliers, equipment providers and End users for the next 5-7 years.
- The ECI is funded only up to the end of 2015 and at a lower level than required to maintain and develop technical capabilities. The shortfall to complete the existing technology roadmaps is approx. 10M€ per annum.
- The Governments of the major space nations outside of EU are investing on EEE technologies to maintain access to key capabilities. Institutional investment within Europe must also continue to maintain European access to space.