STUDY REPORT

Utilisation of Pulsed Laser for SEE testing

BACK IRRADIATION

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ABSTRACT

This report presents the results of a study on the feasibility of irradiating a silicon Integrated Circuit from the die back side with an IR picosecond pulsed laser.
64M-bit SDRAM memories in TSOP packages have been considered and single events were triggered in the memory array. Minimum beam diameter achieved was about 1.7µm and multiple upsets were detected for each hit.

Data processing allowed to correlate the logical address of the words in error and the hit coordinates.

Main difficulty found was with the IR visualisation of the front side of the chip to allow for focusing the laser beam in the sensitive region. A more appropriate IR camera such that a InGaAs CCD camera would be needed for conducting routine evaluation work.
In the same way, the use of industrial picosecond pulsed laser with sable accurate pulses would allow the implementation of a test bench, which could be made available to the space users community.

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1 INTRODUCTION

This work was performed under ESA CALL-OFF ORDER NUMBER 03 ESTEC/CONTRACT No. 13528/99/NL/MV.

Hirex Engineering already acquired some experience in SEE simulation with a picosecond pulsed laser.
In a previous work, an SRAM memory was analysed with this technique using front side irradiation. The sensitive regions inside a memory cell were identified and the physical mapping of the entire memory retrieved, thanks to the error data processing (correlation between hit coordinates and logical addresses).
In addition, Hirex Engineering also heavy ions tested 64M-bit SDRAM devices using backside irradiation. This required a specific sample preparation technique, which consists of thinning the device (including the die) down to a thickness compatible with the penetration depth of available heavy ions at our accelerators. Available ions often have a penetration range in silicon of about 100µm.

The presence of multiple metal layers on top of the active surface of state of the art VLSI devices has been identified as a limit to front side laser irradiation. Furthermore device assemblies such as flip chip construction or Lead On Chip (LOC) construction do not allow for accessing the device from the front side.

On the contrary, these obstructions are avoided when using backside irradiation.

The purpose of this work was then to assess the feasibility of triggering single event upsets using a backside irradiation technique with a picosecond pulse laser.

2 PRELIMINARY DISCUSSION

2.1 Back irradiation advantages

The interest of the Laser Irradiation Technique (LIT) is that the beam wavelength can be adjusted in the near infrared to limit the absorption in the substrate and to excite the cells circuits integrated on the active side.
The associated constraints are :
Backside of the device should have an optical polish prepared prior to the irradiation.
Test bench need to be equipped with an infrared camera and an infrared source to allow for spatial positioning.
Another basic advantage of this technique, is that, thank to the good optical quality of the back surface of the polished test sample, laser beam will not be reflected nor diffracted by any metal track at the back side level. One also need to keep in mind that new devices will have more and more metal layers (up to 10) on top of the active side. In addition, passivation surface irregularities on top of the die do not play any role in laser beam transmission.

2.2 Potential limitations

Using the laser pulse irradiation through the back plane set up several new problems with respect to the usual front irradiation technique:

1. The substrate surface must be optically polished with a typical quality of λ/8. This is a complicated step in respect to the front irradiation method. However, a big advantage is that the metal layers on top of the die, will no more limit the access to the active areas of the circuit as it is excited through the back plane.
2. Obviously the laser beam is absorbed by the substrate introducing an attenuation factor exp(-αL) where L is the substrate thickness and α the beam absorption coefficient at the operation wavelength. Thus, if Φ_0 is the incident flux necessary to generate a SEU in a front irradiation, the corresponding energy in a back irradiation will be (at least) $e^{\alpha L}\Phi_0$. As a result, the operation wavelength must be chosen to operate with a small coefficient. Laser irradiation around 600 nm

is excluded. A first possible choice would be around 1030-1060 nm, i.e., with mode-locked YAG lasers. In that case, α=10-15/cm in Silicon, L=0.06 cm so that $0.6<\alpha L<1$, thus an increase of the excitation energy will be increased by a factor of 3. We must stress that this estimation of α is based on the assumption that the circuit substrate is not heavily doped. This point would have to be checked. Concerning the front surface energy threshold Φ_0, there is an astonishing dispersion of results in the SEU laser testing literature. We then follow the results, which conclude, the excitation energies in reasonable agreement with what is expected from the operation conditions of integrated circuits. The upset threshold occurs using 2-25 pJ pulses at 1064 nm, with duration of 30 ps. Thus we estimate that the same effect is expected in the back irradiation using typically 0.1-1nJ pulses.

3. The beam waist diameter (i.e., the smallest diameter of the focussed beam) will be slightly larger in the back than in the front irradiation. The reason is that in the case of front irradiation, the microscope beam is focused onto the circuit surface. The beam waist diameter is that one achieved in the air, which depends on the objective numerical aperture. In the case of the back irradiation, the beam waist is that one attained in a material with an index n=3.5. For instance, for a beam with a numerical aperture NA=0.6, the beam waist radius is ω_0=0.42µm in this air and 0.53µm in Silicon. Thus the spatial resolution is slightly degraded.
4. The layout of the Integrated circuit will not be visible with standard visualization tools. Two consequences follow: A) Identifying the zone irradiated by the laser beam will become really difficult, although not impossible; B) It will be difficult to accurately focus the laser beam on the zones under investigation. Thus, the solution will consist of integrating new infrared visualization in the existing set-up (around 1.3 or 1.5µm for instance) to observe the ICs through the silicon substrate. However, this procedure might be more or less disturbed by the reflection (R≈30%) of the polished substrate. Thus some tests are necessary. In the worst case (which however is unlikely), it will be necessary to deposit an antireflection coating on the polished substrate of the chip.

3 TEST PLAN

The previous paragraph shows that several issues must be investigated to validate the new proposed experimental procedure, namely:

- The procedure to polish-in situ the back side of the substrate must be demonstrated
- The wavelength of the excitation must be studied. Although, experiments at 1.064 mm with a mode-locked YAG laser are expected to be successful, this is not demonstrated particularly if the substrate is doped. If the operation at 1.064 µm is not satisfactory, pulses emitted at longer wavelength with an optical parametric oscillator would have to be used.
- The incident energy to attain the SEU threshold energy is not known, and depends of the absorption in the substrate.
- The infrared visualization system must be defined, constructed and integrated in a test bench microscope. The possible perturbation of the polished back-side reflectivity must be measured.

In this context the work plan is the following:

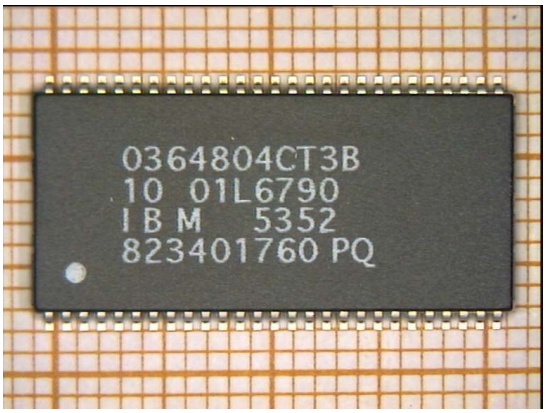
- Improvement of laser test bench and validation
- Selection of the test vehicle (flipped chip or device with a lead frame on top of active side) with available data from previous heavy ion tests
- Preparation of the sample (optical polishing)
- Validation of the test method

4 Devices under Test

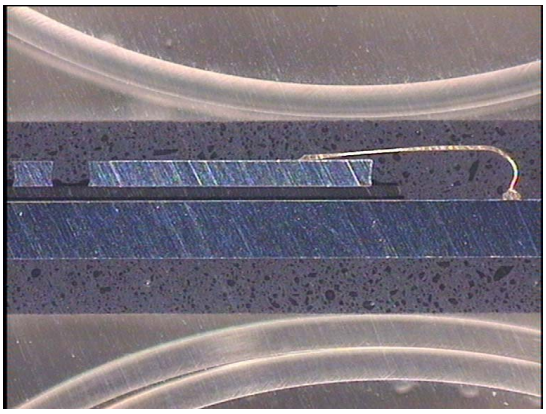
The following SDRAM types were selected for this study;

Manufacturer	Type	Organization
IBM	0364164CT3B	2Mbit x 8 x 4
SAMSUNG	KM416S4030CT-G8	1Mbit x 16 x 4

In parallel and for technology support, two IBM samples were provided to ESA for NMRC to perform Construction Analysis (Constructional Analysis- IBM 0364804CT3B, Report Number DTE 1147).

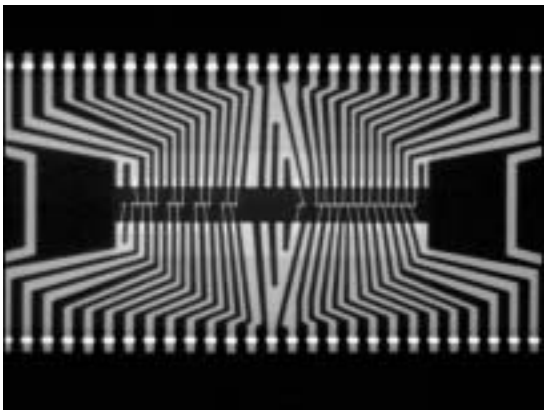


IBM 64 M-bit SDRAM in TSOP package



Lead On Chip Construction

In this micro sectioned view of a TSOP package device; central bonding can be observed with the lead frame on top of the active side



I IBM 64 M-bit SDRAM

This X-Ray photo shows the overall view of the lead frame together with the bonding wires.

Figure 1 – 64M-bit SDRAM from IBM

4.1 Samples preparation

The main reason for selecting these devices is because their construction is of LOC type and because Hirex Engineering already performed a heavy ion testing on mechanical thinned samples. These samples were thinned from the back down to a die thickness of less than 100µm.

For the laser study, two test samples of each type have been prepared using this technique.

For each type, one device was thinned down to less than 100µm while the second sample was left with the original die thickness of about 300µm.

Then as a final step, required for the laser study, consisted in submitting these samples to an optical polishing finish using various grades of micro abrasive alumina powders.
A visual criterion was used to determine the quality of the polished surface (mirror like)

5 HIREX /LAAS LASER TEST BENCH:

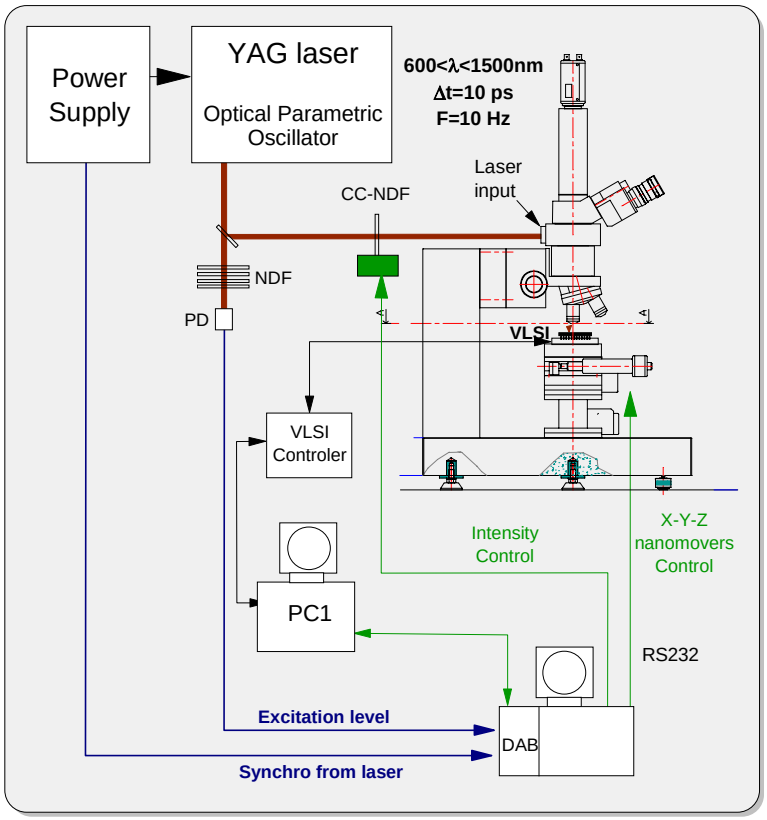
Main characteristics of the system are presented here below.

- Laser source: Mode-locked YAG laser pumping an Optical Parametric Oscillator
  Repetition rate: 10 Hz.
  Excitation wavelength: adjustable from 0.7 à 2.3 µm.
  Pulse duration: 10 ps
  Pulse Energy E: 0.1 µJ<E<50µJ
  Energy Measurement Accuracy: ~10%
- Optical subsystem:
  Focus control by Z adjustment: (0.1 µm)
  Spot diameter: 0.8 µm (at 1/e2)
  Energy adjustment by a two-decade attenuator
- Positioning:
  Minimum horizontal step: 0.1 µm
  Computer-controlled movements
  Minimum movement time between two points separated by 200 µm: 0.1 s

The overall laser test set-up is shown in Figure 2. Main elements are :

- The Yag Laser which pumps the Optical Parametric Oscillator. The power supply of the laser generates a synchronization signal, which is the temporal reference of the whole system. The repetition rate is that of the YAG laser pulse emission, namely 10 Hz.
- The microscope and the XYZ positioning system. Figure 2 shows an exact representation of the final integration of the microscope head with the nanoactuators.
- The photodiode (PD) to measure the energy of the pulses emitted by the Optical Parametric Oscillator (OPO).

This workbench is fully compatible (in terms of electronic and mechanical interface) with the standard heavy-ion test equipment of HIREX with the only limitation on the acquisition cycle, which cannot last for more than 0.1 s today. These matches with the YAG laser operation frequency. An additional shutter could increase the acquisition cycle time for complex VLSI devices.



CC-NDF: Computer-Controlled Neutral density filters; PD: Photodiode; DAB: Data Acquisition Board

Figure 2 - LAAS/HIREX picosecond pulsed laser facility

6 ELECTRICAL SET-UP

6.1 Test Set-up

Hirex test equipment was composed of a modular rack coupled with a generic memory test board :

This modular rack is derived from Hirex BILT modular instrumentation system name BILT.
Present rack configuration, named Tiny BILT, present 8 slots for modular instruments.
In addition to the existing power supply modules which cover the SEE test needs for measurement precision, remote control, LU detection, data storage , scope observation, etc, a new modular board has been specifically designed:
This modular board, named supervisor, provides

- A high speed communication link with the test board under vacuum (up to 500 ko/s)
- Management of DUT positioning (mover)
- Particle and test time counting

Dedicated to the test of memories, the generic test board is based on a 12 MIPs on-board processor which controls the test sequence and the communication with the rack.
The board include programmable logic circuits with a total capacity of 30000 cells and 960 macro-cells. This logic circuitry can work at high speed (up to 100 MHz) while being compatible with thermal requirements imposed by vacuum environment.
Adapters boards which can be mounted onto the mother board allows for fitting each memory product specificity, by adding extended functionality.
The board has a capacity of 50 pin-drivers, using transceivers able to interface memory devices with voltage supply requirements between 1 and 7 volts. The DUT can have two different power supplies.

6.2 Test Configuration

The test sequence was derived from the one used by Hirex during the heavy ion test already performed on similar samples. Some changes were brought to the test programme to cope with the laser test constraints.

The configuration used is a static test configuration and is called Self-Refresh. It consist in the following sequence :

1. Device initialisation
2. Write the test pattern in the memory and perform a read to check eventual stuck bits
3. Programming the DUT in the self-refresh mode
4. Wait for the trigger signal generated with the laser pulse.
5. Read the memory and count the errors
6. Loop with step 2, etc

Typical laser test runs consist in 10 000 laser pulses (100 * 100 hits arrays) and then the sequence steps 2 to 5 are repeated accordingly.

For each run, only one bank was selected and only part of the bank was considered for the test sequence.

The reason for that was that, as the laser pulse generation frequency was fixed and set to 0.1Hz, each test sequence (step2 to step5) described here above should be processed within less than 100ms.

6.3 Errors processing

Each word in error is detected and recorded together with the laser pulse number and the word address. This allows for further error data processing to correlate between the specific spatial laser pulse hit co-ordinates and the logical address of the word in error.

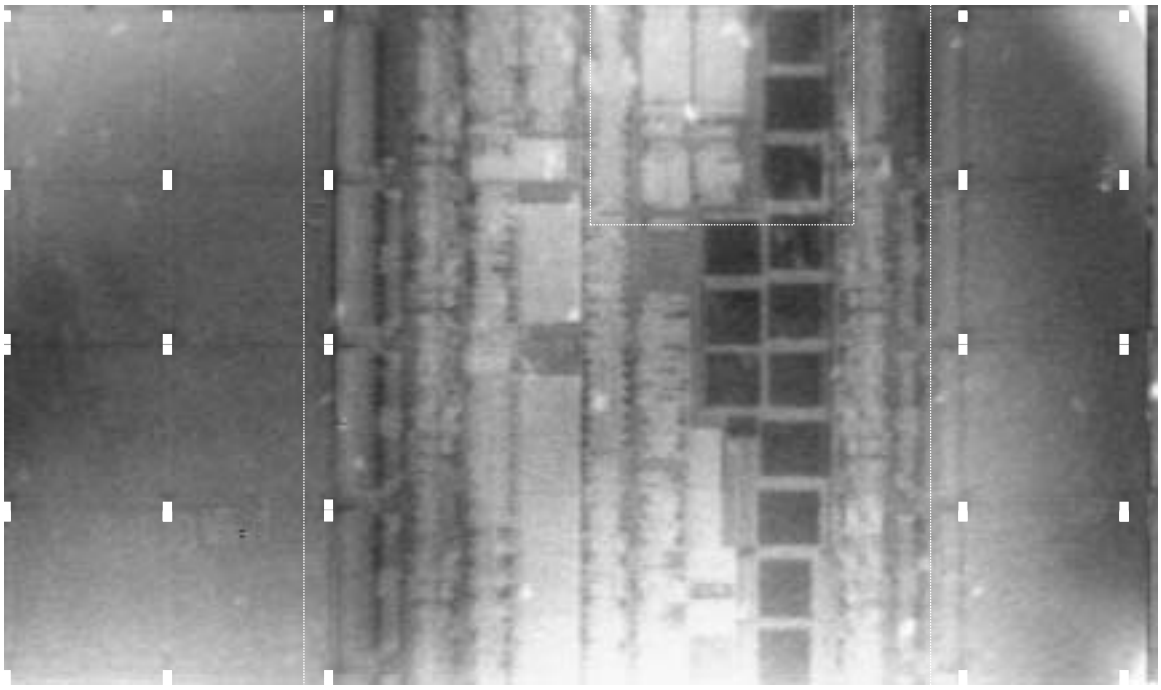
7 RESULTS

7.1 Samples preparation:

Using micro abrasive alumina powders, it was found possible to get a good optical surface finish on the four prepared samples. Mirror like surface could be obtained on each sample.
Samples were then successfully functionally tested.
This final surface preparation coupled with the thinning process used for heavy ion can be repeated routinely on new devices.

7.2 IR visualisation:

This was found to be the most difficult part of the study as the work consisted in adapting an existing system used in the visible range.
First of all, the different optical elements of the microscope used in the actual existing bench have been checked in order to eliminate any IR filtering elements.
Then different IR light sources were tested.
Lastly, it was found that the IR camera used was not very appropriate, as it worked by light integration and saturation was observed before an image of the chip could be obtained.
Figure 3 shows the image, which could be obtained after tight setting operations on the thinned Samsung sample.
However as sweeping on to the chip with the laser beam was the aim of this experiment, the image settings needs to be re-adjusted often to guaranty a good beam focus in the active volume area, it is clear that an other type of camera is needed for a nominal use of the laser and backside irradiation.



This figure shows a portion of the logical section of the die together with memory blocks delimited with white dots.

Figure 3 – IR visualisation from the chip backside.

Out of the three available lenses x5, x20 and x100, only the x5 and x20 lenses could be used successfully.
With the x100, it appeared that the existing set-up could not afford for IR visualisation and then for adjust the beam focus.

With the two first lenses the beam characteristics which could be achieved are the following:

Lens	NA	Spot diameter (µ)
X5	0.15	5
X20	0.4	1.7

7.3 Laser induced events

As explained above, only 256 k-bits were actually tested between each laser pulse and as the exact physical mapping of the memory under test was not known, the first runs consisted by successive trials on the 4 memory banks to locate the area under test.

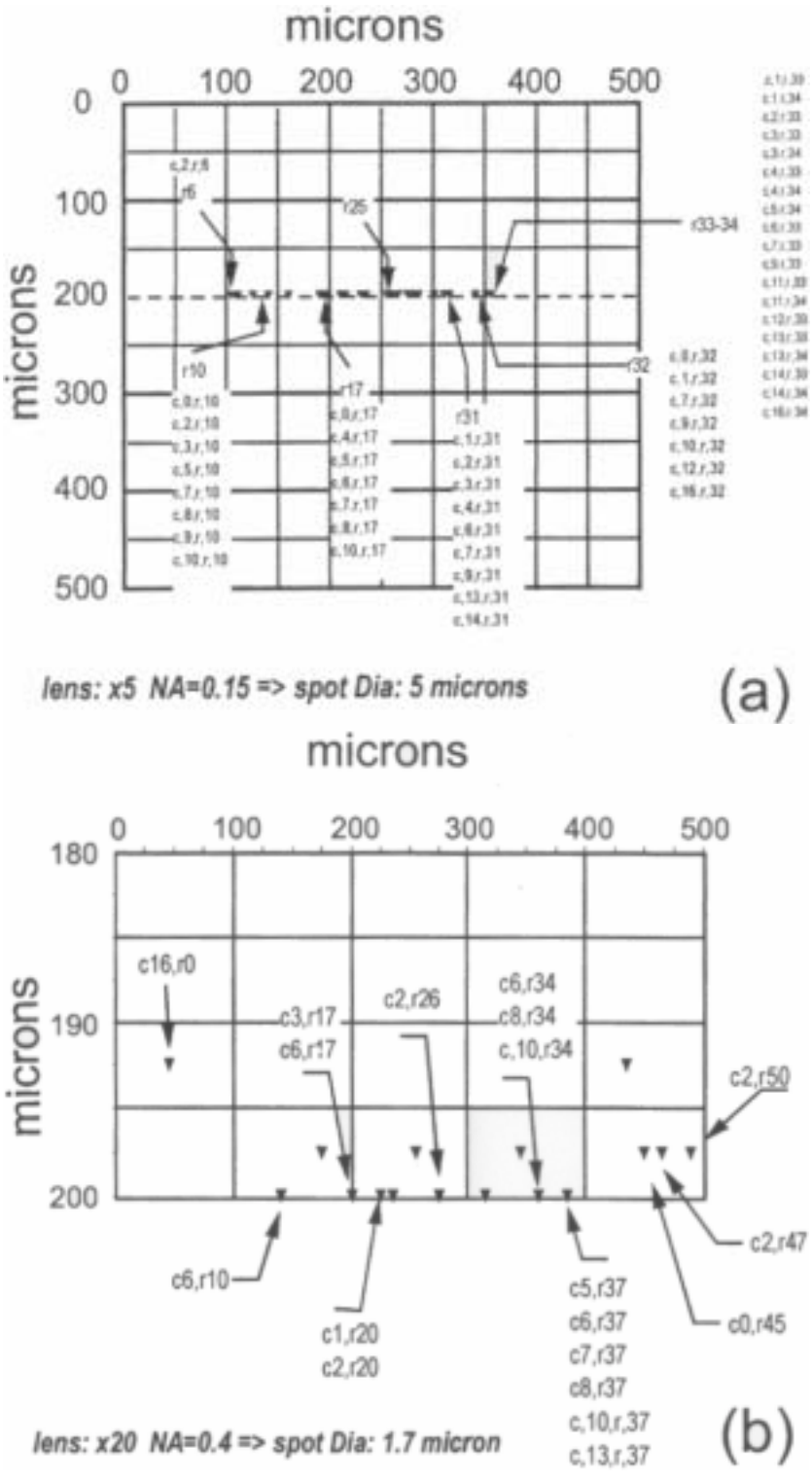
Then, when irradiating a portion of the memory array, of about 500µ x 500µ using the x5 lens, it was possible to trigger numerous events once the laser energy was set above a given threshold.

Further data processing showed that for a given hit, several cells could be upset. For each single hit, these cells correspond to a same logical row and successive columns numbers.
Repeating the same test with the x20 lens on the same chip area, similar results could be observed but this time with a smaller number of cells upset per hit. This is relation with the decrease in the spot diameter from 5µ down to 1.7µ.

This is illustrated in Figure 4 which shows a partial mapping obtained when the laser pulse was focused in a small region of Bank0 of Samsung thinned sample, using the two available beam diameters. For instance upper picture (beam diameter of 5µ) shows a single laser hit which induces 19 cells errors located (logical address) in rows 33 and 34 while in the lower picture 6 errors maximum were observed for a hit at row 37.

Lastly, when positioning the laser pulse on the logical section area of the chip, it was possible to get row or column errors (inside the 256kbit block under test)

Both the thinned sample and the 300µ die have been tested and experimented events. For the second sample, energy threshold had to be increased but still remained inside an acceptable range. (No locally destructive effects were observed due to energy absorption).



(a) Partial mapping obtained at low resolution : beam size is 5 µ
(b) Same region observed with improved resolution: beam size about 1.7µ diameter

Figure 4 –Error mapping on Samsung thinned sample, memory array area

8 CONCLUSIONS AND RECOMMENDATIONS

8.1 Conclusions

Main conclusion is that it is possible to trigger events with similar responses than the ones induced by heavy ions when using a picosecond pulse laser with a back side irradiation technique. This conclusion is very positive as, with the new complex devices, backside irradiation could be the most appropriate technique to characterize the different upset errors with a picosecond laser tool.

Indeed, a pulse laser is a very useful tool as it allows the analysis of the different events signatures: the device can be set in the same error conditions as often as needed and then analysis of the electrical signals can be performed to understand the device status.
This has to be compared with heavy ion experiments where all types of possible events occur randomly and then are more difficult to analyse and then to understand the impact of such an error in a design.

Lastly, when considering latch-up error, information related to the specific area where the latch-up can be triggered, is of prime importance to device designers and the laser technique is particularly adapted to this task.

Second conclusion is that beam diameter cannot be reduced below 1µ with 1,064 µ laser wavelength and this means that upsetting only one cell might be more difficult in the future with the continuously shrinking evolution of the technology. Unfortunately, in this study, due to the problems involved with the use of the x100 lens, it was not possible to check that only one cell of the 64M-bit SDRAM could be upset at a time (NMRC construction analysis showed that a trench capacitor used as the storage element of these memories is about 1µ diameter.)

Last conclusion is that a picosecond laser test bench for backside irradiation needs to be specifically built with elements dedicated to IR experiments.

It is clear that the set-up used, has allowed us to demonstrate the feasibility of the technique, but, in any case, could be used for routine work.
Moreover the fact that the picosecond laser used was for research work and need an important maintenance has limited the availability and then the number of experiments.
If a picosecond laser with backside irradiation technique has to be used in the future, a totally new set-up with an industrial picosecond laser together with an IR CCD camera has to be implemented.

8.2 Recommendations

The backside irradiation technique with a picosecond pulse laser has been experimented and proved to be feasible.

To offer this technique for routine work with a maximum of efficiency , the following would be needed at the same place:

- To master the sample preparation technique,
- To master the electrical test set-up
- To dispose of a laser test bench adapted to IR visualisation with a stable and accurate laser equipment.

A first exercise in the selection of the different elements indicates that an investment of about 120 000 Euros would be needed to have an adequate optical set-up. Details are provided here below:

8.2.1 Laser beam

The ability to accurately simulate the impact of a heavy particle drastically depends on the characteristics of the incident LASER beam.
In this scope, the optimum wavelength for the LASER beam would appear to be around 1µm, to insure

sufficient penetration range in the case of backside irradiation. The pulse duration must not be longer than a few tens of picoseconds, to remain in the same time scale as in the case of heavy ion induced charge creation. The energy deposited near the sensitive volume should be of a few mJ.
Of all the commercial offers for LASER sources, the PL2140 model from BFI OPTILAS turned out to be the most compliant to these requirements. Its features are listed in the table below.

Wavelength 1064 nm
Energy 30 mJ
Energy stability +/- 1.5 %
Pulse duration 20 ps
Pulse duration stability +/- 1%
Pulse rate Tunable from single pulse to 10 Hz

This model is a turnkey LASER source that requires minimal maintenance operations. It appears to be completely suitable for heavy ion simulation.

The LASER outputs a trigger signal just before with the LASER pulse, which allows synchronization with the electrical test setup. Thus, this setup would not only allow one to study the influence of spatial localization of the ion impact on error generation, but also to investigate the different effects of the same charge deposition at different times of the component activation cycle.

The estimated cost for this LASER source model is around 70000 euros.

Moreover, if needed, one can always use a filter at the output of the LASER source to alter the beam wavelength.

8.2.2 IR camera

To avoid long integration times and the associated noise in the image, a very sensitive IR camera is needed to locate the position on the part's die. The SU320MX model of InGaAs camera is suitable for this type of application. The estimated cost for this product is around 35000 euros.

8.2.3 Experimental setup

To avoid imprecision in the laser beam position, a proper optical table is needed to set the experiment up.
The cost of this product is around 6000 euros.
A standard optical bench (mirrors, attenuators, ...) will also be necessary, at the cost of about 1000 euros.

References

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Ref.2 "Generation and mapping of SEU's in flip chips by optical irradiation through the backside", F. Sellaye, J. Collet, JF Pascal, FX Guerre, R. Harboe-Sorensen, RADECS 2001 (Grenoble, F)