Connectivity and Packaging of Systems-of-Microsystems

Activity Summary
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1 Company Presentation

Lusospace, Lda.

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Lusospace was founded in 2002 and since then it has been increasingly involved in the space sector through numerous innovative and diverse programs. The AMR magnetometer being the first space hardware internally developed intended to fly in AEOLUS ESA satellite in 2007.
Along these years, extensive know-how in critical areas has been fostered and consolidated which together with a strong team-work culture has allowed Lusospace to acquire the necessary capabilities to successfully tackle ambitious and technologically challenging projects.
LusoSpace is a privately held company, covering the following main fields of activities:

- Attitude and Orbit Control System (AOCS)
- Laser systems and optoelectronics
- Electric Propulsion
- MEMS / MOEMS

Previous activities in MEMS included the projects “Procedures for MEMS Qualification” and “Optical MEMS for Earth Observation”. Current projects include “Validation and experimental verification of ESA MEMS qualification methodology” and “Miniaturization of a Magnetometer based on Micro Technology”. Previous and current activities in MEMS field provide important knowledge in the development and qualification of MEMS for space applications.
Lusospace vision is founded in two main cornerstones. The first is to the lead the space sector in the Portuguese market and the second is to develop and sell terrestrial applications which result from our space experience and its success.
Lusospace in this project is supported by the companies Optocap (Scotland) and Theon Sensors (Greece).

2 Overview / Scope of Activity

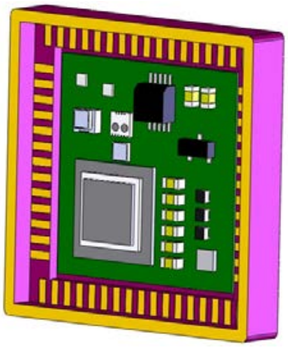
This activity is part of the ESA Basic Technology Research Programme (TRP). The objective of this activity is to demonstrate an integration and packaging solution enabling the realization of miniaturized 3D System-in-Packages, including MEMS components and electronics components assembled in a stack. The connectivity of the 3D System-In-Package with a PCB shall also be demonstrated. In addition, the packaging shall be optimized to cope with MEMS specific packaging constraints (e.g. limited mechanical stress, hermeticity of the packaging, etc.).

The project will set off by reviewing the MEMS packaging, SiP and Connectivity state-of-the-art techniques. After, the team will survey the most appropriate MEMS Foundries to supply the MEMS sensors and electronics, if possible. During this phase, the preliminary selection of package materials shall also take place, as a proper material selection is critical for the device simulation, manufacturing process design and also for the electrical design of the device. The second step is the design of the system comprising sensor and control electronics.

This will address the multi-sensor arrangement, electronic circuits to drive and receive the sensors output signals and calibration circuits should those be deemed necessary. Next, the design of the device package will be developed.
Once the sensor/control circuits and package design is completed, the preliminary design can be disclosed. Following the basic device specification, the project moves to the simulation phase. In this stage, the basic functionalities are confirmed and the physical layout of the device is simulated. Following is the manufacturing phase in which the sensors and control circuits will be processed in the assembly and packaging production lines. A comprehensive manufacturing plan will be followed not only to guarantee process control but also to monitor process yield and manage process failures.
Finally, during the test campaign phase the devices will undergo an approved test plan in order to study the package performance. The test results will then be analysed and the conclusion shall provide insight on the integration and packaging approach.

In this context, primary achievements in this activity shall be:

- design and develop a System-in-Package containing MEMS devices and ASIC;
- manufacture the proposed SiP;
- access performance and reliability of the SIP in space environment.



Typical characteristics for the final device shall be:
- Multiple chip architecture including stacked naked dies arrangement;
- SiP hermetic package;
- Miniaturized architecture;
- External interconnection;

Timescale

The overall project duration is planned to be 24 months starting from January 1st, 2013.

3 Activity approach and Work Structure

The activity approach and work structure for the study "Connectivity and Packaging of Systems-of-Microsystems" are based on the ESA Statement of Work ref. TECQTC/SoW12MSiP/LM.
The work breakdown structure is divided into 4 major technical tasks and one management task.

Task 1: Survey and selection of the SiP technology and of the components to be packaged

A review of the state of the art of MEMS packaging, SiP technologies and connectivity techniques shall be performed. MEMS and electronics components that could be used for the realization of a SiP demonstrator shall be identified. Detail activities in this task are:

WP1100 – Survey and selection of packaging and connectivity techniques

Survey and critical analysis of the state of the art in MEMS packaging, smart systems integration, Systems-in-Packages (SiP) and related connectivity techniques shall be performed. The selected 3D/SiP and connectivity solution for this project shall be as generic as possible to enable its use with a large range of MEMS and electronic components.

WP1200 – Survey of available components for SiP technology demonstration

The components selection shall be driven by the need to demonstrate and assess the selected SiP technology, rather than by a specific application.

WP1300 – Preparation of the test plan

Preparation of a test plan addressing, among others: the demonstration that the functionality and performance of the components is maintained after the packaging; assessing the stress applied on the MEMS by the packaging; assessing the level of protection from external environment achieved and test the robustness of the packaging under thermal and mechanical stress; long term stability via endurance testing and storage.
The test plan shall include a test flowchart describing the nature of the tests, the number of devices to be used, the test conditions and the pass/fail criteria to be applied. The test plan shall also define how the functional tests will be performed on the components before and after assembly. The required test

set-ups shall be described in the test plan and an associated implementation plan shall be provided (making sure that all necessary test equipment will be available and accessible at the time of the performance of WP4100).

The Technical Note 1 (TN1) shall be prepared containing the results of the survey on the SiP technology and on the components to be packaged as well as the proposed test plan followed by preliminary design review.

Task 2: Design of the SiP demonstrator

This task consists in the production of the design and process flow for the realization of a SiP demonstrator implementing the selected MEMS and electronics components.

WP2100 – Design of the SiP demonstrator

A design of the SiP demonstrator will be proposed, taking into account the following objectives, among others: demonstrating the stacking and micro-packaging of the naked MEMS chips and the electronic chips; implementing the interconnections between chips and the external SiP connectivity; achieving the hermetic packaging of the MEMS components; achieving good reproducibility and good reliability.

From an architectural point of view, it would be preferable if each function was built on a separate module/layer to achieve a modular construction. The feasibility of this modular construction in the case of this demonstrator shall be discussed. A description of the process flow and identification of the critical process steps of the assembly and connectivity process shall be prepared.

The Technical Note 2 will be prepared containing the design description, functionalities and performance and the process description. Task 2 will be completed with the Critical Design Review (CDR).

Task 3: Fabrication of the SiP demonstrator

Task 3 shall be dedicated to the validation of critical process steps and the fabrication of the SiP demonstrator.

WP3100 – Validation of critical elementary process steps

The experimental validation of critical elementary process steps in preparation for the fabrication of the SiP demonstrator shall be performed. The steps to be validated will be designated during the CDR. If necessary, dummy components can be used as long as they represent a similar risk for the process step under evaluations.

The results of the critical process steps validation shall be sent to the technical officer at the completion of this WP in the form of Technical Note 3, part 1, containing at least and to discussed via teleconference: description of every process step under validation; validation procedure, including the type of components used for the test; the evaluation criterions for each process steps; the result of the evaluation for each process steps; the need and/or possibilities of assessing the critical steps during the fabrication of the SiP demonstrator. The process steps validation shall be successful before proceeding to WP3200.

WP3200 – Fabrication of the SiP demonstrator

The necessary components shall be procured and then shall be manufactured a sufficient number of units to be able to perform the tests as planned and agreed during the PDR. Any unexpected issues with the fabrication shall be reported to ESA immediately. Any production reject shall be recorded, analyzed in detail, and reported in the Technical Note 3. The reason for the reject shall be clearly identified. The final fabrication yield shall be reported to ESA via the technical note. ESA reserves the right to inspect, at any time, the processed SiP demonstrators. In addition, at least 2 units shall be delivered to ESTEC for ESA independent testing.

Technical Note 3 (TN3), including TN3 part 1 already produced, shall be prepare covering a description of the work performed during task 3, including details of the actual processing performed and a report of any issue encountered during the fabrication. Task 3 will be completed by the performance of a Test Readiness Review (TRR).

Task 4: Test of the SiP demonstrator

Task 4 shall be the performance of the tests and their analysis to conclude on the suitability.

WP4100 – Test of the SiP demonstratorTesting of the SiP demonstrator shall be performed, following the test plan agreed at PDR. The test results shall then be analyzed, including a discussion on the achievements and the limitations of the proposed integration and packaging approach (e.g. number of layers, die size, type of MEMS that can be packaged, potential reliability issues, suitability for the space environment, etc.). Recommendation for potential future work shall be prepared, in view of the obtained results.

Technical Note 4 shall be prepared containing a description of the work performed during task 4, including the test report and the analysis of the results.
The units of the SiP demonstrator remaining at the end of the study shall be delivered to ESTEC.

ID	Text1	Task Name	Duration	Start	Finish	Predecessors
1		**Connectivity of Packaging od Systems-of-Microsyster**	**520 days**	**Tue 1/1/13**	**Mon 12/29/14**	
2						
3	**Phase 1**	**State of the Art review and components identifica**	**85 days**	**Tue 1/1/13**	**Mon 4/29/13**	
4	**Task 1**	**Survey and selection of the SiP technology ar**	**85 days**	**Tue 1/1/13**	**Mon 4/29/13**	
5	WP1100	Survey and selection of packaging and connec	30 days	Tue 1/1/13	Mon 2/11/13	
6	WP1110	Package/PCB mechanical interface analysis	30 days	Tue 1/1/13	Mon 2/11/13	5SS
7	WP1120	Analysis of hermeticity solutions	20 days	Tue 2/12/13	Mon 3/11/13	6
8	WP1130	In-plane versus vertical stacking analysis	20 days	Tue 2/12/13	Mon 3/11/13	6
9	WP1200	Survey of available components for SiP technc	20 days	Tue 3/12/13	Mon 4/8/13	8
10	WP1300	Preparation of the test plan	15 days	Tue 4/9/13	Mon 4/29/13	9
11	**Phase 2**	**Fabrication and Testing of a SiP demonstrator**	**430 days**	**Mon 5/6/13**	**Mon 12/29/14**	**3**
12	PDR	Preliminary Design review	0 days	Mon 5/6/13	Mon 5/6/13	10FS+5 days
13	**Task2**	**Design of the SiP demonstrator**	**95 days**	**Tue 5/7/13**	**Mon 9/16/13**	
14	WP2080	MEMS components analysis	30 days	Tue 5/7/13	Mon 6/17/13	12
15	WP2090	Front-end and Back-end electronics analysis	30 days	Tue 5/7/13	Mon 6/17/13	12
16	WP2100	Design of the SiP demonstrator	60 days	Tue 6/18/13	Mon 9/9/13	15
17	CDR	Critical Design Review	0 days	Mon 9/16/13	Mon 9/16/13	16FS+5 days
18	**Task 3**	**Fabrication of the SiP demonstrator**	**170 days**	**Tue 9/17/13**	**Mon 5/12/14**	
19	WP3090	Test set-up preliminary design	15 days	Tue 9/17/13	Mon 10/7/13	17
20	WP3100	Validation of critical elementary process steps	20 days	Tue 10/8/13	Mon 11/4/13	19
21	WP3110	Manufacturing plan	20 days	Tue 11/5/13	Mon 12/2/13	20
22	WP3115	Sensor and electronics procurement	30 days	Tue 11/5/13	Mon 12/16/13	20
23	WP3120	Sensor and electronics supply	15 days	Tue 11/5/13	Mon 11/25/13	20
24	WP3130	Test components procurement	20 days	Tue 12/17/13	Mon 1/13/14	23,22
25	WP3140	Pilot production device fabrication	20 days	Tue 1/14/14	Mon 2/10/14	24
26	WP3200	Fabrication of the SiP demonstrator	60 days	Tue 2/11/14	Mon 5/5/14	25
27	TRR	Test Readiness Review	0 days	Mon 5/12/14	Mon 5/12/14	26FS+5 days
28	**Task 4**	**Test of the SiP demonstrator**	**165 days**	**Tue 5/13/14**	**Mon 12/29/14**	**18**
29	WP4090	Test Set-up manufacturing	20 days	Tue 5/13/14	Mon 6/9/14	27
30	WP4100	Test of the SiP demonstrator	90 days	Tue 6/10/14	Mon 10/13/14	29
31	WP4200	Test results analysis	50 days	Tue 10/14/14	Mon 12/22/14	30
32	FR	Final Review	0 days	Mon 12/29/14	Mon 12/29/14	31FS+5 days
33	**Task 5**	**Management**	**520 days**	**Tue 1/1/13**	**Mon 12/29/14**	**5SS**
34	WP5100	LS Management	520 days	Tue 1/1/13	Mon 12/29/14