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Study of Radiation Effects in Cryogenic Electronics and Advanced Semiconductor Materials

Final Report

Deliverable D6

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Abstract

This report constitutes Deliverable D6 of Work Order 1938/96/NL/NB on "Study of Radiation Effects in Cryogenic Electronics and Advanced Semiconductor Materials". It is the Final Report and summarizes the main results that have been obtained during the execution of the Work Order. The report contains two parts, one related to Activity I on Radiation Effects in Cryogenic Electronics, and one dealing with Activity II on Radiation Effects in Advanced Semiconductor materials. In case that the results have already been described in detail in one of the Deliverables, only the main results and conclusions are given. However, for Activity II there are some new results included related to the recently performed second proton irradiation round. Important conclusions are i) the circuits envisaged to be used are sufficient radiation hard when processed in a non-LDD 0.7 μm CMOS technology, ii) the kink effect can be beneficially influenced by either a proton or a γ-irradiation, iii) for total dose testing it is important to be able to perform irradiations at cryogenic temperatures, iv) advanced processing modules such as shallow trench isolation and nitrided gate oxides have an impact on the radiation hardness of a 0.18 μm CMOS technology ,v) the use of scaled down COTS CMOS devices looks very promising. The report concludes by giving an outlook for future activities in this field.

INTRODUCTION

This report constitutes Deliverable D6, associated with RFQ/3-8938/97/NL/NB on "Study of Radiation Effects in Cryogenic Electronics and Advanced Semiconductor Materials " It should also be considered as the Final Report of this Work Order, which consisted of two Activities: Activity 1 related to Radiation Effects in Cryogenic Electronics, and Activity 2 dealing with Radiation Effects in Advanced Semiconductor Materials. Each Activity was scheduled to run for 18 months. The project started on May 1, 1997 and ended on June 15, 2000. Compared to the original time schedule there was a delay of 6 weeks, mainly because of unforeseen maintenance requirements of the proton irradiation facility at Louvain-La-Neuve (Cyclone cyclotron).

For each of the two Activities, the main results and conclusions are only briefly discussed as reference is made to the different Deliverables. These Deliverables report extensively on all the different experiments and the obtained results. Each Activity always started with an in-depth critical review of the available literature in the field, thereby forming the basis for the definition of additional experimental work. All experiments were done on devices and circuits fabricated at IMEC. During the execution of the first Activity related to Radiation Effects in Cryogenic Electronics, special attention was given to the performance of the prototype circuits envisaged to be used for the FIRST mission. For the second Activity on Radiation Effects in Advanced Materials, the focus was on the evaluation of the IMEC's 0.18 μm CMOS technology. Beside a general study of the radiation performance of the technology, dedicated process modules such as the isolation technology and the nitridation of the gate oxide were investigated in more detail, as these processes will gain in importance for future scaled down technologies. This part of the report is more extended than the first part, as some new results related to the second proton irradiation round are included. These were not addressed in previous Deliverables.

The Final Report includes a general conclusion and an outlook for possible future activities. For completeness a list of all the generated documents and the resulting publications and conference contributions is given in the Appendix.

ACTIVITY I: RADIATION EFFECTS IN CRYOGENIC ELECTRONICS

The Activity is related to the theoretical and experimental study of radiation effects in cryogenic electronics and contained three main Work Packages:

- Literature Survey
- Radiation testing and Analyses
- Reporting

The work performed and the results obtained during the execution of the work are briefly summarized. Reference will be made to the different Deliverables for more information.

I.1 Literature Study on Radiation Effects in Cryogenic Electronics

The aim of this work package was to draw some general conclusions from the extensive literature study with respect to the low temperature operation of silicon electronics and more in particular regarding the radiation response. From this, some guidelines for the radiation test plan could be drawn. For the latter it is essential to focus on a number of pertinent questions.

A first key issue is whether or not it is relevant to perform the irradiations at cryogenic temperatures. The answer to this question is different in the case that displacement damage is at stake or the total dose response. One can roughly state that the stable displacement damage created is larger for room temperature irradiations compared with cryogenic irradiations. This follows from the larger introduction rates of the most prominent radiation defects. Of course, the stable defects created at low temperatures can be quite different than the room temperature ones. Anyhow, a marked difference is to be expected for irradiations well above 100 K and below (77 K and 4.2 K), where the vacancy is believed to be immobile and thus creates a number of stable defects in the bandgap. As a conclusion from all this, one can say

that the room temperature displacement damage studies can be considered as a kind of worst case situation and therefore are on the safe side.

Total dose effects on the other hand, follow a completely different behaviour. Operation at 77 K prevents the trapped holes first of all to move towards the negative interface and secondly to escape (tunnel), to recombine, to annihilate or to be transformed into interface traps. As a consequence, the degradation of the gate oxide (and field oxides) should be clearly more pronounced at low temperatures. In addition to that, very little information is available with respect to 4.2 K behaviour - of interest for the FIRST mission for example. A related aspect is the effect of single-events on low temperature CMOS devices and circuits. The available studies indicate that the susceptibility towards latchup (or the cross section) increases significantly below •100 K, which is of concern for cryogenic space electronics. Certainly more data (down to 4.2 K) would be welcome to have an idea about the SE response of CMOS.

A second important item is whether one should harden the technology for cryogenic operation or not and this in view of the recent COTS (custom-off-the-shelf) strategy. There is indeed more and more a tendency to abandon considerable technology hardening efforts and to replace expensive hardened space components by standard commercially available devices. Along with this line of thought goes a strategy for risk management, built-in sufficient redundancy etc.. From a radiation effects viewpoint, the downscaling of technologies in some aspects bears an inherent hardening by the use of thinner gate oxides, different more radiation tolerant isolation schemes and so one, which improves the total-dose response. Of concern, however, become the single-events effects. In fact, even for non-space, or non-military applications, the DRAM community is concerned about the effect of the natural radiation environment on present-day and future generations of memories.

The sense of this new philosophy may be questioned for cryogenic applications. In many cases, the technology needs to be optimised anyhow for specific cryogenic operation, in order to meet the requirements and to reduce/eliminate some specific low temperature anomalies, like kink and transient effects. Since no standard (off-the-shelve) technology is used, it becomes worthwhile to reconsider the use of hardening techniques in addition to cryogenic hardening. This goes of course at the

expense of integration density and an increased processing complexity and risk (lower yield?). The first point, however, is not really an issue for most of the envisaged cryogenic space applications. Taking into account the dominance of CMOS for cryogenic applications, one should particularly focus on the ionization damage (i.e. total dose and SE).

It is also worthwhile mentioning that bipolar technologies show an inherent better radiation tolerance compared with CMOS. This means that SiGe-based technologies may be attractive alternatives in the "near" future. It probably explains the fast growing interest in radiation studies of these materials and devices. However, little information is available on the radiation response at cryogenic temperatures. In addition, bulk displacement damage may be of concern for the SiGe layers, which seem to be (more) susceptible than silicon. Some radiation aspects of more advanced silicon based technologies have been studied in the second Activity of this Work Order.

With respect to the radiation damage response of cryogenic circuits probably the same remark can be made as with respect to hot-carrier degradation. The degradation of a device in many cases gives an overestimation of the observed circuit operation. This may be related to the fact that for many ICs, the operation voltages switch continuously (ac mode of operation), whereby the "damage" experienced during the positive cycle for example, is partially counteracted during the negative cycle. The studies of the individual components are particularly important from a fundamental viewpoint, in order to get a better understanding of the degradation mechanisms involved. Such studies can also be of interest from a technological (hardening) viewpoint, since one can better estimate the effect of a certain technological change. On the other hand, it is strongly felt that it is very risky to extrapolate results obtained at a transistor level to a complete integrated circuit. In other words, it is hard to predict the radiation response based on device simulators. This is the more true for cryogenic operation, where even the low-temperature static device parameters can not be accurately predicted aforehand. In addition, there is insufficient data base to even start thinking of building technology specific cryogenic radiation simulators.

The following general guidelines for defining a radiation test plan had to be taken into account:

1/ **Total dose testing** should preferably be done at the operation temperature of interest. This brings along some heavy practical roadblocks as there are not so many radiation facilities available to allow low temperature γ-irradiation **under operation bias** and **in-situ testing**. Alternatively, one can think of irradiating the devices at room temperature (or maybe at low temperature, if no local testing is possible) and to store the device at low temperature (liquid nitrogen?) in between irradiation and cryogenic testing, to prevent considerable annealing. Within the first phase of the present Work Order, the possibilities to perform cryogenic irradiations will be explored. Although technical aspects are the main concern, economical issues will also have to be taken into account.

2/ For displacement damage evaluation, one can consider to perform the irradiations at room temperature, followed later by a cryogenic testing. In-between, one could store the irradiated parts at LNT. An important remark with respect to high energy ion irradiation is that if devices are mounted in a metal cryostat, there can be a serious constraint related to radiation protection. Parts of the cryostat may become activated. Additionally, the metal shielding of the cryostat requires rather high energies for the bombarding particles. These may not be the most relevant energies for the envisaged missions.

3/ It is important to irradiate both circuits and individual devices of the same technology in parallel and under realistic bias conditions. A sufficient amount of circuits should be irradiated at the same time to allow some statistical variation. The irradiation of the circuits are to be considered as go/no go tests and should be for sufficiently high doses, in agreement with the total dose expected during the FIRST mission. A detailed evaluation at a component level is essential to gain some fundamental insight into the degradation mechanisms and to evaluate possible hardening measures.

I.2 Radiation Testing of Cryogenic Devices and Circuits.

Based on the literature review, it was decided to have some cryogenic circuits, specially designed as prototypes for the FIRST mission, irradiated with both gamma's and protons. Along with these circuits, selected test structures were also irradiated. The outcome of a first irradiation round would form the input for the experimental conditions for the execution of a possible second irradiation round. All these irradiations have been performed at room temperature. As the literature study pointed out that, in case of total dose effects, the device performance more severely degrades if the irradiations are done at low temperatures, another task was devoted to investigate the possibility for cryogenic irradiations. The full experimental details and all obtained results are described in Deliverable D2 (P35284-IM-Rp-0012). Therefore, this section will only summarize the most important conclusions.

The experimental study allowed to draw some important conclusions, especially related to the technology used for the fabrication of the cryogenic electronics which will be applied for the prototypes. One has to differentiate between, on one hand, the irradiation type (protons or gamma's) and, on the other hand, between the device and the circuit performance.

- For the studied fluences the impact of proton irradiation on the electrical device performance is typically of the order of 10%. A pronounced influence is seen when there is a Lowly Doped Drain (LDD) region present. While for p-channel devices with LDDs the expected irradiation induced reduction of the threshold voltage and drain current is observed, non-LDD devices can show a rebound effect as illustrated in Fig. I.1. The latter implies that for moderate fluences the drain current increases, while for higher fluences a reduction is noticed. Additional irradiation experiments would be required to acquire a better understanding of the physical mechanisms at stake.

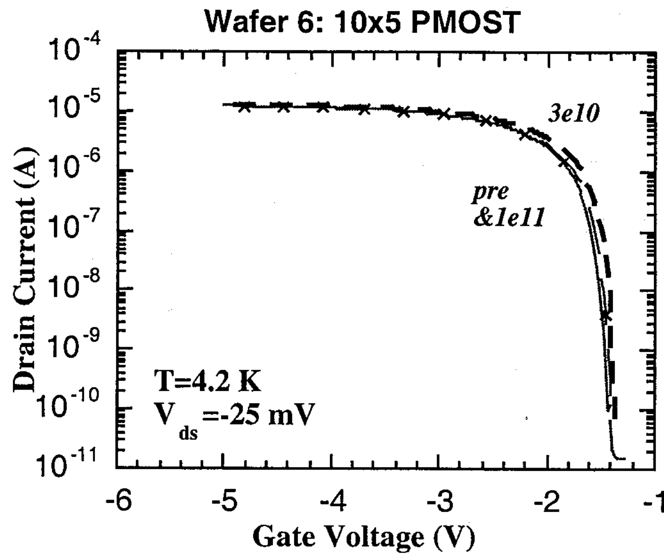


Fig. I.1. Input characteristics of a split 1 10 μmx5 μm proton irradiated p-MOSFET at 4.2 K, before and after two 60 MeV proton fluences.

- In the case of γ-irradiation the classical device performance degradation is observed, i.e. a reduction of the threshold voltage and an increase of the transconductance for n-channel devices and the opposite trend for p-channels. In contrast to the proton irradiations, no rebound effect is seen for the non-LDD p-channels. A particular feature, observed for the first time according to the author's knowledge, is the fact that γ-irradiations can reduce the pre-irradiation kink effect present in n-channel devices operating at cryogenic temperatures. This phenomenon, which is shown in Fig. I.2, might be explained by the generation of positive oxide and interface charges. The well-known occurrence of hysteresis effects at cryogenic temperatures is not influenced by the irradiations. Although the used technology is quite hard from a total dose viewpoint, a further hardening is obtained by eliminating the threshold voltage adjustment ion implantation. There is no clear scaling of the performance degradation with the fluence.

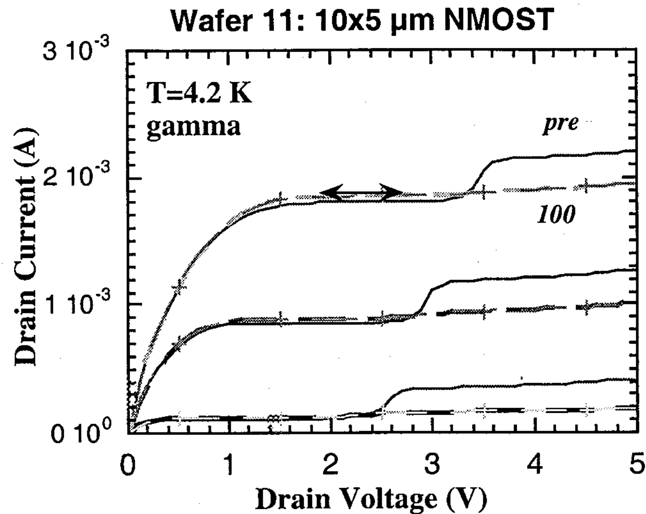


Fig. I.2. Output characteristics of a γ-irradiated split 11 n-MOSFET at 4.2 K, corresponding to a dose of 100 krad(SiO_2). Both the low-to-high and high-to-low curves after 100 krad are shown.

- The study of the post-irradiation device performance leads to the conclusion that the highest radiation hardness is achieved for a technology without LLD's, transistors without oxide spacers and removal of the threshold voltage adjustment implant. The latter may have an impact on the symmetry of the threshold voltages for the n- and p-channel devices. Whether or not the LDDs and the spacers can be eliminated depends on the minimum feature size of the circuits.

- The study of the post-irradiation performance of the FIRST prototype circuits points out that the used technology is sufficiently radiation hard for the studied proton and total dose irradiations. However, it is essential to remark that in the case of total dose radiation hardness assessment room temperature irradiations are not the worst case situation. It is, therefore, essential to perform also some cryogenic irradiations.

The main recommendations for future activities related to the above mentioned conclusions are:

- Execution of additional proton irradiations at room temperature in order to get a better insight into the physical mechanisms involved in the impact of the presence of LLDs on the displacement damage.
- Modeling experiments in order to explain quantitatively the basic mechanisms leading to a reduction of the kink phenomenon during cryogenic operation.
- Execution of low temperature irradiations in order to study in detail the total dose irradiation hardness of both the devices and the circuits.

Dedicated experiments are needed in order to determine the differences between room temperature and cryogenic irradiations to point out the impact of possible room temperature annealing effects in the first case. Especially in the case of γ-irradiations the irradiation at room temperature could be too optimistic.

I.3 Manual for Cryogenic Electronics in Space Applications

The objective of deliverable D3 was to formulate some practical guidelines for the development, the design and the testing of radiation hard cryogenic electronics intended for operation in the liquid helium temperature (LHT) range. They were formulated keeping two main goals in mind: first, successful operation at 4.2 K and, second, providing sufficient resistance against (space) radiation damage. The report was aimed to be concise and contained three parts. Part 1 focused on technology aspects, part 2 on design guidelines and part 3 concerned some testing prescriptions.

I.3.1. Technological Aspects

The radiation testing performed during the first phase of the project yielded some interesting trends. In summary, the non-LDD devices gave rise to a better radiation performance, so that this is again an argument in favor of skipping this process module. One of the effects observed was that the change in V_T at 4.2 K was 20 times smaller for non-LDD devices compared with their LDD counterparts. Furthermore, the non-LDD p-MOSFETs showed a slight improvement of the I-V characteristics for low to moderate proton irradiation fluences, which was not

observed for the LDD case. Previous studies also highlighted the extra device degradation associated with the series resistance of the LDD devices. The main reason for this enhanced susceptibility to radiation is the presence of the spacer oxides on top of the LDDs, which are of inferior quality than that of the gate oxide. This is due to the fact that spacer oxides are not thermally grown but rather deposited. Positive charging of the spacers causes a change in the surface potential and in the carrier density of the LDDs, leading to a change in R_S.

With respect to the well processing, one positive feature which came out of the study was the reduction of the drain current kink in saturation after exposure to both protons or γs. The kink reduction can be explained by the change in the 4.2 K substrate current characteristic observed after the exposures.

I.3.2. Design Considerations

There are a number of well established design techniques for improving the radiation hardness of CMOS technologies. These include the use of closed geometry devices or of guard rings. It has been demonstrated in the past that these techniques are also successful for low temperature operation. Maybe more specific for cryogenic electronics, is the use of cascode transistors. It is a transistor consisting of two parts in series with a common contact, preferrably left floating. It helps in reducing the kink effect. This has for example been shown convincingly for partially depleted (PD) SOI transistors operating in the so-called twin-gate mode. Not only the drain current kink is removed, but also the associated low-frequency (LF) noise overshoot. It has furthermore been demonstrated that the noise margins of SOI inverters improve drastically for twin-gate structures. This design concept has a good potential for analogue applications.

I.3.3. Cryogenic irradiations

For displacement damage studies room temperature irradiation is a kind of worst case situation. This implies that no direct cryogenic irradiations are needed if

one accepts that the taken measures to improve the radiation hardness are maybe an overkilling of the problem.

For total dose effects the situation is quite different. Operation at 77 K prevents the trapped holes first of all to move towards the negative interface and secondly to escape (tunnel), to recombine, to annihilate or to be transformed into interface traps. Therefore it is expected that the degradation of the field and eventually also of the gate oxide will be more pronounced during low temperatures irradiations. As also stated before, while some information can be found in the literature for 77 K irradiations, this is hardly the case for irradiations at liquid helium temperatures. This is very important for the studied FIRST prototypes as they have to function at LHT.

The main problem with the cryogenic irradiations are related to the following aspects:

- The irradiations have to be performed while the devices are cooled. This may cause some hardware configuration problems. There are not many irradiation facilities offering this option.
- The devices and circuits have to be kept at cryogenic temperature untill the post-irradiation characterization has been completed. This implies that one either needs access to test facilities near the irradiation place or that one has to transport the devices in a cooled Dewar. The latter may cause some problems with the safety regulations.

ACTIVITY II

RADIATION EFFECTS IN ADVANCED SEMICONDUCTOR MATERIALS

This Activity contained three main Work Packages:

- Literature Survey
- Radiation testing and Analyses
- Reporting

The work performed and the results obtained during the execution of the work are briefly summarized, with the exception of the Radiation testing for which new data have been generated, which were not reported before. Reference will be made to the different Deliverables for more information.

II.1 Literature Survey

The main goal of Work Package was to give a critical literature review of the published information on the radiation performance of advanced materials and devices. Different technologies such as Ge, SiGe, bipolar, submicron CMOS, and GaAs have been reviewed and discussed. Attention was also given to optoelectronic and ferroelectric materials and components. The quite extensive review resulted in Deliverable D4, containing more than 250 pages. The most important conclusions resulting from this literature study are briefly summarized:

- The radiation-induced defects in Ge materials and devices are much less studied and characterized than those in silicon. To some extent this is due to the fact that the available analytical tools have mostly been optimized for silicon and are more difficult to use for Ge. Therefore, there are still a lot of questions to be answered such as the impact of the irradiation particle on the

divacancy and the role of the substrate quality on the irradiation-induced defects. In view of the strong interest to use Ge-based solar cells for space applications, it would be interesting to study the impact of high energy proton irradiations.

- SiGe is a rather new technology, which is gaining more and more interest. Although the dominant radiation-induced defects are known, less clear information is available on the impact of the Ge concentration. Much activity has to be done related to modeling the impact of these defects on the electrical performance of the devices. The radiation response of SiGe diodes is rather well documented, no real data is available on the SiGe field effect devices. It is therefore too early to make any conclusions on their radiation hardness compared to silicon-based devices.

- The radiation performance of bipolar devices has been studied for several decades. Also the radiation behavior of modern bipolar technologies is being studied and there is the general trend that downscaling will improve the radiation resistance. However, detailed information is lacking on the bulk damage effects after high-energy particles. Some of the advanced processing steps may also lead to plasma-induced damage, especially in the spacer oxides.

- Also for future submicron CMOS technologies, it is expected that downscaling of the geometries will have a positive impact on the radiation performance. The implementation of alternative gate dielectrics and advanced isolation schemes (e.g. shallow trench isolation) has surely to be monitored in order to avoid the occurrence of second-order effects which may become more pronounced and therefore can have a degrading impact on the device/circuit lifetime and reliability. In view of the general trend to use COTS for space applications, an investigation of the radiation hardness of sub 0.35 μm technologies is required.

- In general, GaAs-based technologies are well known for their excellent radiation hardness, which is much better than for silicon-based technologies. However, photodiodes and optical components may still suffer from

displacement damage. There is also a good understanding of the fundamental aspects of the irradiation-induced defects and the correlation with microscopic parameters such as NIEL. There is, however, some discrepancy between the calculated NIEL and the experimentally observed variation of the device parameters in case that high energies are used. This requires some further attention.

- A totally new generation of optoelectronic III-V based devices are nowadays gaining more and more interest for a variety of applications. Before they can be used for space applications a more detailed radiation testing is needed. An important parameter to monitor is the low frequency noise performance. Even more pronounced than for some other components, it is essential to irradiate these devices while applying the standard operating conditions.

- Ferroelectric materials and devices are newcomers in the field and, therefore, only a limited amount of information on their radiation hardness is available. Initial irradiation testing is, however, showing very promising results. It is expected that ferroelectrics may become very important for both infrared and non-volatile memory applications.

This review clearly pointed out that the future use of the present day state-of-the-art devices and materials requires some additional radiation testing, complemented in some cases by more fundamental studies. Therefore, within the second Work Package within this Activity, attention has been given to a radiation study of advanced devices fabricated by IMEC.

II.2 Radiation Testing of Advanced Microelectronic Devices

Based on the literature study outlined above, it was decided to focus on the radiation damage in the 0.18 μm CMOS technology, which is IMEC 's current workhorse technology. Also microelectronics industry is now moving towards this level of scaling. The radiation testing has been done employing two 60 MeV proton irradiation rounds. The first one was November 99 and the second one in March 2000. The results obtained after the first irradiations are described in details in Deliverable

D5 (P35284-IM-RP-0018), so that here only the most important results and conclusion will be summarized. A full report will be given on the second irradiation round.

II.2.1 Results Obtained from the First Round of Radiation Testing

It has been demonstrated that deep submicron transistors and process modules suffer from radiation damage albeit for a higher fluence range than typically encountered in a space environment. However, even for a fluence of $3x10^{10}$ cm^{-2} 60 MeV protons, some subtle changes are induced particularly in the n-channel transistors. In fact, unusual device parameter shifts have been noted, i.e. an increase of the threshold voltage for example, which become furthermore length dependent. These two aspects, which are illustrated in Figs II.1 and II.2, deserve and require further in-depth studies in view of the ongoing trend in downscaling. The results suggest that some new or modified degradation mechanisms occur, which are maybe no longer related to the thin gate oxide itself, but to other parts of the device structure, such as e.g. the isolation along the edges or the extension region. In addition, one should not overlook the impact of non-ionising energy losses in the highly doped p-well (substrate) regions upon interaction with protons. The generation of radiation-induced trap levels generally increases with the doping density. This is certainly the case for boron, which is known to interact with silicon interstitials to create mobile interstitial boron B_i. It could be worthwhile in future experiments on MOS transistors to assess the changes (if any) in the p-well doping density by measuring for example the body factor dependence on the threshold voltage V_T. Also the study of diodes processed in the corresponding well could facilitate such a study, by using C-V measurements.

The observed length-dependence of the parameter shifts is quite intriguing and can be to some extent understood in view of the charge-sharing concept. However, a further modeling is required in order to fully understand what is going on and to include the role of inhomogeneous damage creation along the channel. This is related to the LDD/HDD device architecture used for deep submicron transistors. In addition, it is worthwhile to extend these studies to the next generation of technologies (0.15 μm and beyond) which contains STI and other advanced processing steps (e.g. Cu

metallisation,...). Additional device parameters which are of great potential interest are the low-frequency noise and the series resistance.

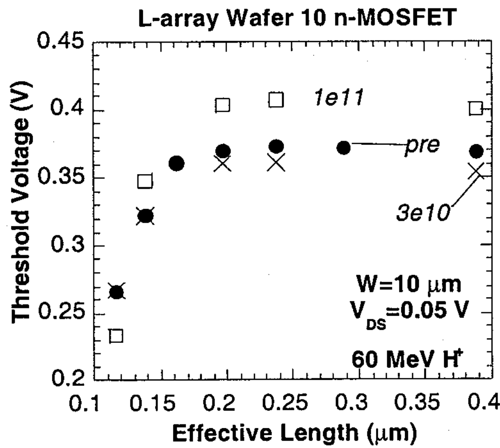


Fig. II.1. Threshold voltage vs effective length for the Wafer 10 n-MOSFETs before and after a 60 MeV proton irradiation.

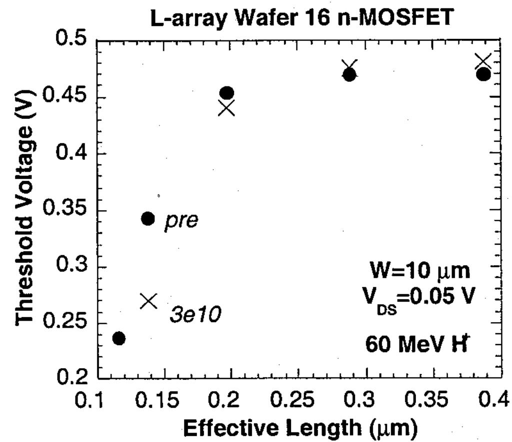


Fig. II.2. Threshold voltage vs effective length for the Wafer 16 n-MOSFETs before and after a 60 MeV proton irradiation.

From the radiation studies of the STI diodes it has become clear that ionisation damage in the trench oxide occurs and affects the surface generation/recombination current of ST-isolated diodes. Given the large impact of peripheral and corner components on the leakage currents of downscaled source/drain junctions, this is an important observation. The advantage of using a diode as a test vehicle is that it is more easy to assess such degradation effects, which should allow a better insight in what is going on. In addition, the study of the bulk current component enables to investigate whether the NIEL concept is useful for such advanced diodes and allows the extraction of the lifetime parameters τ_r and τ_g. Combining lifetime and Arrhenius measurements should give an indication of the dominant generation-recombination (GR) centers in irradiated p-well diodes. This information could then be linked to more spectroscopic studies like DLTS or low-frequency noise.

Another exciting observation, illustrated in Fig. II.3 for different high-energetic particles, is that there appears to be some effect of the STI processing on the radiation damage and response of the diodes. This means that in principle one can optimise the STI module for radiation hardness. The data are in any case useful if this would become an issue later on. A similar approach could be followed in order to study other

advanced processing modules, which are currently under development for future technology generations.

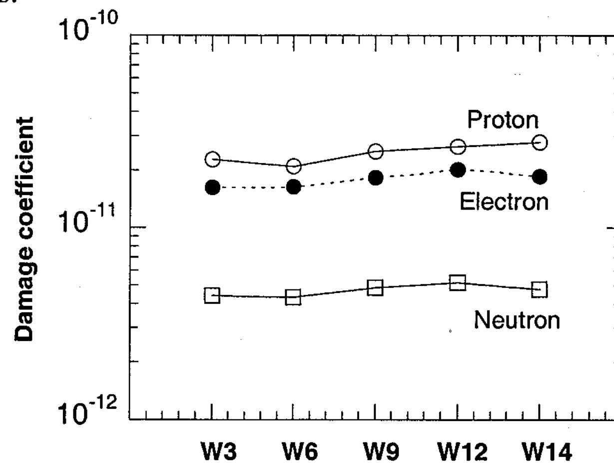


Fig. II.3. Damage coefficients of the irradiated ME1 diodes at –1 V and 25 °C corresponding with the different particles and STI processing splits.

II.2.2 Results Obtained from the Second Round of Proton Radiation Testing – Impact of Nitrided Oxides

As proposed in the original test plan [1], a second irradiation round was carried out on the 0.18 μm test devices. The aim of this was twofold: first, verifying the trends, which were observed during the first round. The results can be found in part I of Deliverable 5 [2]. Second, test structures of a different split were included to investigate the impact of NO oxidation on the radiation hardness of deep submicron CMOS. This NO oxidation is performed to improve the reliability of the ultra-thin gate dielectric and, hence, the lifetime of the devices and will certainly replace standard thermal oxidation for the next technology generation(s). There are also indications in the literature that the radiation hardness of NO oxides should be better than for thermal oxides (OX) (for an overview, see chapter 4 of Ref. 1).

This section of the final report is organized as follows. In a first part, the device and radiation matrix will be described and motivated. Next, the pre-radiation characteristics will be summarized, followed by the post-radiation results. Part 4 discusses the main trends observed and tries to unravel the physical degradation mechanisms. In the final conclusions part, some guidelines for the space operation of

deep submicron CMOS will be formulated and areas requiring further in-depth study will be identified.

II.2.2.1 Sample and Radiation Matrix

II.2.2.1.a Description of the transistor arrays.

The main features of IMEC's 0.18 μm technology have been outlined previously [2]. Here, the relevant details of the splits studied will be briefly reported in Table I. Transistors of 3 wafers have been selected for the second round: wafer 13, 19 and 21 (abbreviated w + number). Wafer 13 has been optimized for the n-MOS devices and should be comparable with w10 of the previous round. Therefore, these devices serve as a reference for the OX condition. Unfortunately, no good OX reference was available for the p-MOS case (w19), so that it was decided to compare with the data of the first round obtained on w16 (OX; p-MOS).

As can be seen, the gate oxide thickness t_{ox} is 3.5 nm in all cases, allowing for a breakdown voltage of at least 2.5 V in absolute value. During the measurements, all biases were kept therefore below 2 V. The isolation was achieved by Polysilicon Encapsulated Local OXidation of silicon (PELOX), which will be replaced by Shallow Trench Isolation (STI) in the next technology generation.

Radiation tests were performed on 24 pins dual-in-line packaged devices. Pure n- or p-MOSFET L-arrays were mounted, with a fixed width (W=10 μm) and a polysilicon gate length L_{poly} varying from 0.48 μm down to 0.18 μm (7 lengths available). The L_{poly}=0.48 μm device serves as a long-channel reference, necessary for the extraction of the effective length and the series resistance, using a modified shift and ratio method [3]. In addition to the active transistors, also non-overlapped field-effect transistors (FETs) have been packaged with dimensions WxL=1000 μmx0.6 μm (both n- and p-FETs). This is to investigate the degradation of the 400 nm thick field oxide (Table II.I).

Table II.I. Technological splits studied in the second irradiation round.

	OX(w13) NMOS	OX(w16) PMOS	NO(w19) PMOS	NO(w21) NMOS
t_{ox}	3.5 nm	3.5 nm	3.5 nm	3.5 nm
gate oxidation	SiO_2 (wet@650 °C)	SiO2 (wet@650°C)	NO-SiO_2	NO-SiO_2
isolation	PELOX	PELOX	PELOX	PELOX
field oxidation thickness	400 nm	400 nm	400 nm	400 nm
p-well implantation	B@(200&55) keV	B@(200&55) keV	B@(200&55) keV	B@(200&55) keV
n-well implantation	P@380 keV & As@120 keV	P@380 keV & As@120 keV	P@380 keV & As@120 keV	P@380 keV & As@120 keV
n-LDD	Yes	--	--	Yes
Nitride spacer	80 nm	80 nm	80 nm	80 nm
RTA	1050°C	1070°C	1070°C	1070°C
Silicidation	Co/Ti (15/8 nm)	Co/Ti (15/8 nm)	Co/Ti (15/8 nm)	Co/Ti (15/8 nm)

II.2.2.1.b Radiation matrix.

The radiation matrix is summarized in Table II.II. In order to compare with round 1 results, it was decided to keep the same proton energy and fluences. The main experimental variables are thus the gate dielectric type (OX or NO) and the device length. This should allow to study the impact of scaling on the device degradation as well. The irradiated FET devices came from one wafer (w21) since there was no difference between the splits with respect to the isolation technology. No bias was applied during the irradiations, which were performed in Louvain-la-Neuve in the week-end of 18 March. Testing was carried out during the following week.

Table II.II. Radiation matrix for the second round, carried out in the week-end of 18 March 2000 in Louvain-la-Neuve. The proton energy was 60 MeV. No bias was applied.

Fluence Φ ($x10^{10}$ cm^{-2})	OX (w13)	NO (w21)	NO (w19)
3.0	LA13-4 LA13-6	LA21-1 LA21-4 FET21-1 FET21-2	LA19-1 LA19-2
10.0	LA13-9 LA13-10	LA21-7 LA21-9 FET21-3 FET21-4	LA19-9 LA19-10

The main static device parameters, i.e. the threshold voltage V_T, the transconductance g_m, the subthreshold swing S and the short-channel threshold voltage lowering $\Delta V_{T@1V}$ were derived according to the previously described procedures [2]. The V_T and g_m for the FETs was determined in linear operation for a fixed drain voltage V_{DS}=±0.25 mV. The series resistance R_S was evaluated starting from the fact that the total channel resistance in the ohmic regime obeys:

$$R_{tot} = V_{DS}/I_D = R_{chan}(L_{eff}) + R_S \quad (1)$$

with R_{chan} the effective length dependent channel resistance and I_D the drain current. Several methods have been proposed in the literature for the extraction of R_S (and of $L_{eff}=L_{poly}-\Delta L$) [3-4]. For more details of the used extraction method, we would like to refer to Ref. 3 and 5.

Finally, in order to investigate the damage mechanisms, the simple charge separation technique by McWhorter and Winokur is applied [6] on the subthreshold characteristics. This consists of separating the radiation-induced change in the threshold voltage ΔV_T in two contributions, namely:

$$\Delta V_T = \Delta V_{ot} + \Delta V_{it} \quad (2)$$

where ΔV_{ot} stands for the oxide-trapped hole charge and ΔV_{it} for the interface-state trapped charge. Usually, these contributions have opposite sign, so that a reduction of V_T (n-MOSFET) points to a dominance of ΔV_{ot}, while the opposite is true if the threshold voltage increases. One reserve which needs to be made is the fact that it is doubtful that the separation technique is still applicable for short-channel devices. One reason is the inhomogeneous distribution of the degradation over the channel area [7]. This will be discussed in more detail in section 4..

II.2.2.2 Pre-Radiation Characterization

II.2.2.2.a n-MOSFETs.

In first order, the pre-rad characteristics are similar as for the first round, so no curves will be shown here [2]. However, one particular feature which we would like to draw the attention on is the cross-over behavior of the device transconductance for an NO MOSFET compared with an OX one. This is illustrated in Fig. II.4. It is clear from this figure that the V_T of the NO devices is lower than for the OX case, which is partially ascribed to the higher fixed oxide charge density associated with the incorporation of a nitrogen layer close to the silicon interface. In addition, the

maximum transconductance is about 10 % lower, which is a drawback for using NO. The reason for this lower g_{mmax} is the enhanced scattering produced by the higher interface and fixed-oxide charge for NO. Finally, at higher gate overdrive voltages (V_{GS}-V_T) the g_m curve for NO crosses the one for OX, in agreement with literature [1,8]. The reason for this behaviour is thought to originate from a different dependence of the interface- and oxide-trap scattering on the vertical electric field [8]. Similar results are observed for the p-channel transistors [5].

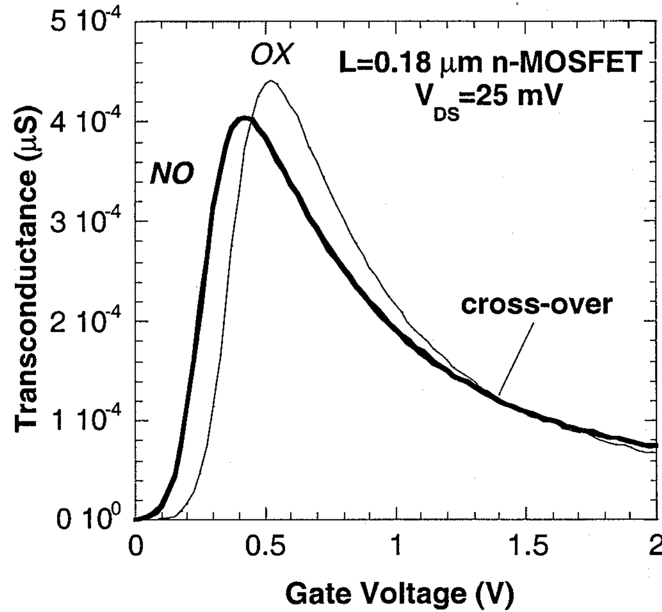
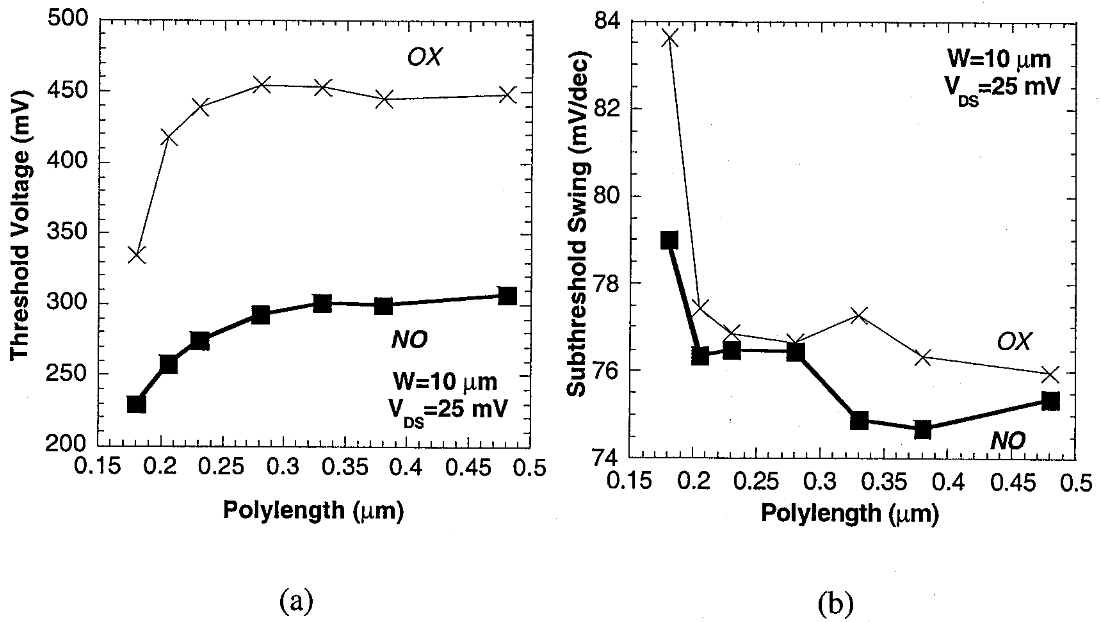


Fig. II.4. Comparison of the transconductance for a 10 μmx0.18 μm n-MOSFET in linear operation (V_{DS}=0.025 V) for an OX (w13) and an NO device (w21).

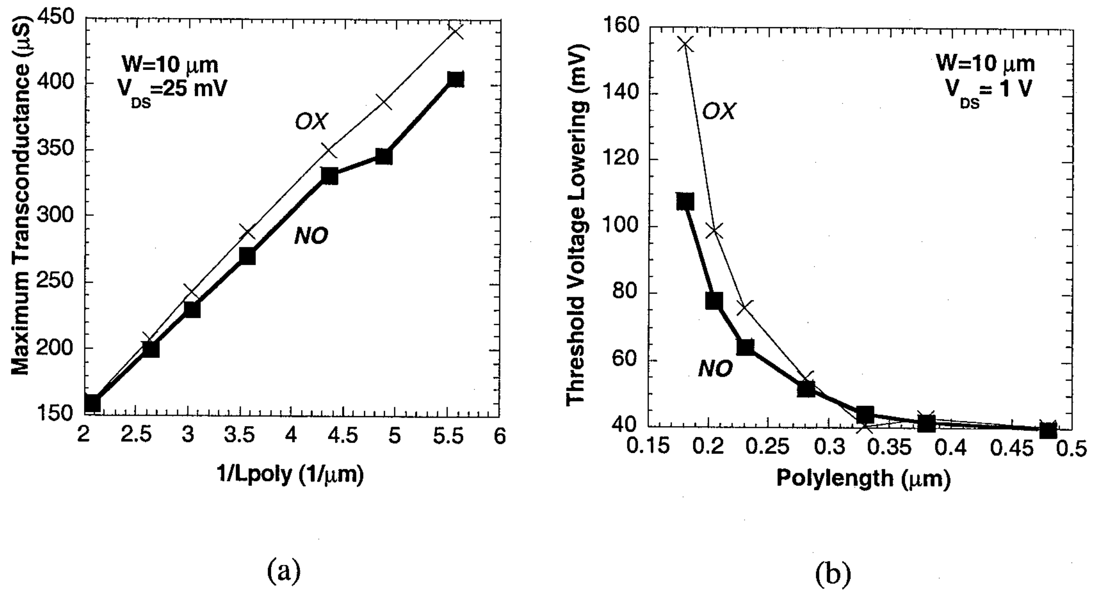
The n-MOSFET parameters before irradiation are summarized in Figs II.5 and Fig. II.6. From Fig. II.5a it is clear that the threshold voltage for the NO devices is significantly lower. At the same time, the reverse short-channel (RSC) effect is suppressed, while the V_T roll off is smaller in absolute value but smeared out over a larger polysilicon gate length range. The reduction of the RSC effect is probably related to the effect nitrogen has on the diffusion of B and its accumulation close to the source/drain extensions.

S is smaller for NO compared with OX (Fig. II.5b) and shows a smaller variation with L_{poly}. The same goes for the g_{mmax} (Fig. 1.3a) and the DIBL effect (Fig. II.6b).



(a) (b)

Fig. II.5. Threshold voltage (a) and subthreshold swing (b) as a function of the polylength for the OX and NO n-MOSFETs. V_{DS}=25 mV.



(a) (b)

Fig. II.6. Maximum transconductance (a) and threshold voltage reduction (DIBL) (b) as a function of the polylength for the OX and NO n-MOSFETs.

Finally, in Fig. II.7 the extracted series resistance is represented, showing a typically 20 Ω higher R_S value for the NO case. The reduction of R_S with smaller length is probably related to the gate voltage dependence of R_S, on the one hand, and

the reduction of the threshold voltage for smaller L_{poly}, on the other. It is known that R_S follows roughly a $1/(V_{GS}-V_T)$ variation for submicron MOSFETs [4].

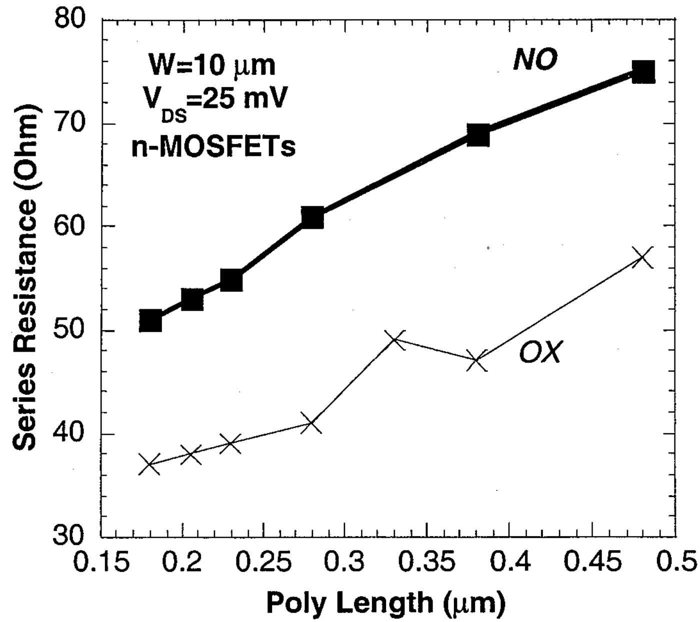
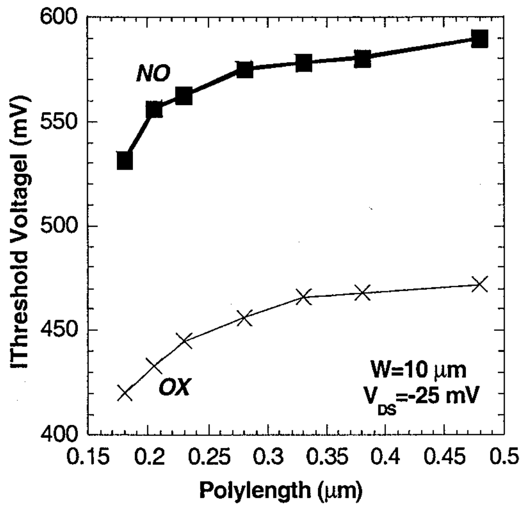
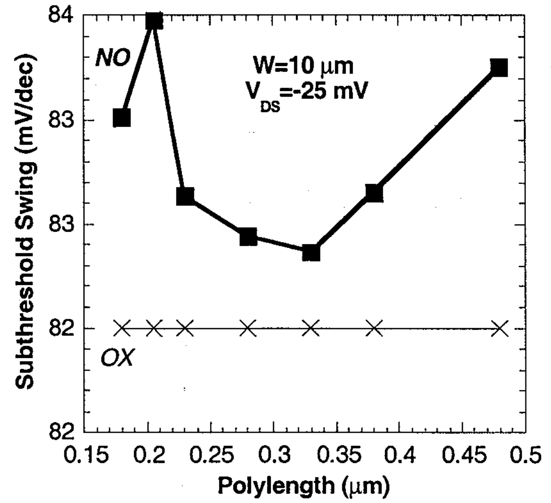


Fig. II.7. Series resistance versus polylength for the NO and OX n-MOSFETs in the ohmic regime.

II.2.2.2.b p-MOSFETs.

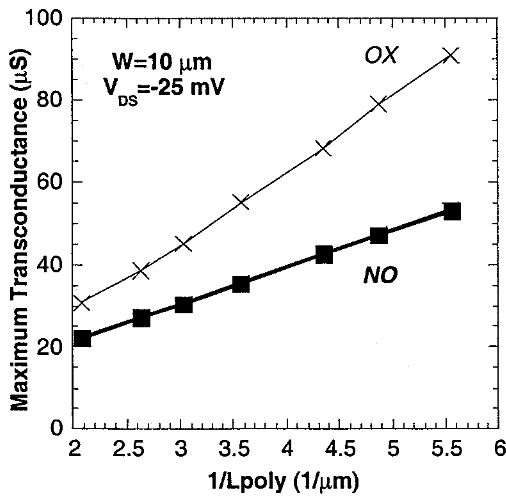
The main static parameters of the p-MOSFETs studied are summarised in Figs II.8 and II.9. The threshold voltage of NO devices is about 100 mV more negative compared with OX (Fig. II.8a). Again, the higher fixed charge is probably responsible for this effect. The subthreshold swing is also higher for NO, suggesting a higher density of interface traps (Fig. II.8b). This causes more interface scattering and a lower mobility and, hence, a lower g_{mmax} (Fig. II.9a). The NO p-transistors also show a higher DIBL effect in Fig. II.9b, although the difference reduces for smaller L_{poly}. No series resistance has been extracted for the p-MOSFETs.

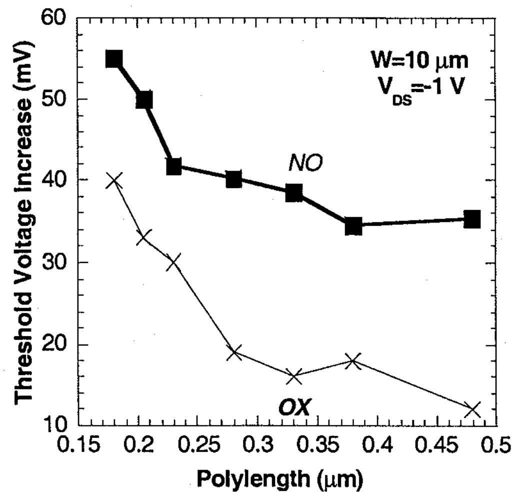




(a) (b)

Fig. 1II.8. Threshold voltage (a) and subthreshold swing (b) as a function of the polylength for the OX and NO p-MOSFETs. V_{DS}=-25 mV.





(a) (b)

Fig. II.9. Maximum transconductance (a) and threshold voltage increase (b) as a function of the polylength for the OX and NO p-MOSFETs.

II.2.2.2.c FETs.

The FET devices show overall a high V_T (>±50 V) before irradiation. In the next section, mainly the proton-radiation induced changes will be discussed.

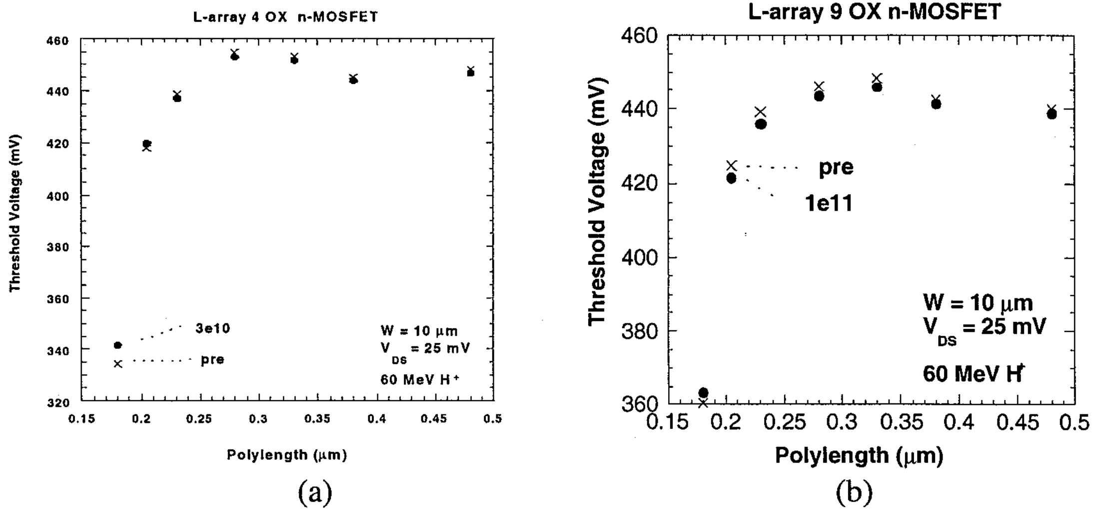
II.2.2.3 Post-Radiation Characteristics

II.2.2.3.a n-MOSFETs.

As can be derived from Table II.II, for each fluence and process split 2 arrays have been irradiated and characterised in order to check the reproducibility of the results. In most cases, similar results have been obtained, within the measurement accuracy. Figure II.10 compares the threshold voltage of the OX n-MOSFETs before and after a 3x (a) and 10×10^{10} proton/cm^2 (b) 60 MeV proton exposure, versus the polylength. Note first of all that the observed changes are rather small, which is expected for thin-gate devices [1,9]. It is clear from the figure that V_T reduces after irradiation for the longer channels, while a slight increase is found for the shorter ones. Such a behaviour was also found for the Wafer 10 devices of the first round, after 3×10^{10} cm^{-2} (Fig. I.50 of Ref. 2). There is a cross-over between the pre- and post-rad V_T curve situated at L_{poly}=0.22 μm (3×10^{10} ptoton/cm^2) and 0.19 μm for 10^{11} proton/cm^2, which thus shifts to lower lengths for higher fluences. A similar conclusion was reached previously, pointing to the existence of an optimal channel length for the n-MOSFET, corresponding to a negligible V_T shift. This length lowers for higher fluences Φ. Although the V_T shift slightly increases with Φ, the change is not really proportional to the fluence.

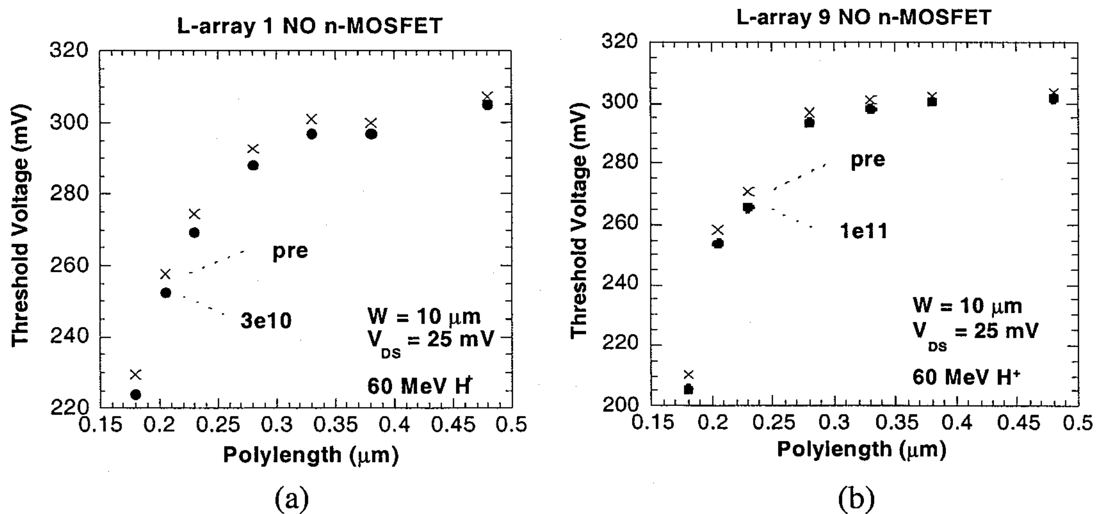
For NO n-MOSFETs on the other hand, no such a cross-over is observed in Fig. II.11. Here, a reduction of V_T is found for all lengths, which becomes higher for the shorter transistors at both fluences. The threshold voltage reduction is also more pronounced for NO compared with OX (compare e.g. Fig. II.10a and II.11a). From a perspective of V_T change, OX shows a better radiation resistance than NO, which is

rather surprising. All obtained results are summarized in Fig. II.12a (OX) and b (NO) and Fig. II.13.



(a) (b)

Fig. II.10. Threshold voltage after 3.0x (a) and $10x10^{10}$ cm^{-2} (b) 60 MeV proton irradiation for an array of OX n-MOSFETs. V_{DS}=25 mV.



(a) (b)

Fig. II.11. Threshold voltage after 3.0x (a) and $10x10^{10}$ cm^{-2} (b) 60 MeV proton irradiation for an array of NO n-MOSFETs. V_{DS}=25 mV.

The subthreshold swing of the OX n-MOSFETs shows a slight increase after both 60 MeV fluences studied (Fig. II.14). The increase seems to become smaller for shorter channels, reflecting more or less the V_T behaviour. This indicates that the radiation-induced density of interface traps shows length dependence, increasing for shorter channels. In contrast, S for NO devices shows even a reduction after

irradiation for long channels, while a cross-over occurs for shorter transistors (Fig. II.15). It seems that complementary V_T and S behaviour is found for the OX versus NO n-MOSFETs after 60 MeV proton irradiation, whereby the V_T behaviour is more favorable for OX, while the subthreshold swing is better for NO. It also demonstrates that there exists a delicate balance between interface-state creation and trapped-hole charging of the thin gate oxide.

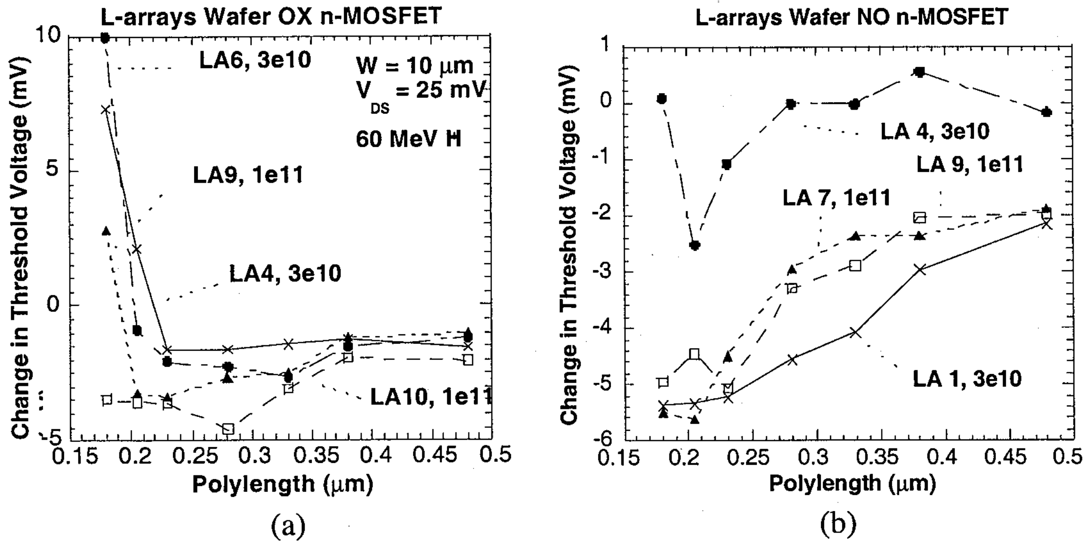


Fig. II.12. Threshold voltage change for the OX (a) and NO (b) n-MOSFETs for all arrays studied. V_{DS}=25 mV.

The maximum transconductance shows in both cases a more or less similar reduction after irradiation for OX (Fig. II.16) or NO (Fig. II.17) arrays. The g_{mmax} remains about 10 % smaller for NO compared with OX. This is shown more explicitly in Fig. II.18, comparing the transconductance curve for a 0.18 µm OX and NO n-MOSFET after $3x10^{10}$ cm^{-2} (a) and 10^{11} cm^{-2} (b). Comparing both figures, a tendency is observed for the crossing point to shift to lower gate biases, for higher Φ. This could point to a different impact of the transverse electric field on the mobility, although a careful analysis also needs to account for the different V_T behaviour in both cases.

It is finally shown in Fig. II.19 and II.20 that there seems to be a slight increase in the effective channel length and series resistance for the n-MOSFET after 10^{11} proton/cm^2 irradiation. This points to role of the charge trapping in the nitride

spacers on top of the LDD regions. It also suggests that especially for the shorter transistors, the radiation-induced damage may be highly non-uniform along the channel and might be concentrated in the source/drain edges (spacers) of the structure and not in the bulk of the gate oxide (channel region).

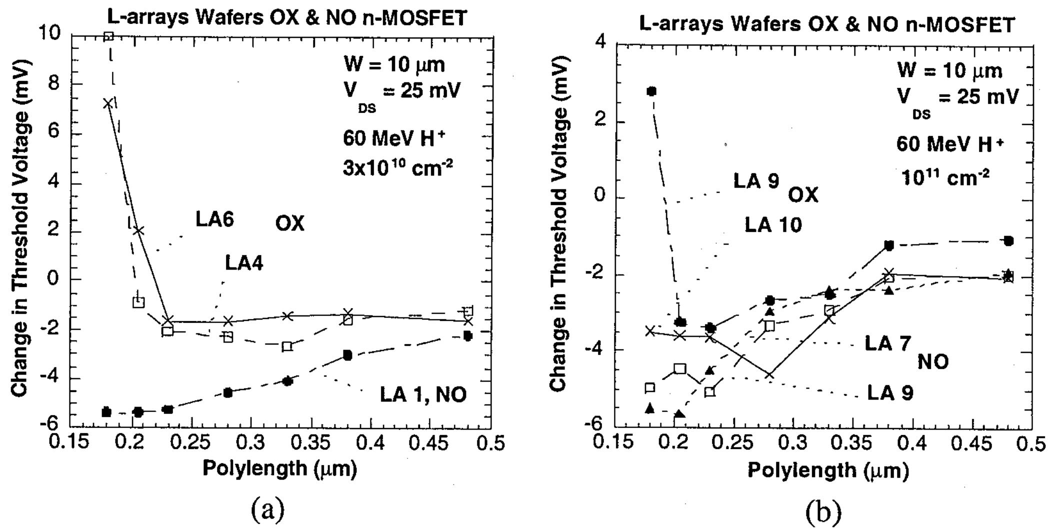


Fig. II.13. Threshold voltage after 3.0x (a) and $10x10^{10}$ cm^{-2} (b) 60 MeV proton irradiation for the NO and OX n-MOSFET arrays. V_{DS}=25 mV.

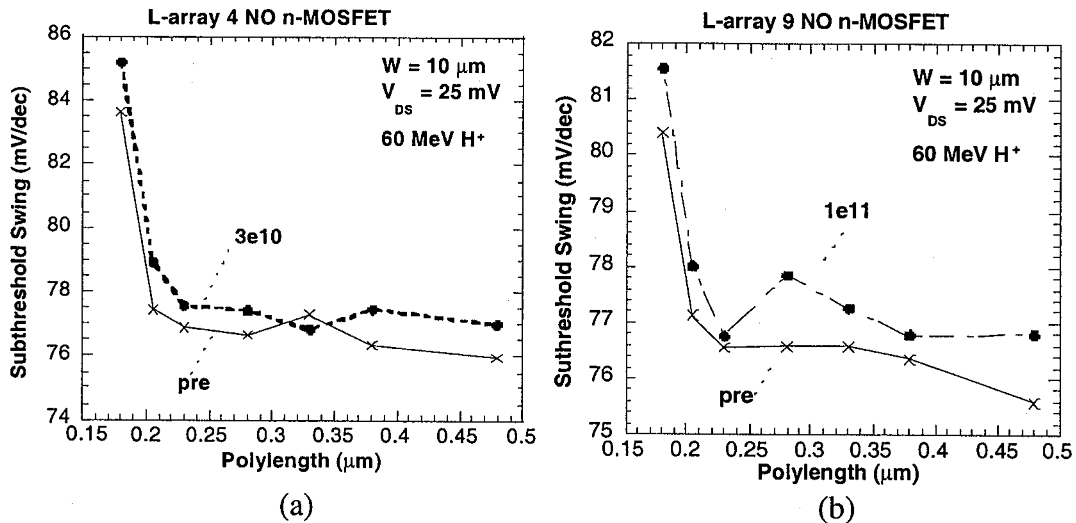
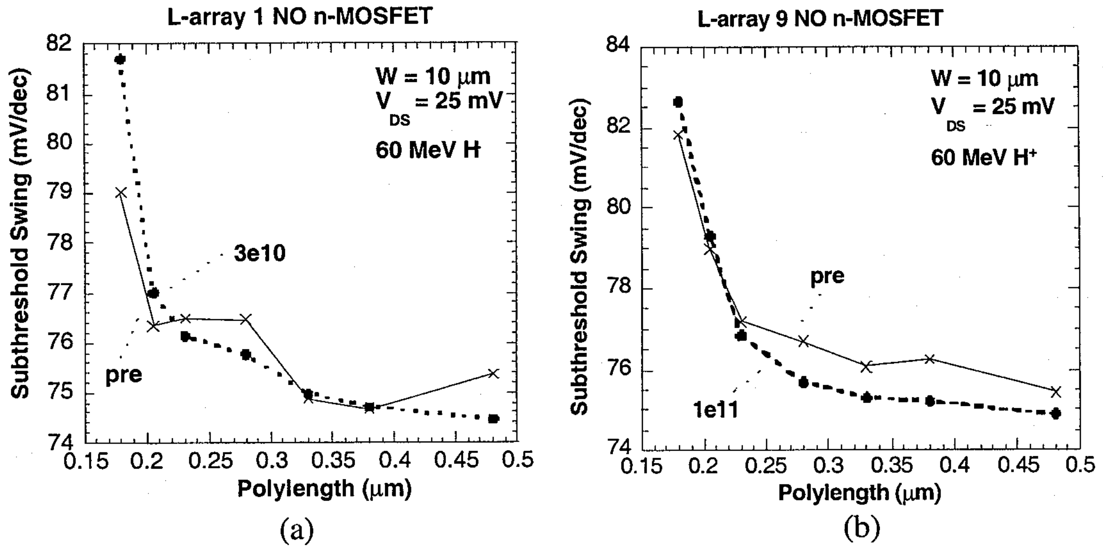
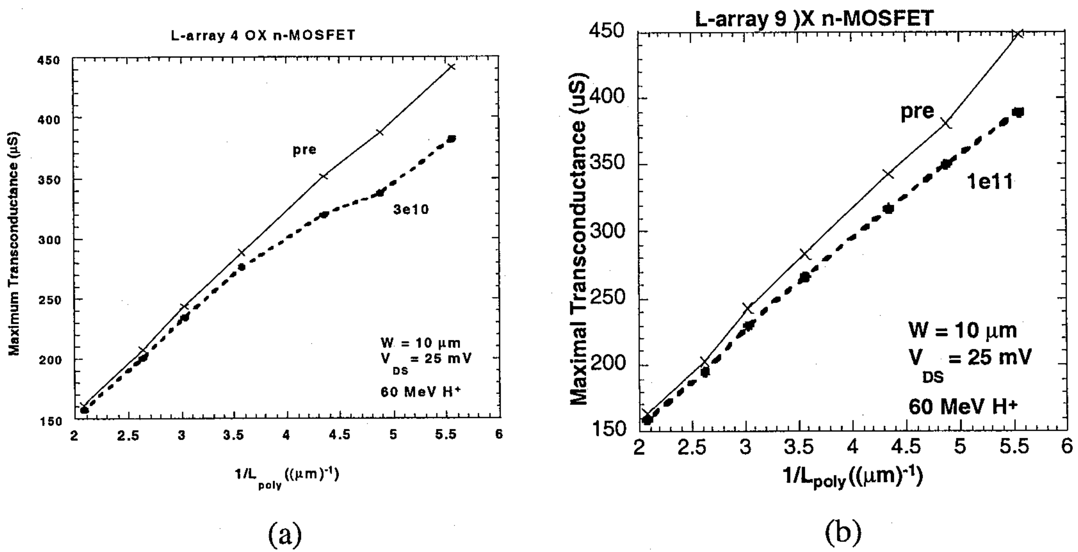


Fig. II.141. Subthreshold swing after 3.0x (a) and $10x10^{10}$ cm^{-2} (b) 60 MeV proton irradiation for an array of OX n-MOSFETs. V_{DS}=25 mV.



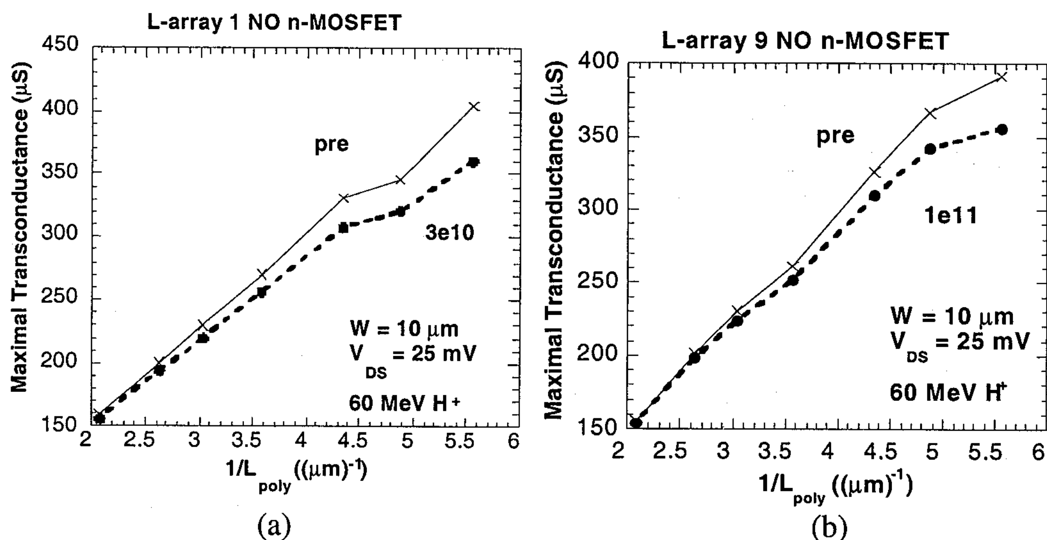
(a) (b)

Fig. II.15. Subthreshold swing after 3.0x (a) and 10×10^{10} cm^{-2} (b) 60 MeV proton irradiation for an array of NO n-MOSFETs. V_{DS}=25 mV.



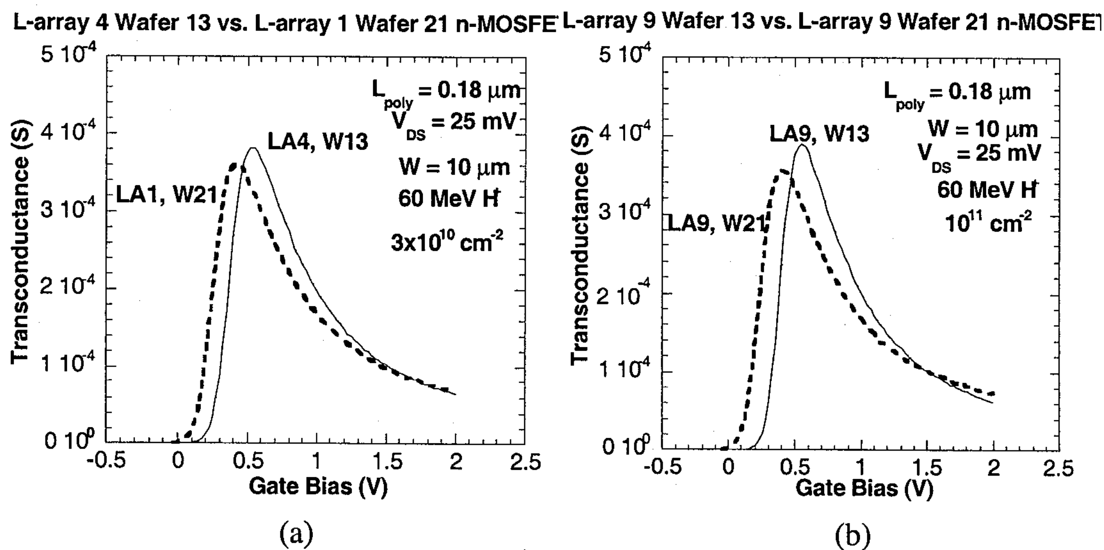
(a) (b)

Fig. II.16. Maximum transconductance after 3.0x (a) and 10×10^{10} cm^{-2} (b) 60 MeV proton irradiation for an array of OX n-MOSFETs. V_{DS}=25 mV.



(a) (b)

Fig. II.17. Maximum transconductance after 3.0x (a) and $10x10^{10}$ cm^{-2} (b) 60 MeV proton irradiation for an array of NO n-MOSFETs. V_{DS}=25 mV.



(a) (b)

Fig. II.18. Transconductance versus gate bias for an NO and OX transistor with L_{poly}=0.18 µm and after 3x (a) and $10x10^{10}$ cm^{-2} 60 MeV protons. V_{DS}=25 mV.

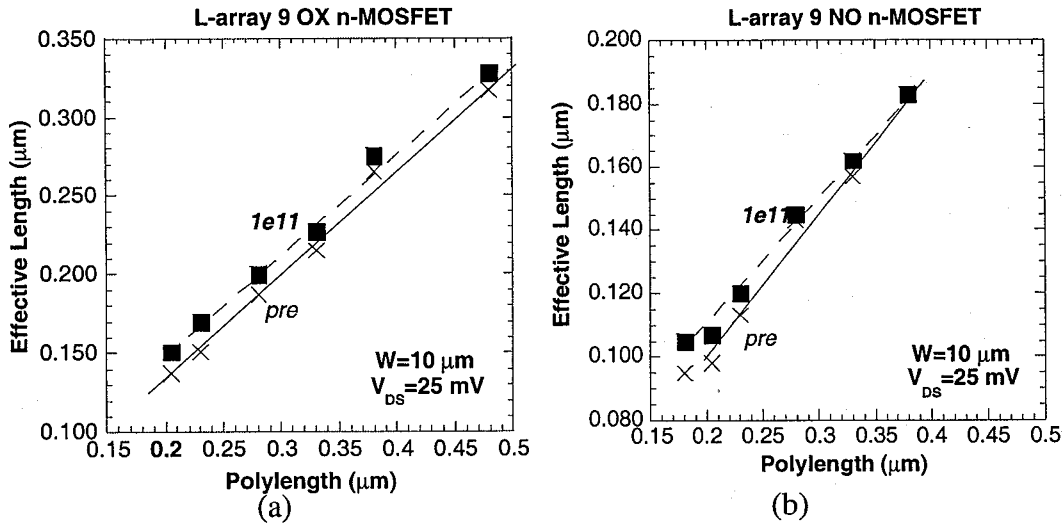


Fig. II.19. Effective channel length after 10^{11} cm^{-2} 60 MeV protons for an OX (a) and an NO (b) n-MOSFET array. V_{DS}=25 mV.

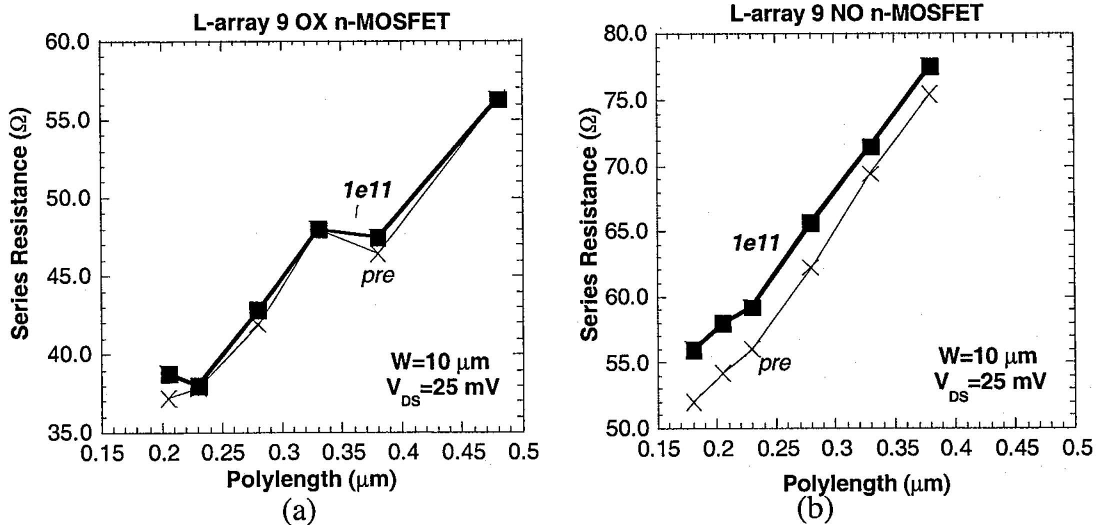


Fig. II.20. Series resistance after 10^{11} cm^{-2} 60 MeV protons for an OX (a) and an NO (b) n-MOSFET array. V_{DS}=25 mV.

It should finally be remarked that LA21-4 (NO) showed very little changes after irradiation. The sample was mounted at the edge of the printed circuit board during the irradiations, so that it is not unlikely that it was outside the proton beam during the exposures.

II.2.2.3.b n-MOSFETs.

There is no clear trend in the change of the threshold voltage of the irradiated NO p-MOSFETs in Fig. II.21, if any. The same conclusion was reached for the OX p-

MOSFETs in round 1 [2] (see also Fig. II.22b). Interestingly, the subthreshold swing of the NO p-MOSFETs shows a slight reduction after irradiation (Fig. II.23), however, without a clear length-dependence. This stands in contrast with the case for the OX p-MOS transistors of round 1, shown in Fig. II.24a. The transconductance shows a slight reduction for OX (Fig. II.24b) and a negligible change for NO (Fig. II.25). Overall, the device degradation of p-MOSFETs is small both for OX and NO, so that no clear conclusions can be drawn with respect to the radiation resistance of the NO split, compared with OX.

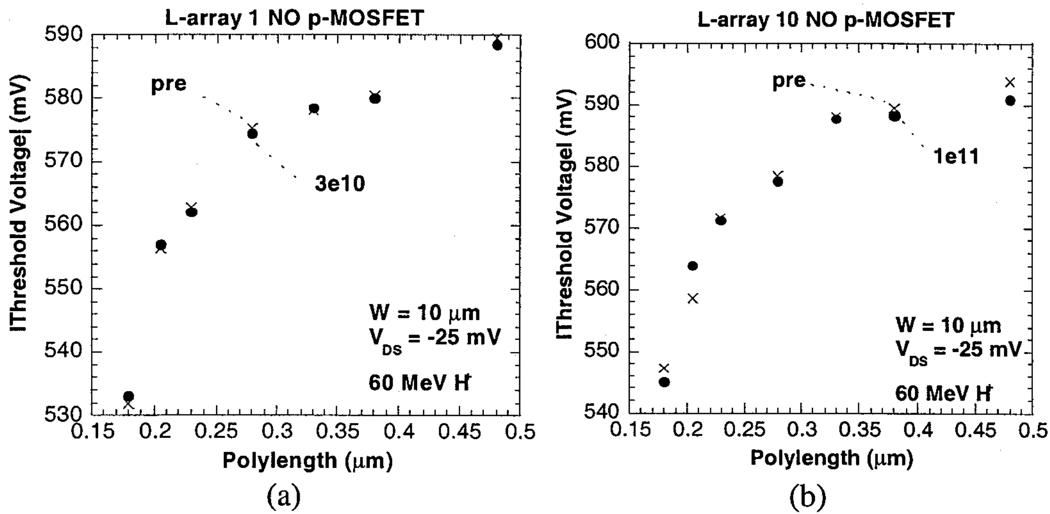


Fig. II.21. Threshold voltage after 3.0x (a) and 10×10^{10} cm^{-2} (b) 60 MeV proton irradiation for an array of NO p-MOSFETs. V_{DS}=-25 mV.

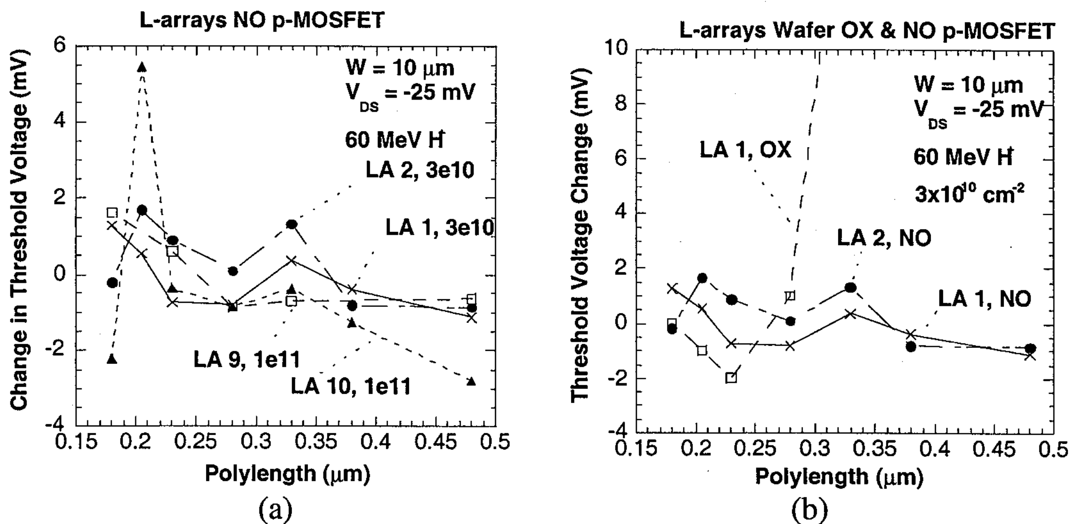


Fig. II.22. Threshold voltage change for the NO (a) and for the NO and OX p-MOSFET arrays after 60 MeV proton irradiation. V_{DS}=-25 mV.

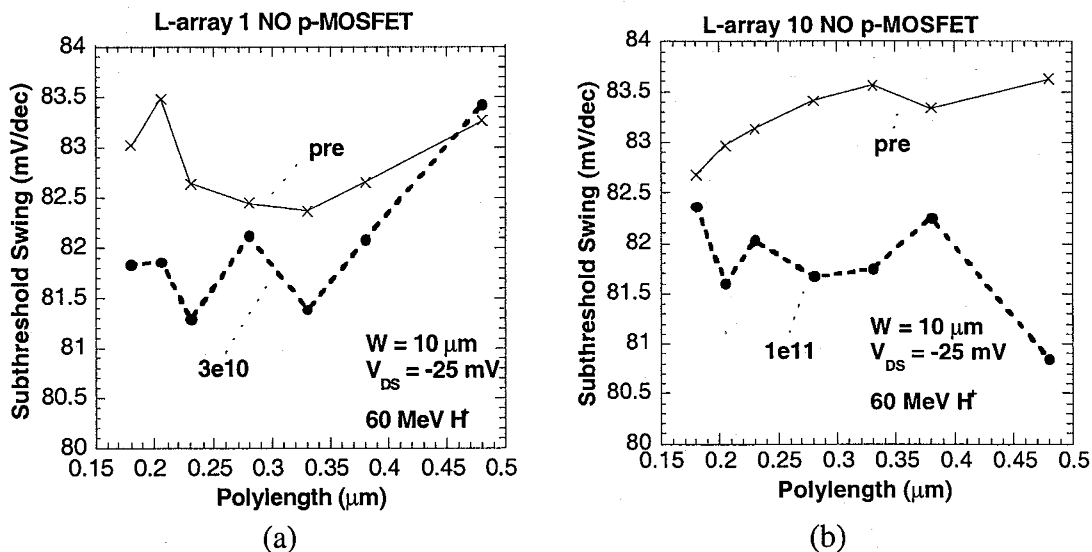


Fig. II.23. Subthreshold swing after 3.0x (a) and $10x10^{10}$ cm^{-2} (b) 60 MeV proton irradiation for an array of NO p-MOSFETs. V_{DS}=-25 mV.

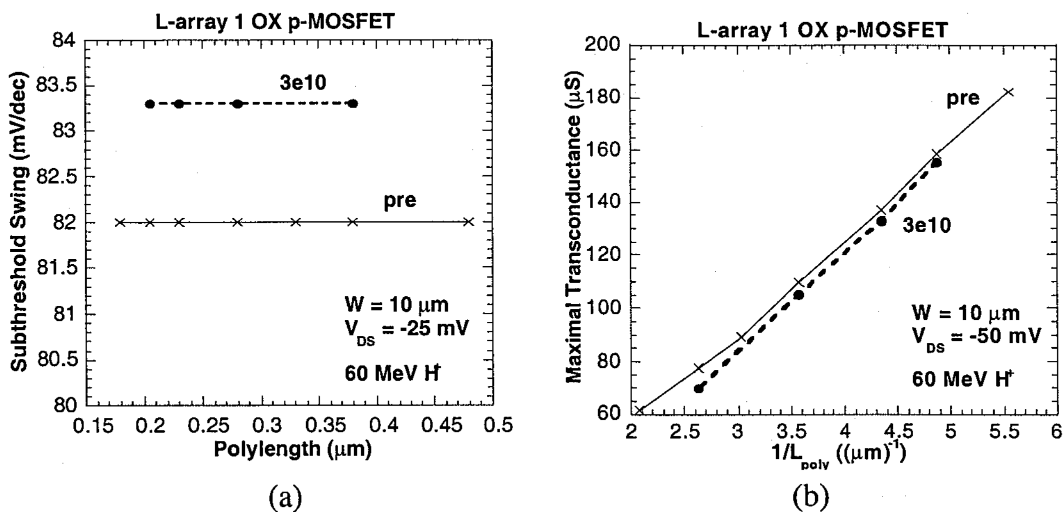


Fig. II.24. Subthreshold swing (a) and max. transconductance (b) after a $3.0x10^{10}$ cm^{-2} 60 MeV proton irradiation for an array of OX p-MOSFETs. V_{DS}=-25 mV.

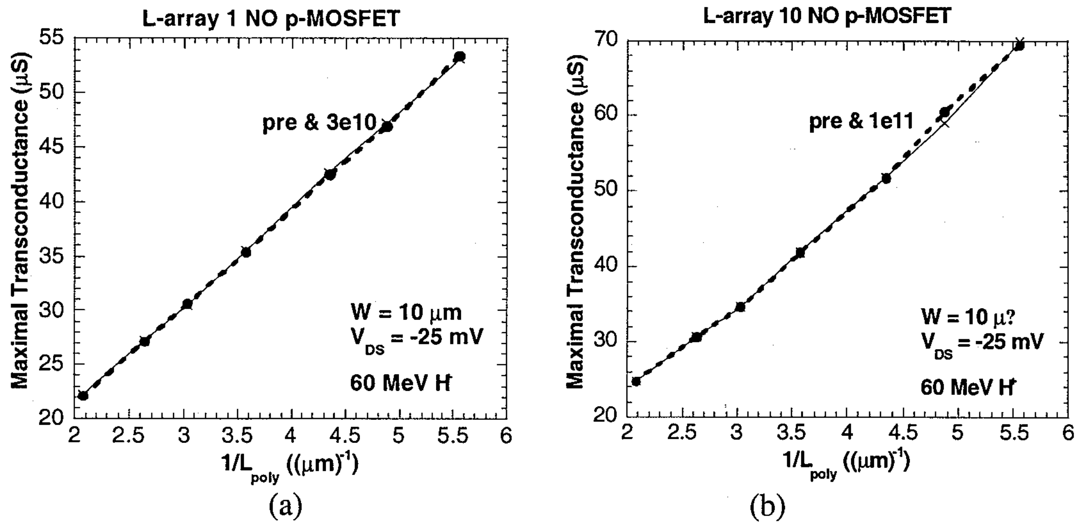


Fig. II.25. Maximum transconductance after a 3.0x (a) and $10x10^{10}$ cm^{-2} (b) 60 MeV proton irradiation for an array of NO p-MOSFETs. V_{DS}=-25 mV.

II.2.2.3.c FETs.

The changes of the field-effect transistor parameters are summarized in Table II.III. Overall, a mixed behavior is observed as a function of the fluence. The most consistent changes are for the V_T of the n-FETs, showing a pronounced increase, which is higher for the highest fluence. However, the change in the V_T is certainly not enough to turn on the parasitic edge devices. It can be concluded that for the fluence range studied, the FETs can certainly withstand the induced damage. In addition, it seems very unlikely that the degradation of the active transistors described above is related to the edge transistors and can, therefore, be ascribed to the channel region.

Table II.III. 60 MeV proton radiation-induced changes of the static device parameters in linear operation of the FETs of wafer 21 (NO).

FET type	Proton Fluence ($x10^{10}$ cm^{-2})	Δg_{mmax} (mS)	ΔV_T (mV)	ΔS (mV/dec)
NFET	3.0	-0.045	-1.24	-0.07
NFET	3.0	-0.027	-0.78	-0.08
NFET	10.0	-0.046	-2.10	0.14
NFET	10.0	-0.025	-2.63	0.23
PFET	3.0	-0.008	0.70	0.018
PFET	3.0	-0.410	8.33	0.001
PFET	10.0	0.082	-3.57	0.014
PFET	10.0	-0.017	-2.24	0.073

II.2.2.4. Discussion

In order to interpret the obtained results on V_T, the charge-separation technique of McWhorter and Winokur [6] has been applied. This assumes that the displacement damage produced by the high-energy protons does not cause any measurable change in the channel doping density. From the measurements of the capacitance-voltage characteristics on the 60 MeV proton irradiated STI diodes (see part II), it is indeed concluded that at least the p-well doping density is not affected up to a fluence of 10^{11} cm^{-2}. However, in order to investigate this more closely, it is necessary to study the body factor before and after irradiation. This can be achieved by measuring V_T as a function of the reverse substrate bias. From the results of Table II.IV, a few conclusions can be drawn. For the OX n-MOSFETs, ΔV_{ot} is in the range of –1 to –5 mV. For the 0.48 μm transistors, it is the largest contribution to the total threshold voltage change, while for the 0.18 μm device, $|\Delta V_{ot}| < |\Delta V_{it}|$. This explains the cross-over behaviour described above.

II.IV. ΔV_{ot} and ΔV_{it} contributions to the total V_T change, obtained from the charge separation technique [6].

L_{poly} (Fluence) (μm)	NO ΔV_{ot} (mV)	NO ΔV_{it} (mV)	OX ΔV_{ot} (mV)	OX ΔV_{it} (mV)
0.48 (3.0)	-1.16	-0.41	1.25	-3.41
0.48(10.0)	-2.47	1.43	-168.7	166.7
0.18 (3.0)	-3.56	10.85	-14.97	9.61
0.18 (10.0)	-5.15	7.95	-169.4	164.4

For NO, on the other hand, the charge-trapping contribution is larger than for the OX case, which is reasonable, given the expected higher density of oxide traps. Unfortunately, also ΔV_{it} is much higher, which is not expected. From the literature it is known that the formation of interface traps is suppressed in nitrided oxides [1,8]. This is believed to be related to the fact that the nitrogen close to the interface forms a diffusion barrier for hydrogen and, therefore, reduces the formation of new interface traps. It is not clear why the opposite is seen here. However, it should be noted that the NO oxidation is not optimised yet, even before irradiation. This follows for example from low-frequency noise studies where a 10 times higher noise magnitude (i.e. oxide trap density) is found. Overall, the total ΔV_T is still dominated by the oxide-trapped charge, explaining the negative V_T shift in this case.

Related to the results of Table II.IV, a few comments have to be made. First, the total V_T shift is generally quite small, so that the error on the separated contributions is quite large. In a few cases, highly questionable results have been

obtained [5]. A second point is that for 3.5 nm devices one normally does not expect oxide charge trapping, singe this is smaller than the total tunneling distance of 6 nm. The question then rises regarding the meaning of the extracted ΔV_{ot}? Of course, a MOS transistor is more complex than a plain thin-gate MOS capacitor, so that one can expect a different degradation behaviour. One important factor with respect to short-channel transistors (with LDD) is the fact that the damage is most likely not uniformly distributed along the channel [7]. It has been demonstrated in the past that the source/drain edge regions show a different damage behaviour than the channel region. This can be attributed to a different electric field near the junctions, differences in the pre-rad gate-oxide defects and above all, the presence of the LDD and (nitride) spacers. Of course, these edge effects will become more pronounced the shorter the channel is, which may explain the short-channel behaviour reported in rounds 1 and 2.

From this, it is concluded that the results shown in Table II.IV should be handled with great care and are in first instance rather qualitative. For a true charge separation, taking account of the channel inhomogeneity, more sophisticated techniques like the Gate-Induced Drain Leakage (GIDL) current technique and modified charge-pumping have to be applied [7], which are outside the scope of the present work.

II.2.2.5. Conclusion and Outlook

Summarizing, it has been shown that NO oxidation yields a different radiation response, compared with standard furnace oxidation. Overall, the results on n-MOSFETs seem to indicate *both* a larger oxide charge trapping and interface-state creation. The former is expected, because of the presence of a larger density of fixed oxide traps and charges before irradiation and related to the presence of nitrogen. The enhanced interface trap creation is unexpected and should be studied in more detail and with more sophisticated methods, in order to make sure that it is a real effect and not an artifact of the analysis method. Anyhow, the cross-over behavior with length, observed for the threshold voltage V_T (OX transistors) or for the transconductance S (NO transistors) can only be explained by considering the contribution of at least two mechanisms, which have a different length dependence. For the moment, effects

related to displacement damage or to the field-oxide edges seem to be rather unlikely, but can not be completely ruled out.

A second important observation is that the radiation damage show a consistent length-dependence, which can also be considered a radiation-induced short-channel effect. In order to explain it, the contribution of at least two opposite mechanisms is necessary (cross-over effects), whereby interface-state generation and oxide charge-trapping are the most obvious ones. However, another crucial factor is the inhomogeneity of the channel and its response to the radiation damage.

For future radiation-damage studies in short-channel transistors and technologies it could be worthwhile to study for example:

i) The body factor before and after irradiation, by measuring the V_T as a function of the substrate bias.
ii) The GIDL current, which is a useful technique to separate interface-state and oxide-charge contributions to the degradation, especially close to the source/drain junctions.
iii) Low-frequency noise is also a useful technique to obtain more information on the oxide traps close to the interface.
iv) So far, there is no clear evidence for electron trapping in the NO dielectric nor in the nitride spacer. This needs to be further looked into.

As it is expected that the NO gate oxide will replace standard oxide in the next CMOS generation, further radiation-studies are highly desirable, especially if the NO module continues to be improved. The same applies for the STI module, which will be incorporated in the 0.15-0.13 μm technology at IMEC.

II.2.2.6. Acknowledgements

J. Hermans is thanked for performing the second round electrical characterisation in the frame of his Masters thesis. G. Berger kindly performed the irradiations. Finally, the members of the CMOS group are acknowledged for providing the wafers and the

relevant technological information; in particular we wish to mention the contributions of E. Augendre, G. Badenes and R. Rooyackers.

II.2.2.7 References

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II.2.3 Results Obtained from the Second Round of Proton Radiation Testing – Irradiation effects in Shallow Trench Isolated Diodes

One of the key elements in future down-scaled CMOS technologies is the device isolation [1-4]. Recent reports indicate that it is no longer intrinsic channel damage which dominates the radiation response, but rather the leakage related to the devices edges (isolation regions). This is certainly the case for shallow trench isolation (STI), where the edge leakage is a sensitive function of the processing details [1-4]. This was also observed in a first irradiation round, where the effect of high-energy electron, neutron and proton damage was studied, by means of the degradation of the curren-voltage (I-V) and capacitance-voltage (C-V) characteristics of junctions, surrounded by STI [5].

In order to further study displacement and ionisation damage effects in these devices, an additional proton-irradiation round was undertaken. The 8 MeV proton irradiations took place on March 8 at Demokritos. No bias was applied and the particle fluence was $5x10^{11}$, $5x10^{12}$ and $5x10^{13}$ cm^{-2}. Combined with the earlier 60 MeV H^+ (Cyclone – Louvain-la-Neuve) and 20 MeV H^+ irradiations (Takasaki JAERI) allows a comparison with the Non Ionising Energy Loss (NIEL) parameter [6-7]. The I-V and C-V characteristics of the junctions are analysed using the recently developed methodology [8-9]. For more details on the device technology and layout, we refer to the report of the first round [5].

II.2.3.1. Post Proton Irradiation Characterization

After proton irradiation, a clear increase of both the forward and reverse current is observed in Figs II.26a and II.26b, corresponding with 20 and 8 MeV proton irradiations, respectively. However, for sufficiently large forward bias, the forward current in Fig. II.26a reduces after irradiation, indicating an increase of the series resistance. This could for example result from a deactivation of the boron concentration ([B]) in the p-well. High-frequency (100 kHz) C-V measurements support this idea: the capacitance of the reversely biased diodes reduces with proton fluence. A lowering by a factor 2 has been reported after a 10^{13} cm^{-2} 20 MeV proton irradiation, corresponding to a reduction by a factor 4 of the active dopant

concentration in the p-well [5]. This deactivation is thought to proceed according to the interaction with radiation-induced interstitials (I):

$$B_s + I \rightarrow Si + B_i \qquad (1)$$

whereby a substitutional B atom (B_s) is kicked out of its lattice site by a silicon interstitial, generating a mobile and inactive B interstitial (B_i). B_i can subsequently react with other impurities, generating more stable radiation complexes like B_iB_s, B_iO_i, B_iC_s,....

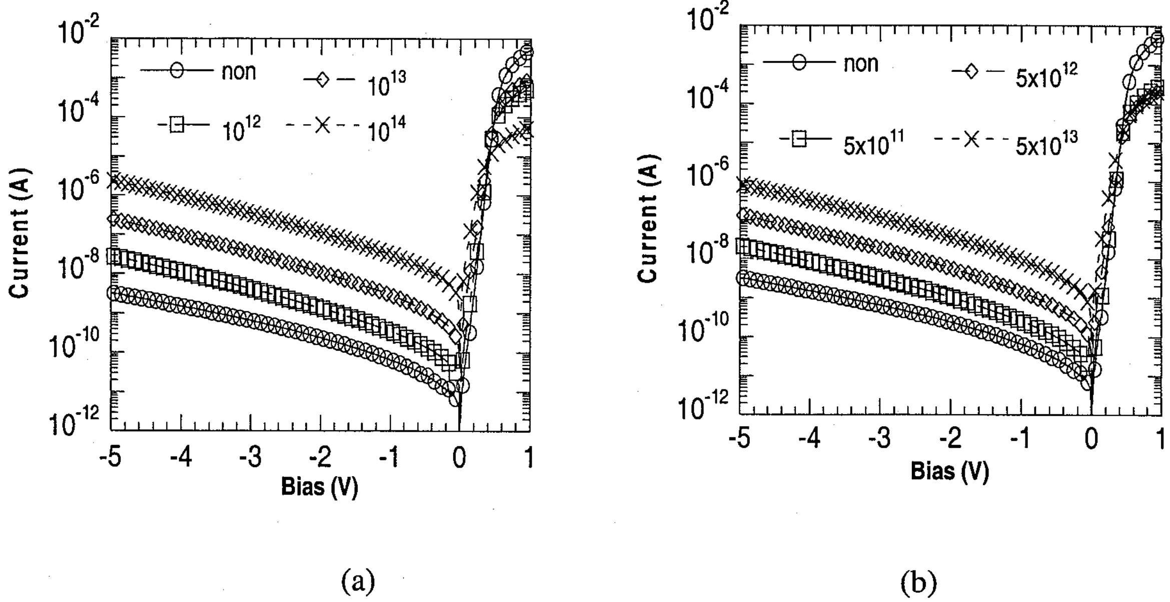

Fig. II.26. I-V characteristics of a 10 mm^2 n$^+$-p diode after 20 MeV proton irradiation, for different fluences and 25°C (a) and after 8 MeV proton irradiation (b).

The increase in reverse current for a large area diode scales roughly with the fluence Φ, as shown more explicitly in Fig. II.27 for a V_R=-1 V. The slope of the straight-line fit to the data points gives the reverse-current damage coefficient K_I, defined by:

$$K_I = \partial I_R/\partial\Phi \approx \Delta I_R/\Delta\Phi \qquad (2)$$

which is proportional to the generation-lifetime damage coefficient $K_{\tau g}$ in first instance. The increase of the leakage current and of the forward current in Fig. II.27 is

mainly due to a decrease of the generation and recombination lifetime, respectively. However, the deactivation of the boron will in turn cause an increase of the depletion width for the same reverse bias. This should eventually cause a non-linear change in I_R at the largest fluences.

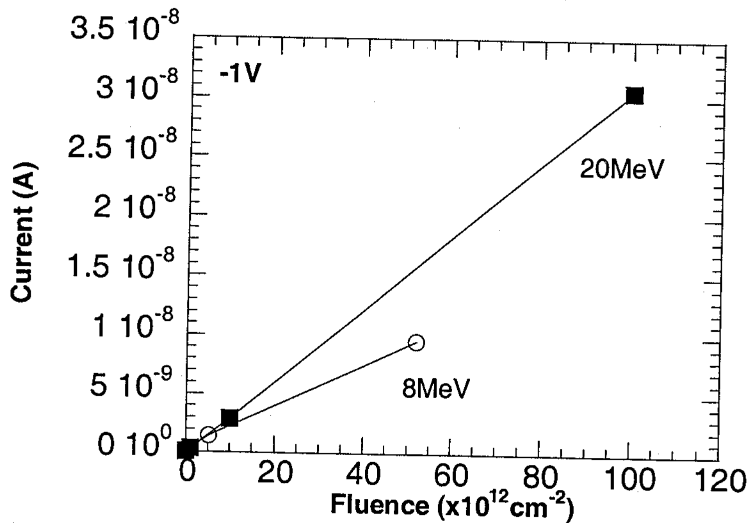

Fig. II.27. I-V characteristic of 8 MeV and 20 MeV proton-irradiated SQ1 STI diodes in function of the fluence, corresponding with a V_R=-1 V and 25°C.

The damage coefficients corresponding with the data of Fig. II.27 are summarized in Table II.V and compared with the NIEL parameter [7]. Surprisingly, no proportionality is observed between K_I and NIEL, which is expected if the main degradation mechanism is due to lattice damage in the bulk. One possible explanation may be the occurrence of ionisation damage in the STI oxides, which causes an increase of the peripheral leakage current. Evidence for that is provided in Fig. II.26a or II.27b for example, showing the development of a clear non-ideal recombination component in forward operation at low bias, which is generally associated with interface states. Therefore, we should compare the NIEL with the damage coefficient for the volume leakage current, which can be separated by combining the data of different-geometry diodes [8-9]. Unfortunately, for the 8 MeV diodes only part of the structures were irradiated because of the small beam diameter, so that the analysis can not be performed. However, for these large area SQ1 diodes, it is anticipated that in principle the perimeter component is negligible even after proton irradiation. Another factor which may play is the B-deactivation mentioned above. Currently, further C-V

analysis is undertaken to study the K_B damage coefficient ($=-\partial[B]/\partial\Phi$) and its relationship with NIEL.

Table II.V : Leakage current damage coefficient obtained at –1 V for proton-irradiated 10 mm^2 area diodes, compared with the theoretical total NIEL (after [7]).

Proton Energy (MeV)	K_I (A cm^2/proton)	NIEL (keV cm^2/g)
8	1.8×10^{-22}	9.49
20	3.1×10^{-22}	5.36
60	2.8×10^{-22}	3.52

In order to derive the activation energy of the generation current density, temperature dependent measurements have been performed for the 20 MeV STI diodes. A result obtained for a reverse bias of -1 V and a fluence $\Phi=10^{13}$ cm^{-2} is given in Fig. II.28. It is clear that after irradiation, the generation current dominates in the whole temperature interval, giving rise to activation energies in the range 0.49 to 0.66 eV, i.e. near mid gap, which explains the drastic increase of J_{gA}. The different energy level E_T after proton exposure indicates that radiation-induced centres are mainly responsible for the leakage current increase in Fig. II.28, overwhelming the effect of the pre-existing deep levels [10]. Although no DLTS results are available yet, one can anticipate that the divacancy level at E_c-0.42 eV will play an important role [11-14], eventually assisted by some other deep traps, possibly associated with B_I or its stable complexes. It should finally be noted that after the temperature dependent I-V measurements, a reduction of the leakage current of no more than 10% has been found [5], indicating some annealing of radiation defects.

The occurrence of ionisation damage can be investigated by studying the peripheral leakage current component of large perimeter diodes. This should give an idea of the charge-trapping and interface-state generation properties of proton-irradiated STI oxides. An example is given in Fig. II.294, after 20 MeV proton exposure. Again, a linear increase of I_P with Φ is observed, which enables to derive a

corresponding damage coefficient. The slopes indicated in Fig. II.29 are for a proton fluence of 10^{12} cm^{-2} and show a strong dependence on the reverse bias. This suggests a field-dependent non-SRH generation mechanism to be responsible for the surface generation current. It has also been found that the STI processing has a marked impact on the ionisation damage [5], in agreement with recent reports [3-4].

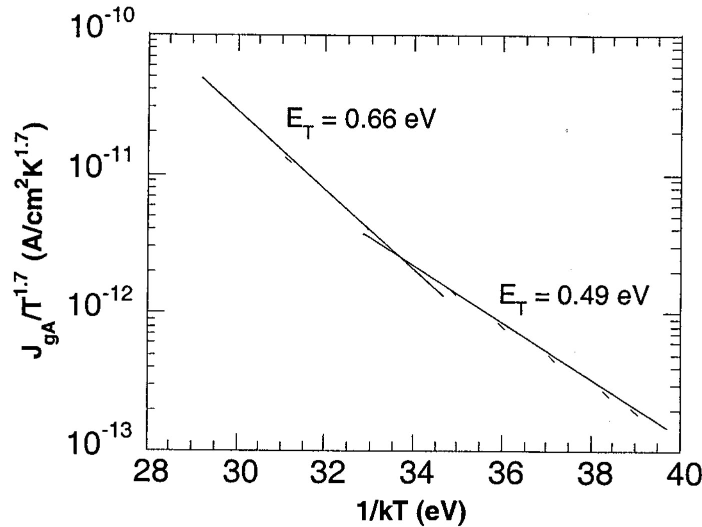

Fig. II.28. Arrhenius plot of the generation current density after a 20 MeV 10^{13} cm^{-2} proton irradiation. V_R=-1 V.

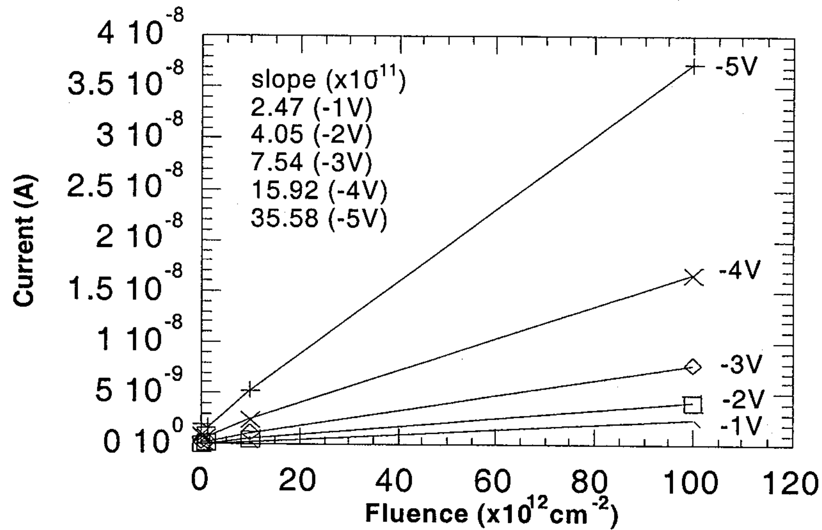

Fig. II.29. Increase in the reverse current of a meander diode at different reverse bias, in function of the 20 MeV proton fluence. T=25°C.

II.2.3.2. Conclusions

Summarizing, a clear degradation of the forward and reverse characteristics of high-energy proton irradiated diodes with STI has been observed. Both the area and the peripheral leakage current component increase significantly, implying the occurrence of ionization and displacement damage, respectively.

II.2.3.3. Acknowledgments

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II.2.3.4. References

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CONCLUSIONS

In general it can be stated that the two activities have been successfully completed. The two extensive literature reviews contain a huge amount of information, which for the first time have been brought together in practical and useful documents. This has been forming the basis for the additional experimental work, needed to validate some of the conclusions and/or to obtain new insights into certain issues.

The most important conclusions of the first Activity related to Radiation Effects in Cryogenic Electronics, are the following:

- From a radiation hardness viewpoint, the 0.7 μm CMOS technology can be simplified by omitting the Lowly Doped Drain (LDD) process module.
- For the studied range, both proton and γ-irradiations have a beneficial impact on the suppression of the kink effect.
- The detector read-out circuits for the FIRST mission can be fabricated in the simplified 0.7 μm CMOS technology while keeping a sufficient radiation hardness performance.
- While for protons irradiation at room temperature is the worst case, the opposite is valid for γ-irradiation.

The most important conclusions of the second Activity related to Radiation Effects in Advanced Semiconductor Materials, are the following:

- Scaling down the technology has a positive effect on the radiation hardness of the devices and circuits.
- There exists a length dependence of the radiation behavior of some electrical performance parameters.
- For some of the process modules, which will be used in future scaled down technologies, some more research is needed in order to investigate their

impact on the radiation hardness. Important modules are the shallow trench isolation and the use of nitrided gate oxides.

- For STI diodes, both ionization and displacement damage may occur in parallel, resulting into an increase of both the area and the peripheral leakage current density.
- Some of the observed radiation behavior can not be fully explained yet with the presently used physical models.

In support of future activities in this field, it is suggested to focus on the following topics:

- The execution of irradiation at low temperature. Although this should in first place be done for γ-irradiations, it would surely be worthwhile to also check the impact of the temperature for proton irradiations.
- To continue with the study of the radiation hardness of advanced process modules, in order to define some better theoretical models.
- To complement the already available information on the radiation hardness of the 0.18 μm CMOS technology, in order to extract the different performance parameters which are required as input for device simulators such as SPICE.
- To check the impact of radiation on the circuits performance parameters such as speed and power consumption.

A part of the above mentioned studies are essential for some missions to be launched in the coming years (e.g. impact of low temperature irradiation on the performance of the FIRST devices), while another part (e.g. study of deep submicron technologies) are required to increase the confidence level in the use of COTS devices fabricated in a scaled down technology, i.e. with 0.18 μm geometries. For the missions envisaged to be launched by 2010, such 0.18 μm and below technologies will be standard on the market.

APPENDIX: DOCUMENT CATALOGUE

P35284-IM-PP-0001: Proposal for RFQ/3-8938/97/NL/NB : Study of Radiation Effects in Cryogenic Electronics and Advanced Semiconductor Materials.

Minutes

P35284-IN-MN-0001: Minutes of the Kick-off meeting held at ESTEC on April 24, 1997

Deliverables

P35284-IM-RP-0003: Deliverable D1 - Literature Study on Radiation Effects in Cryogenic Electronics

P35284-IM-RP-0012: Deliverable D2 - Radiation Testing of Cryogenic Devices and Circuits

P35284-IM-RP-0016: Deliverable D4 – Literature Study on Radiation Effects in Advanced Semiconductor Materials

P35284-IM-RP-0017: Deliverable D3 – Application Manual for Cryogenic Electronics in Space

P35284-IM-RP-0018: Deliverable D5 – Radiation Damage Studies in Advanced Microelectronic Materials and Devices

P35284-IM-RP-0023: Deliverable D6 – Final Report

Progress Reports

P35284-IM-RP-0001: Progress Report nr. 1

P35284-IM-RP-0002: Progress Report nr. 2

P35284-IM-RP-0004: Progress Report nr. 3

P35284-IM-RP-0005: Progress Report nr. 4

P35284-IM-RP-0006: Progress Report nr. 5

P35284-IM-RP-0007: Progress Report nr. 6

P35284-IM-RP-0008: Progress Report nr. 7

P35284-IM-RP-0009: Progress Report nr. 8

P35284-IM-RP-0010: Progress Report nr. 9

P35284-IM-RP-0011: Progress Report nr. 10

P35284-IM-RP-0013: Progress Report nr. 11

P35284-IM-RP-0014: Progress Report nr. 12

P35284-IM-RP-0015: Progress Report nr. 13

P35284-IM-RP-0018: Progress Report nr. 14

P35284-IM-RP-0019: Progress Report nr. 15

P35284-IM-RP-0020: Progress Report nr. 16

P35284-IM-RP-0021: Progress Report nr. 17

P35284-IM-RP-0022: Progress Report nr. 18

Conference Contributions:

"Proton Radiation Hardness of MOS Transistors at Cryogenic Temperatures", E. Simoen, C. Claeys and A. Mohammadzadeh, presented at the General Scientific Meeting of the Belgian Physical Society, Brussels, Belgium, May 20-21, 1999

"Comparison of the total-dose and 60 MeV proton-irradiation response of CMOS transistors operated at 4.2 K", E. Simoen, C. Claeys and A. Mohammadzadeh, presented at RADECS 99, Abbaye de Fontevraud (France), Sept. 13-17, 1999

"Impact of 60 MeV Proton Irradiations on the 4.2 K Characteristics of 0.7 μm CMOS Transistors", E. Simoen, C. Claeys and A. Mohammadzadeh, presented at Symposium on Low Temperature Electronics, The Electrochemical Society Fall Meeting, Honolulu, Hawaii, Oct. 17-22, 1999

"Semi Empirical Modeling of the Multiplication current in n-MOSFETs Operating at Liquid Helium Temperatures", E. Simoen, C. Claeys and A. Mohammazadeh, presented at the Belgian Physics Society Meeting, UCL, Louvain la Neuve, Belgium, May 25-26, 2000

"Guidelines for Cryogenic Spaceborn CMOS Testing and Optimization", C. Claeys, E. simoen and A. Mohammadzadeh, presented at 4th European Workshop on Low Temperature Electronics, Noordwijk, The Netherlands, June 21-23, 2000

"Substrate Current and Kink Analysis of MOSFETs at Liquid Helium Temperature", E. Simoen, C. Claeys and A. Mohammadzadeh, presented at 4th European Workshop on Low Temperature Electronics, Noordwijk, The Netherlands, June 21-23, 2000

"High-Energy Boron Implantation and Proton Irradiation Effects in Diodes With Shallow Trench isolation", A. Poyai, E. Simoen, C. Claeys, K. Hayama, K. Kobayashi, H. Ohyama, H. Takizawa, M. Kokkoris, E. Kossionides, G. Fanourakis and A. Mohammadzadeh, presented at the 2nd ENDEASD Workshop, Kist-Stockholm, Sweden, June 27-19, 2000

"Displacement Damage Effects after High-Energy Proton Irradiation in cryogenic MOSFETs for Space Applications", E. Simoen, C. Claeys and A. Mohammadzadeh , accepted for presentation at the RADECS 2000 Workshop, Louvain-La-Neuve, Belgium, Sept. 11-13, 2000

"Evidence for Short-Channel Effect in the Radiation Response of 0.18 μm CMOS Transistors", E. Simoen, A. Augendre, T. Marescaux, C. Claeys, A. Badenes and A. Mohammadzadeh , accepted for presentation at the RADECS 2000 Workshop, Louvain-La-Neuve, Belgium, Sept. 11-13, 2000

"Radiation Source Dependence of Degradation in Shallow Trench Isolation Diodes", K. Hayama, H. Ohyama, A. Poyai, E. Simoen, Y. Takami, H. Takizawa and A. Mohammadzadeh, accepted for presentation at the RADECS 2000 Workshop, Louvan-La-Neuve, Belgium, Sept. 11-13, 2000

"Radiation Hardness of Deep Submicron CMOS Technologies", C. Claeys, E. Simoen, H. Ohyama and A. Mohammadzadeh, invited presentation to be given at the 4th International Workshop on Radiation Effects on Semiconductor Devices for Space Applications, Tsukuba-chi, Japan Oct. 11-13, 2000

Publications:

E. Simoen, C. Claeys and A. Mohammadzadeh, "Comparison of the Total-Dose and 60 MeV Proton-Irradiation Response of CMOS Transistors Operated at 4.2 K", accepted for publication in Proceedings RADECS '99

A. Poyai, E. Simoen, C. Claeys, K. Hayama, K. Kobayashi, H. Ohyama, H. Takizawa, M. Kokkoris, E. Kossionides, G. Fanourakis and A. Mohammadzadeh, "High-Energy Boron Implantation and Proton Irradiation Effects in Diodes With Shallow Trench isolation", in Proc. 2nd ENDEASD Workshop, Ed. C. Claeys, 193-203, 2000

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