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Heavy Ion Test of 2-Gbit Micron DDR2-SDRAM Devices MT47H256M8

Preliminary Contributions to the Test Report

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1. Scope

The primary goal of the Nov. 2009 Jyväskylä test campaign was to check the functionality of the new DDR2 test bed, and to collect some test data sets for the development of realistic test data evaluation S/W.

In consequence of the positive outcome of the Nov. 09 test we regard the DDR2 test bed to be fully functional for tests at room temperature.

Never the less improvements are always possible. At the time being the implementation of an error screen zoom is in progress. This will allow the visual differentiation between adjacent data symbols.

Also envisaged is the implementation of a temperature controlled device heating.

Randomly distributed Single Errors are of minor concern. These errors easily can be coped even by Hamming error correction.
But, clustered errors are prone to exhaust the capability of the error correction. In consequence, the characterization of the various types of clustered errors and the evaluation of respective cross section curves are of major importance.

Clustered errors can be differentiated into two main categories:

a) Those, which directly are caused by a single hit of adjacent structures of the cell array, and
b) SEFIs, which originate from particle induced malfunctions of the control circuitry.

A related aspect is the study of countermeasures against SEFIs. Re-initialization of the device is known to be an effective countermeasure. But, it slows down the effective access rate. Which re-initialization rate should be applied? How much resistant SEFIs withstand the re-initialization?

Another related aspect is whether SEFI induced cluster errors will be induced during non-access periods. Refresh is still running and the generation of cluster errors due to particle induced disturbances of the refresh circuitry is imaginable.

Relevant questions are (i) whether those SEFIs occur, and in case(ii) whether they are only transient or even all / some of them persistent, and again in case (iii) whether re-initialization during non-access periods should be recommended.

Another point, often highlighted in the literature, is hard errors / weak cells. From published papers we see that these hard errors are a specific very rare type of distributed single errors, which can be wiped out easily by the usual error correction, together with the more frequent soft single errors.

Therefore, we plan to inspect our test data sets for hard errors, but this will not be an high priority task. In particular, at this time we don't plan to investigate the influence of the refresh period on the occurrence frequency of hard errors.

To summarize, at this time our main goals are partly test related, namely

a) Collection of test data sets in three test modes (M3 "Static" Storage, M1 Dynamic Read and M2 Dynamic Marching) at room temperature, and in a following test also at elevated temperature (up to 75°C).
b) Studying the effect of re-initialization (Two initialization modes, several re-initialization periods)

and partly S/W related, namely

c) to improve the automatic detection, classification and extraction of the different cluster error / SEFI types in order to gain reliable SEFI type specific cross section curves,
d) to implement the zoom function to improve the resolution of the screen image
e) to extend the address range of the test bed to cover the full address range of up to 8 Gbit devices

2. Preliminary Discussion of Nov. 2009 Test Results

Due to a S/W limitation of the test bed all tests were restricted to one half of the address space (1 Gbit).

2.1 Storage Mode M3b (Read after Irradiated Storage with Re-Initialization)

See Tab. 1 + 6, Fig. 1 + 2

Initialization was performed every second and before read out.

First four static errors already at N, LET = 1.8 MeV cm^2 mg^{-1}.

No SEFIs at all, i.e. no SEFI-disturbances of Refresh (because of cyclic re-initialization ?)

At high LET we see a very minor difference between raw data and clean data after passing the cluster extraction filter

No significant difference between both samples.

Cross section curves of raw (Fig. 1) and cleaned (Fig. 2) single bit errors are identical

Tab. 6 shows the spectrum of bit errors per 32 bit word. Significant counts of double and tri-

ple bit errors appear only at Xe, LET = 60).

The error map (Tab. 11) shows only single errors.

2.2 Read Mode M1 (Dynamic Read under Irradiation)

See Tab2 + 3, Fig. 3 + 4, 7 - 11

Tab. 12 shows the error map without repetitive initialization and Tab 13 the error map with initialization. In Tab 12 the periodic occurrence of row errors is significant. The reason for this periodicity still is not understood.

The more favorable appearance of device Mic1d (second column) is misleading. This originates from the occurrence of a persistent SEFI after about 10 test cycles, indicated by a red bar near the lower edge.

Initialization removes those row errors completely at low LETs and reduces by much at high LETs.

Fig. 3 shows the cross section of raw single errors for both, operation without initialization (M1a) and with initialization (M1b). As already mentioned the raw single error count does no more include errors belonging to regular row and column SEFI pattern.

Surprisingly, both single error cross sections differ by much. This seems strange because initialization shouldn't affect the cell status. In other words, the difference should be caused by still not extracted SEFI related "pseudo"-single errors.

This could be verified by inspection of the respective regions of the data set.

In consequence S/W filter were developed to extract cluster-like single error accumulations.

Fig. 8 and 9 show one regular row and one regular column error. Each bin represents a 32-bit word. It appears in red if one ore more of these 32 bit are erroneous. These SEFI data easily are extractable.
But, besides of these regular SEFIs other repetitive error pattern appear. Examples are shown in Fig. 10 and 11.

The extraction of the more sophisticated "pseudo"-cluster errors and additionally of all 32-bit words affected by multi-bit errors delivers the clean cross section, which represents only cell errors.

Then, the clean cross section curves of read with and without initialization become identical.

The classification of the extracted "≥1 bit error per 32 bit word" is in progress. Possibly, they reflect more complicated repetitive error pattern.

Tab 7 shows for M1a (no repetitive initialization) the spectral distribution of the error count per 32-bit word, (i) for raw data in red and (ii) for cleaned data in blue.

Apparently the red spectrum with peaks at 8 and 16 bit points to SEFI induced corruptions of larger data elements.

Tab. 8 shows the same spectrum for M1b (with initialization once per row).

The broad SEFI related spectra disappear with the exception of one persistent SEFI of device Mic1f at Ar.

2.3 Marching Mode M2 (Continuous Sequence of Write, Storage and Read Operations under Irradiation)

See Tab. 4 + 5, 9 + 10, 14 + 15, Fig. 5 + 6

Again repetitive re-initialization reduces the SEFI occurrence drastically.

Also, we see periodic row SEFIs.

Further cleaning of the raw data results in identical single error cross section curves with and without re-initialization.

Mode: M3b (Read after storage with Init) Micron DDR2-SDRAM MT47H256M8, JYV Nov. 2 - 5, 2009 2010_03_18

Run IDA	Run RADEF	Ion	LET_{eff} [MeV cm^2mg^{-1}]	Device Marking	Tested Adress Range [Bit]	Date Code	Write Adress dependend IS (0x0001 = each row)	Read Adress dependend IS (0x0001 = each row)	IS each time [ms]	Mode	Fluence [cm^{-2}]	Time [s]	Average Flux [$cm^{-2}s^{-1}$]	Raw Static Errors [bits]	Cleaned Static Errors [bits]	$\sigma_{static,bit}$ [cm^2bit^{-1}]	$\sigma_{static,device}$ [cm^2die^{-1}]
131	139	15N4+	1,8	Mic1d	1E+09	0742	-	-	1000	M3b	2,00E+07	262	76336	4,00E+00	4,00E+00	1,86E-16	1,73E-25
Σ		**15N4+**								**M3b**	**2,00E+07**	**262**		**4,00E+00**	**4,00E+00**	**1,86E-16**	**1,73E-25**
94	125	20Ne6+	3,6	Mic1a	1E+09	0742	-	-	1000	M3b	2,00E+06	107	18692	3,50E+01	3,50E+01	1,63E-14	1,52E-23
114	132	20Ne6+	3,6	Mic1d	1E+09	0742	-	-	1000	M3b	2,00E+06	108	18519	1,60E+01	1,60E+01	7,45E-15	6,94E-24
Σ		**20Ne6+**								**M3b**	**4,00E+06**	**215**		**5,10E+01**	**5,10E+01**	**1,19E-14**	**1,11E-23**
5	93	40Ar12+	10,1	Mic1a	1E+09	0742	-	-	1000	M3b	2,00E+05	127	1575	1,60E+03	1,61E+03	7,50E-12	6,99E-21
51	111	40Ar12+	10,1	Mic1d	1E+09	0742	-	-	1000	M3b	2,00E+05	100	2000	1,50E+03	1,48E+03	6,89E-12	6,42E-21
Σ		**40Ar12+**								**M3b**	**4,00E+05**	**227**		**3,10E+03**	**3,09E+03**	**7,20E-12**	**6,70E-21**
157	149	56Fe15+	18,5	Mic1a	1E+09	0742	-	-	1000	M3b	2,00E+05	110	1818	7,50E+03	7,45E+03	3,47E-11	3,23E-20
197	160	56Fe15+	18,5	Mic1d	1E+09	0742	-	-	1000	M3b	2,00E+05	98	2041	8,20E+03	8,21E+03	3,82E-11	3,56E-20
Σ		**56Fe15+**								**M3b**	**4,00E+05**	**208**		**1,57E+04**	**1,57E+04**	**3,65E-11**	**3,40E-20**
226	169	82Kr22+	32,1	Mic1d	1E+09	0742	-	-	1000	M3b	4,00E+04	108	370	4,00E+03	3,75E+03	8,72E-11	8,13E-20
245	175	82Kr22+	32,1	Mic1a	1E+09	0742	-	-	1000	M3b	4,00E+04	96	417	3,70E+03	3,55E+03	8,27E-11	7,70E-20
Σ		**82Kr22+**								**M3b**	**8,00E+04**	**204**		**7,70E+03**	**7,30E+03**	**8,50E-11**	**7,91E-20**
263	232	131Xe35+	60	Mic1a	1E+09	0742	-	-	1000	M3b	1,00E+05	107	935	5,20E+04	2,78E+04	2,59E-10	2,41E-19
287	240	131Xe35+	60	Mic1d	1E+09	0742	-	-	1000	M3b	1,00E+05	127	787	5,20E+04	2,24E+04	2,09E-10	1,94E-19
Σ		**131Xe35+**								**M3b**	**2,00E+05**	**234**		**1,04E+05**	**5,02E+04**	**2,34E-10**	**2,18E-19**

Tab. 1: Mode M3b (Read after storage with Initialisation)

Tab. 2: Mode M1a (Read only without Initialisation)

Mode: M1a (Read only without Init) Micron DDR2-SDRAM MT47H256M8, JYV Nov. 2 - 5, 2009 2010_03_18

Run IDA	Run RADEF	Ion	LET_{eff} [MeV cm^2mg^{-1}]	Device Marking	Loops [1E9 Bit]	Tested Adress Range [Bit]	Write Adress dependend IS (0x0001 = each row)	Read Adress dependend IS (0x0001 = each row)	Fluence [cm^{-2}]	Time [s]	Average Flux [$cm^{-2}s^{-1}$]	Raw SEU during Irr.	Cleaned SEU during Irr.		$X_{SEU, dev}$ [cm2bit-1]	$X_{SEU,bit}$ [cm2bit-1]
133	140	15N4+	1,8	Mic1d	58	6E+10	-	-	2,00E+07	164	121951	1,26E+02	1,55E+02		7,75E-06	7,22E-15
Σ		**15N4+**							**2,00E+07**	**164**						**7,22E-15**
100	127	20Ne6+	3,6	Mic1a	13	1E+10	-	-	2,00E+06	55	36364		3,24E+02		1,62E-04	1,51E-13
116	133	20Ne6+	3,6	Mic1d	21	2E+10	-	-	2,00E+06	86	23256	2,44E+03	4,66E+02		2,33E-04	2,17E-13
Σ		**20Ne6+**							**4,00E+06**	**141**						**1,84E-13**
12	96	40Ar12+	10,1	Mic1a	29	3E+10	-	-	2,00E+05	130	1538	6,44E+06	2,54E+04		1,27E-01	1,18E-10
16	97	40Ar12+	10,1	Mic1a	4	4E+09	-	-	2,10E+04	15	1400	6,77E+04	1,01E+03		4,79E-02	4,46E-11
53	112	40Ar12+	10,1	Mic1d	1	1E+09	-	-	2,00E+05	104	1923	6,08E+06	2,04E+04		1,02E-01	9,50E-11
72	118	40Ar12+	10,1	Mic1f	22	2E+10	-	-	2,00E+05	99	2020	4,66E+06	3,72E+04		1,86E-01	1,73E-10
Σ		**40Ar12+**							**6,21E+05**	**348**						**1,08E-10**
159	150	56Fe15+	18,5	Mic1a	26	3E+10	-	-	2,00E+05	118	1695	1,22E+07	1,04E+05		5,20E-01	4,84E-10
205	162	56Fe15+	18,5	Mic1d	1	1E+09	-	-	2,00E+05	97	2062		8,55E+03	persistant SEFI	4,27E-02	3,98E-11
Σ		**56Fe15+**							**4,00E+05**	**215**						**2,62E-10**
228	170	82Kr22+	32,1	Mic1d	23	2E+10	-	-	4,00E+04	109	367	1,54E+06	4,18E+04		1,05E+00	9,74E-10
247	176	82Kr22+	32,1	Mic1a	21	2E+10	-	-	4,00E+04	96	417	2,93E+06	3,83E+04		9,57E-01	8,92E-10
Σ		**82Kr22+**							**8,00E+04**	**205**						**9,33E-10**
267	234	131Xe35+	60	Mic1a	22	2E+10	-	-	1,00E+05	98	1020	6,81E+06	2,82E+05		2,82E+00	2,63E-09
289	241	131Xe35+	60	Mic1d	21	2E+10	-	-	1,00E+05	126	794		1,25E+05	persistant SEFI	1,25E+00	1,16E-09
294	242	131Xe35+	60	Mic1d	30	3E+10	-	-	1,00E+05	135	741	1,07E+07	3,40E+05		3,40E+00	3,16E-09
Σ		**131Xe35+**							**3,00E+05**	**359**						**1,93E-09**

Tab. 3: Mode M1b (Read only with Initialisation)

Mode: M1b (Read only with Init) Micron DDR2-SDRAM MT47H256M8, JYV Nov. 2 - 5, 2009 2010_03_18

Run IDA	Run RADEF	Ion	LET_{eff} [MeV cm^2mg^{-1}]	Device Marking	Loops [1E9 Bit]	Tested Adress Range [Bit]	Write Adress dependend IS (0x0001 = each row)	Read Adress dependend IS (0x0001 = each row)	Fluence [cm^{-2}]	Time [s]	Average Flux [$cm^{-2}s^{-1}$]	Raw SEU during Irr.	Cleaned SEU during Irr.		$X_{SEU, dev}$ [cm2bit-1]	$X_{SEU,bit}$ [cm2bit-1]
136	141	15N4+	1,8	Mic1d	57	6E+10	-	RAIS 0x0001	2,00E+07	261	76628	1,99E+02	1,99E+02		9,95E-06	9,27E-15
Σ		**15N4+**							**2,00E+07**	**261**						**9,27E-15**
104	128	20Ne6+	3,6	Mic1a	15	2E+10	-	RAIS 0x0001	2,00E+06	66	30303	3,05E+02	3,05E+02		1,53E-04	1,42E-13
120	134	20Ne6+	3,6	Mic1d	20	2E+10	-	RAIS 0x0001	2,00E+06	90	22222	1,72E+02	1,72E+02		8,60E-05	8,01E-14
Σ		**20Ne6+**							**4,00E+06**	**156**						**1,11E-13**
7	94	40Ar12+	10,1	Mic1a	27	3E+10	-	RAIS 0x0001	2,00E+05	128	1563	2,63E+04	2,65E+04		1,33E-01	1,23E-10
57	113	40Ar12+	10,1	Mic1d	23	2E+10	-	RAIS 0x0001	2,00E+05	103	1942	1,96E+04	1,97E+04		9,86E-02	9,18E-11
80	120	40Ar12+	10,1	Mic1f	21	2E+10	-	-	2,00E+05	96	2083		5,38E+03	persistant SEFI	2,69E-02	2,50E-11
83	121	40Ar12+	10,1	Mic1f	22	2E+10	-	RAIS 0x0001	2,00E+05	98	2041	2,94E+04	2,96E+04		1,48E-01	1,38E-10
Σ		**40Ar12+**							**8,00E+05**	**425**						**9,46E-11**
163	151	56Fe15+	18,5	Mic1a	25	3E+10	-	RAIS 0x0001	2,00E+05	115	1739	9,74E+04	9,84E+04		4,92E-01	4,58E-10
208	163	56Fe15+	18,5	Mic1d	22	2E+10	-	RAIS 0x0001	2,00E+05	97	2062	1,01E+05	1,02E+05		5,09E-01	4,74E-10
Σ		**56Fe15+**							**4,00E+05**	**212**						**4,66E-10**
232	171	82Kr22+	32,1	Mic1d	23	2E+10	-	RAIS 0x0001	4,00E+04	105	381	4,45E+04	4,42E+04		1,11E+00	1,03E-09
251	177	82Kr22+	32,1	Mic1a	21	2E+10	-	RAIS 0x0001	4,00E+04	96	417	3,90E+04	3,86E+04		9,65E-01	8,99E-10
Σ		**82Kr22+**							**8,00E+04**	**201**						**9,65E-10**
271	235	131Xe35+	60	Mic1a	21	2E+10	-	RAIS 0x0001	1,00E+05	95	1053	4,15E+05	2,73E+05		2,73E+00	2,54E-09
298	243	131Xe35+	60	Mic1d	31	3E+10	-	RAIS 0x0001	1,00E+05	141	709	5,05E+05	3,53E+05		3,53E+00	3,29E-09
311	247	131Xe35+	60	Mic1d	31	3E+10	-	RAIS 0x2000	1,00E+05	138	725	5,60E+05	3,53E+05		3,53E+00	3,29E-09
Σ		**131Xe35+**							**3,00E+05**	**374**						**3,04E-09**

Mode: M2a (Marching without Init) Micron DDR2-SDRAM MT47H256M8, JYV Nov. 2 - 5, 2009 2010_03_18

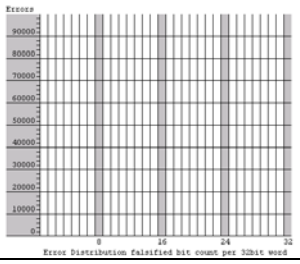
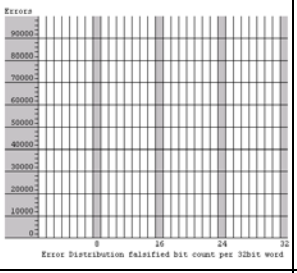
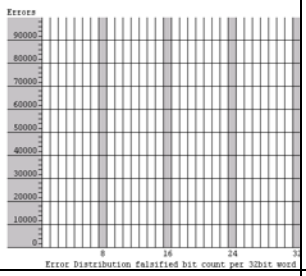
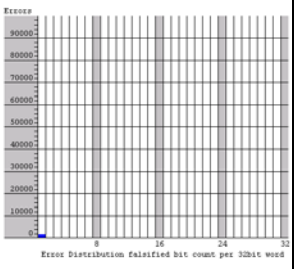
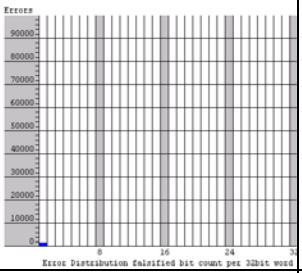
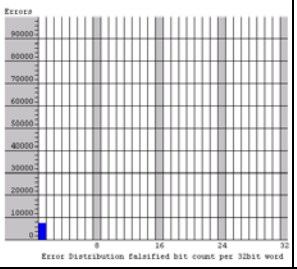
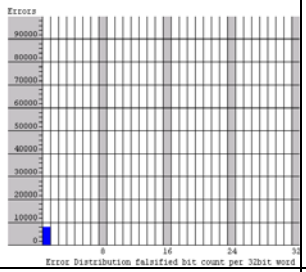
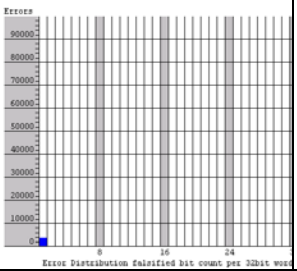
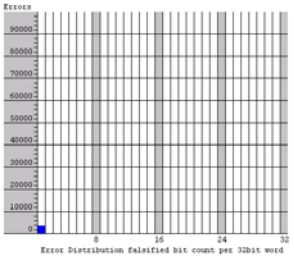
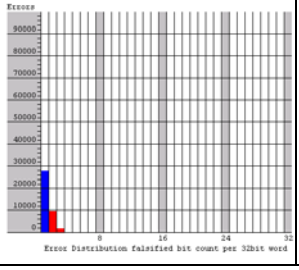
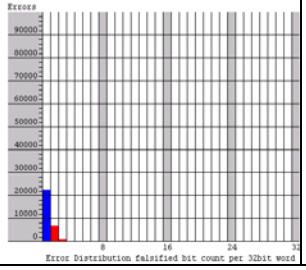
Run IDA	Run RADEF	Ion	LET_{eff} [MeV cm^2mg^{-1}]	Device Marking	Loops [1E9 Bit]	Tested Adress Range [Bit]	Write Adress dependend IS (0x0001 = each row)	Read Adress dependend IS (0x0001 = each row)	IS during Marching	Fluence [cm^{-2}]	Time [s]	Average Flux [$cm^{-2}s^{-1}$]	Raw SEU during Irr.	Cleaned SEU during Irr.	$X_{SEU, dev}$ [cm2bit-1]	$X_{SEU,bit}$ [cm2bit-1]
139	142	15N4+	1,8	Mic1d	20	2E+10	-	-	-	2,00E+07	255	78431	0,00E+00	0,00E+00	5,00E-08	4,66E-17
Σ		**15N4+**								**2,00E+07**	**255**					**4,66E-17**
107	129	20Ne6+	3,6	Mic1a	9	1E+10	-	-	-	2,00E+06	115	17391		2,13E+02	1,07E-04	9,92E-14
123	135	20Ne6+	3,6	Mic1d	8	9E+09	-	-	-	2,00E+06	95	21053	1,07E+02	9,60E+01	4,80E-05	4,47E-14
Σ		**20Ne6+**								**4,00E+06**	**210**					**7,19E-14**
18	98	40Ar12+	10,1	Mic1a	11	1E+10	-	-	-	2,00E+05	127	1575	9,15E+03	4,52E+03	2,26E-02	2,10E-11
60	114	40Ar12+	10,1	Mic1d	8	9E+09	-	-	-	2,00E+05	100	2000	1,29E+05	2,35E+03	1,17E-02	1,09E-11
86	122	40Ar12+	10,1	Mic1f	7	8E+09	-	-	-	2,00E+05	83	2410	6,46E+04	4,26E+03	2,13E-02	1,98E-11
Σ		**40Ar12+**								**6,00E+05**	**310**					**1,73E-11**
166	152	56Fe15+	18,5	Mic1a	8	9E+09	-	-	-	2,00E+05	97	2062	3,15E+05	9,15E+03	4,57E-02	4,26E-11
211	164	56Fe15+	18,5	Mic1d	8	9E+09	-	-	-	2,00E+05	99	2020	1,90E+05	9,27E+03	4,64E-02	4,32E-11
Σ		**56Fe15+**								**4,00E+05**	**196**					**4,29E-11**
235	172	82Kr22+	32,1	Mic1d	8	9E+09	-	-	-	4,00E+04	101	396	5,36E+03	4,82E+03	1,20E-01	1,12E-10
254	178	82Kr22+	32,1	Mic1a	7	8E+09	-	-	-	4,00E+04	89	449	5,34E+03	4,33E+03	1,08E-01	1,01E-10
Σ		**82Kr22+**								**8,00E+04**	**190**					**1,06E-10**
274	236	131Xe35+	60	Mic1a	9	1E+10	-	-	-	1,00E+05	107	935	6,86E+05	3,37E+04	3,37E-01	3,14E-10
301	244	131Xe35+	60	Mic1d	12	1E+10	-	-	-	1,00E+05	142	704	3,71E+05	3,11E+04	3,11E-01	2,89E-10
Σ		**131Xe35+**								**2,00E+05**	**249**					**3,02E-10**

Tab. 4: Mode M2a (Marching without Initialisation)

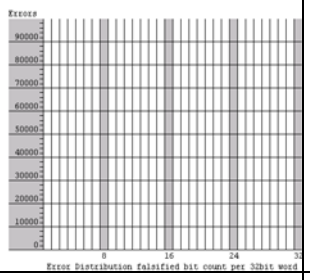
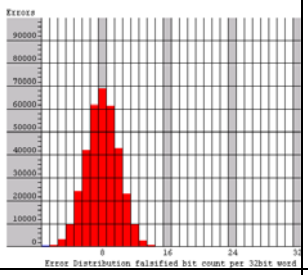
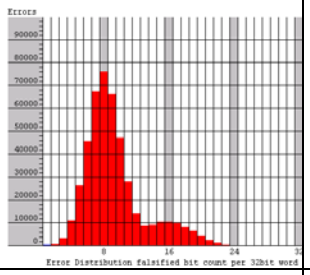
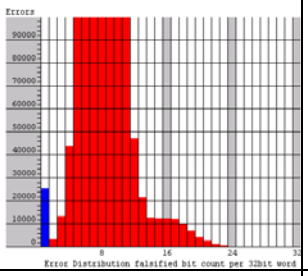
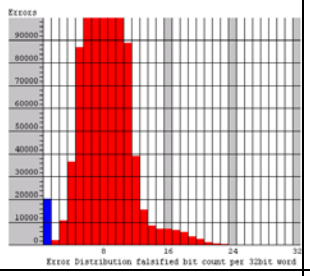
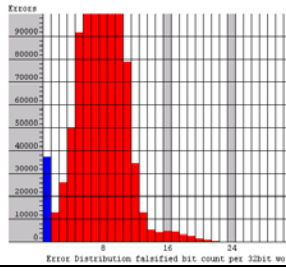
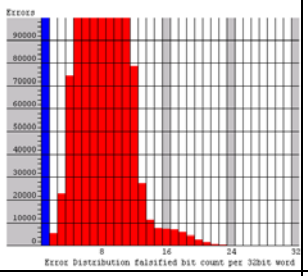
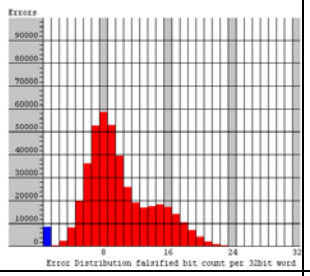
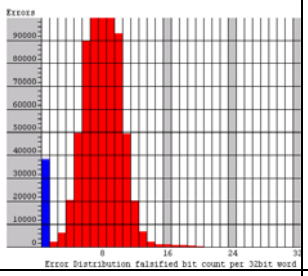
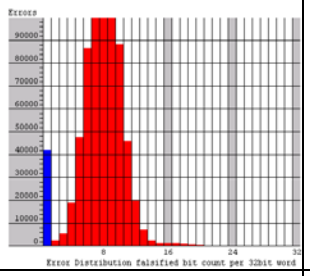
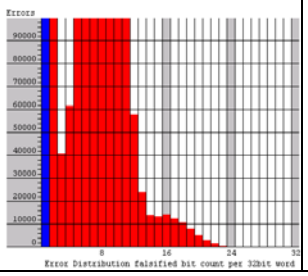
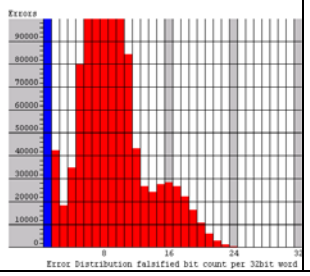
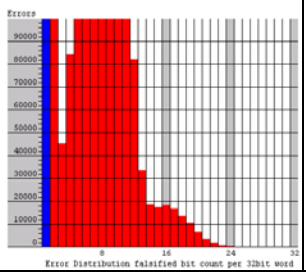
Mode: M2b (Marching with Init) Micron DDR2-SDRAM MT47H256M8, JYV Nov. 2 - 5, 2009 2010_03_18

Run IDA	Run RADEF	Ion	LET_{eff} [MeV cm^2mg^{-1}]	Device Marking	Loops [1E9 Bit]	Tested Adress Range [Bit]	Write Adress dependend IS (0x0001 = each row)	Read Adress dependend IS (0x0001 = each row)	IS during Marching	Fluence [cm^{-2}]	Time [s]	Average Flux [$cm^{-2}s^{-1}$]	Raw SEU during Irr.	Cleaned SEU during Irr.	$X_{SEU,dev}$ [cm2bit-1]	$X_{SEU,bit}$ [cm2bit-1]
141	143	15N4+	1,8	Mic1d	20	2E+10	WAIS 0x0001	RAIS 0x0001	-	2,00E+07	255	78431	5,00E+00	9,00E+00	4,50E-07	4,19E-16
Σ		**15N4+**								**2,00E+07**	**255**					**4,19E-16**
109	130	20Ne6+	3,6	Mic1a	8	9E+09	WAIS 0x0001	RAIS 0x0001	-	2,00E+06	100	20000	4,20E+01	3,20E+01	1,60E-05	1,49E-14
125	136	20Ne6+	3,6	Mic1d	8	9E+09	WAIS 0x0001	RAIS 0x0001	-	2,00E+06	95	21053	3,00E+01	1,90E+01	9,50E-06	8,85E-15
Σ		**20Ne6+**								**4,00E+06**	**195**					**1,19E-14**
20	99	40Ar12+	10,1	Mic1a	11	1E+10	-	-	IS-W-IS-R1-IS-R2	2,00E+05	131	1527	9,05E+03	1,69E+03	8,47E-03	7,89E-12
22	100	40Ar12+	10,1	Mic1a	10	1E+10	WAIS 0x0001	RAIS 0x0001	IS-W-IS-R1-IS-R2	2,00E+05	128	1563	1,79E+03	1,81E+03	9,04E-03	8,41E-12
24	101	40Ar12+	10,1	Mic1a	11	1E+10	WAIS 0x0400	RAIS 0x0400	IS-W-IS-R1-IS-R2	2,00E+05	128	1563	1,75E+03	1,73E+03	8,63E-03	8,04E-12
63	115	40Ar12+	10,1	Mic1d	9	1E+10	-	-	IS-W-IS-R1-IS-R2	2,00E+05	100	2000	1,90E+03	1,57E+03	7,83E-03	7,29E-12
76	119	40Ar12+	10,1	Mic1f	8	9E+09	-	-	IS-W-IS-R1-IS-R2	2,00E+05	99	2020	2,68E+04	2,56E+03	1,28E-02	1,19E-11
Σ		**40Ar12+**								**1,00E+06**	**586**					**8,71E-12**
172	153	56Fe15+	18,5	Mic1a	8	9E+09	WAIS 0x0001	RAIS 0x0001	-	2,00E+05	103	1942	5,70E+03	7,72E+03	3,86E-02	3,59E-11
175	154	56Fe15+	18,5	Mic1a	9	1E+10	WAIS 0x2000	RAIS 0x2000	-	2,00E+05	110	1818	2,89E+04	8,60E+03	4,30E-02	4,00E-11
179	155	56Fe15+	18,5	Mic1a	8	9E+09	WAIS 0x2000	RAIS 0x2000	-	2,00E+05	99	2020	1,23E+04	8,66E+03	4,33E-02	4,03E-11
215	165	56Fe15+	18,5	Mic1d	8	9E+09	WAIS 0x0001	RAIS 0x0001	-	2,00E+05	94	2128	8,14E+03	8,23E+03	4,11E-02	3,83E-11
Σ		**56Fe15+**								**8,00E+05**	**406**					**3,87E-11**
239	173	82Kr22+	32,1	Mic1d	7	8E+09	WAIS 0x0001	RAIS 0x0001	-	4,00E+04	93	430	3,99E+03	4,00E+03	1,00E-01	9,32E-11
256	179	82Kr22+	32,1	Mic1a	7	8E+09	WAIS 0x0001	RAIS 0x0001	-	4,00E+04	91	440	3,95E+03	3,87E+03	9,66E-02	9,00E-11
Σ		**82Kr22+**								**8,00E+04**	**184**					**9,16E-11**
278	237	131Xe35+	60	Mic1a	10	1E+10	WAIS 0x0001	RAIS 0x0001	-	1,00E+05	124	806	3,03E+04	2,76E+04	2,76E-01	2,57E-10
305	245	131Xe35+	60	Mic1d	12	1E+10	WAIS 0x0001	RAIS 0x0001	-	1,00E+05	141	709	2,72E+04	2,51E+04	2,51E-01	2,34E-10
308	246	131Xe35+	60	Mic1d	11	1E+10	WAIS 0x2000	RAIS 0x2000	-	1,00E+05	137	730	4,90E+04	2,91E+04	2,91E-01	2,71E-10
Σ		**131Xe35+**								**3,00E+05**	**402**					**2,54E-10**

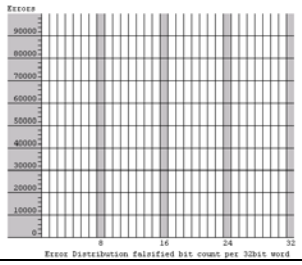
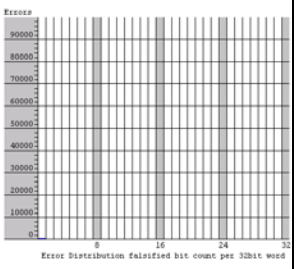
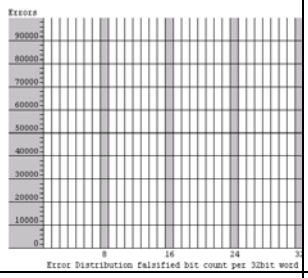
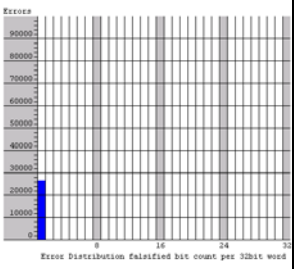
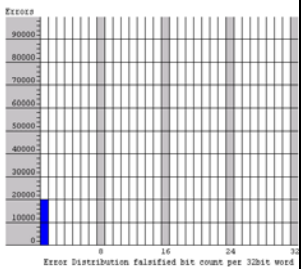
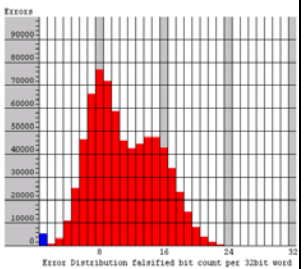
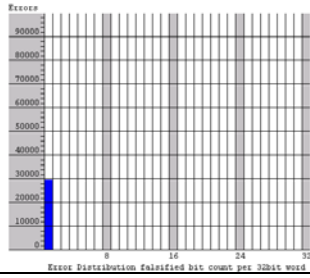
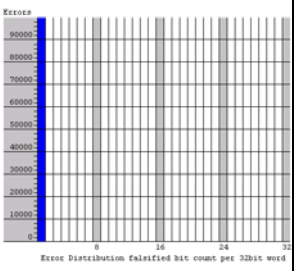
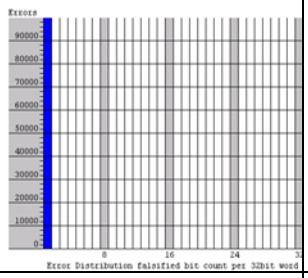
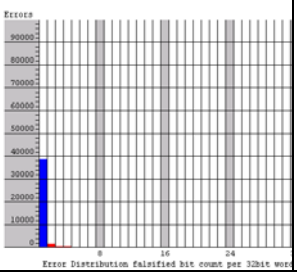
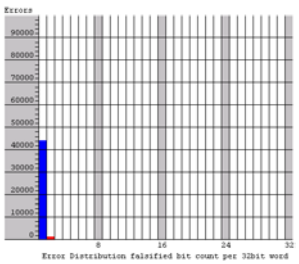
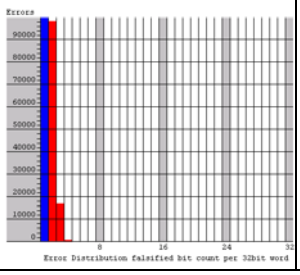
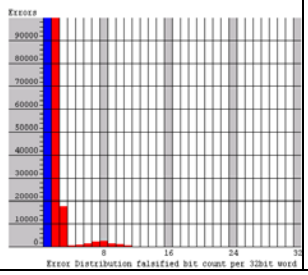
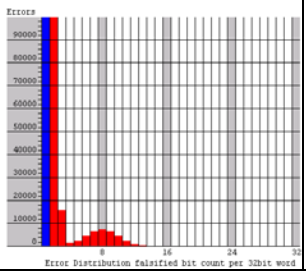
Tab. 5: Mode M2b (Marching with Initialisation)

	Mic1a	Mic1d		
15N4+				
20Ne6+				
40Ar12+				
56Fe15+				
82Kr22+				
131Xe35+				

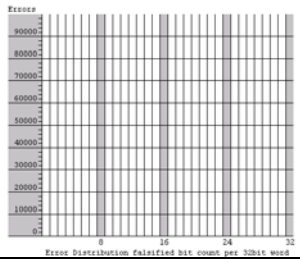
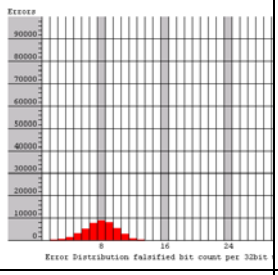
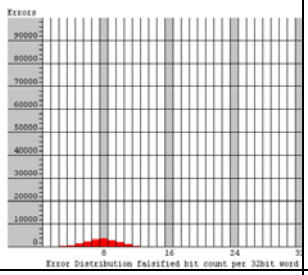
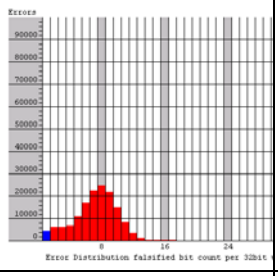
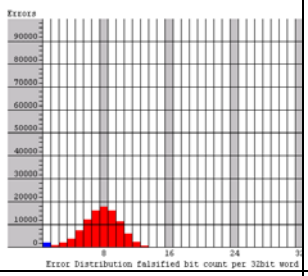
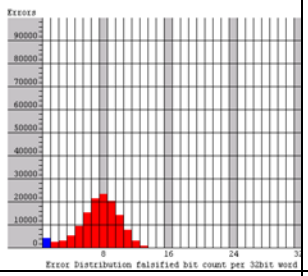
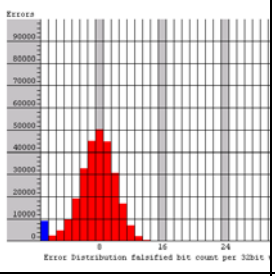
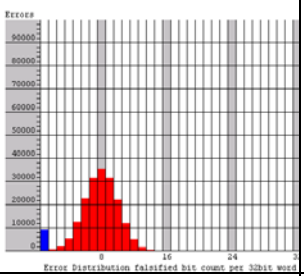
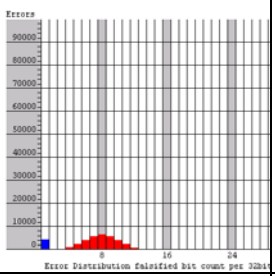
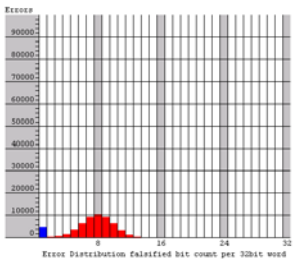
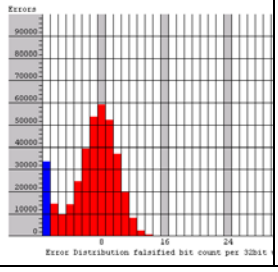
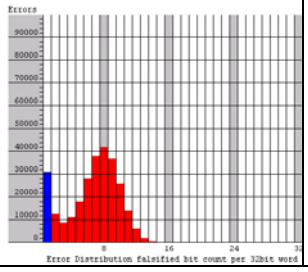
Tab. 6: Error Distribution falsified bit count per 32bit word in Mode M3b

	Mic1a	Mic1d	Mic1d	Mic1f
15N4+				
20Ne6+				
40Ar12+				
56Fe15+				
82Kr22+				
131Xe35+				

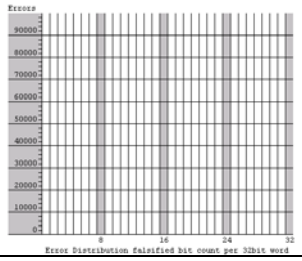
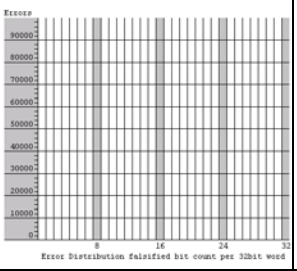
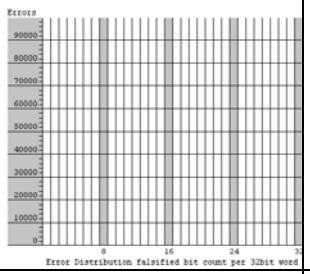
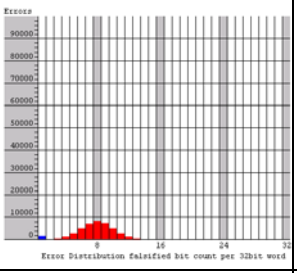
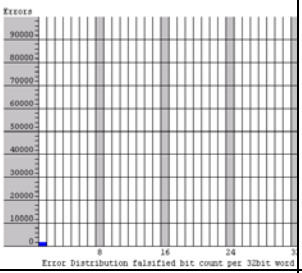
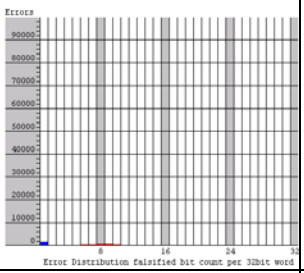
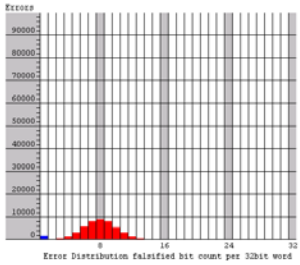
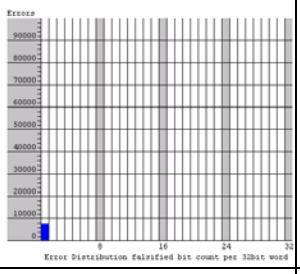
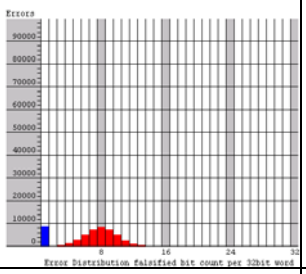
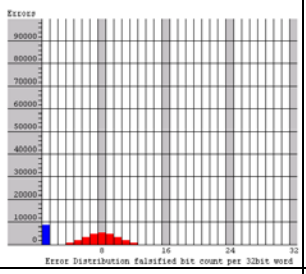
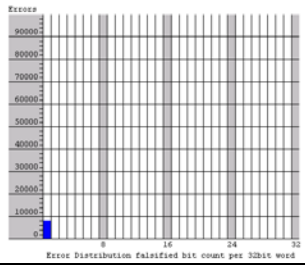
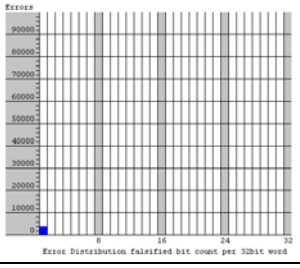
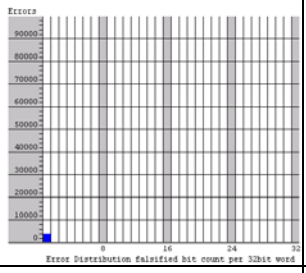
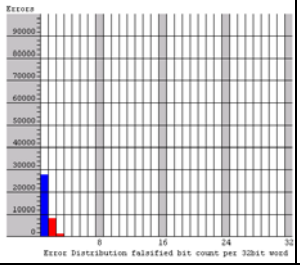
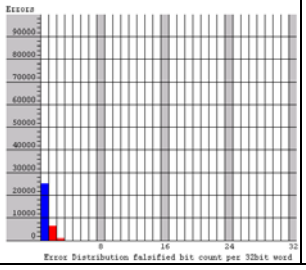
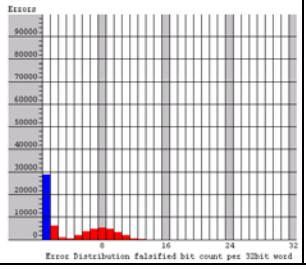
Tab. 7: Error Distribution falsified bit count per 32bit word in Mode M1a

	Mic1a	Mic1d	Mic1f	Mic1f
15N4+				
20Ne6+				
40Ar12+				
56Fe15+				
82Kr22+				
131Xe35+				

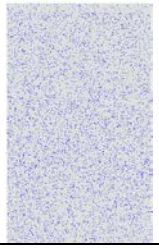
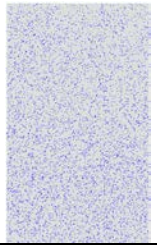
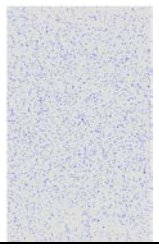
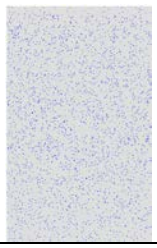
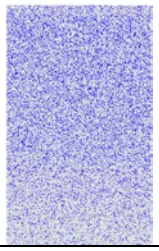
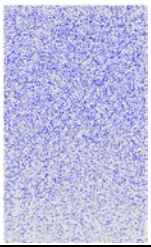
Tab. 8: Error Distribution falsified bit count per 32bit word in Mode M1b

	Mic1a	Mic1d	Mic1f	
15N4+				
20Ne6+				
40Ar12+				
56Fe15+				
82Kr22+				
131Xe35+				

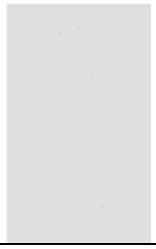
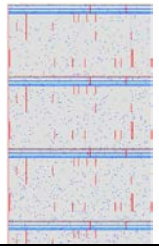
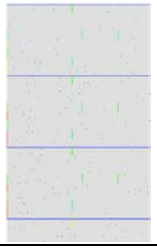
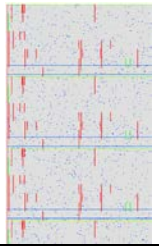
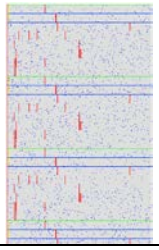
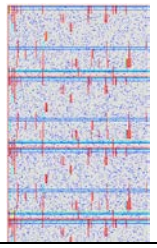
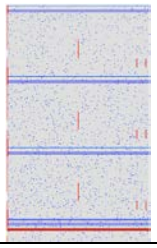
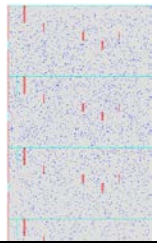
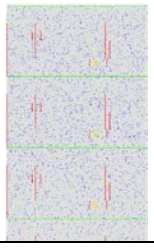
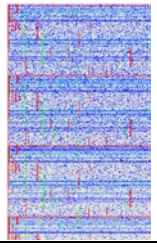
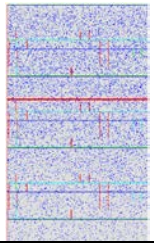
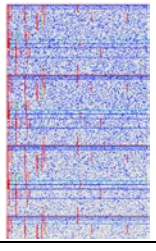
Tab. 9: Error Distribution falsified bit count per 32bit word in Mode M2a

	Mic1a	Mic1a	Mic1d	Mic1f
15N4+				
20Ne6+				
40Ar12+				
56Fe15+				
82Kr22+				
131Xe35+				

Tab. 10: Error Distribution falsified bit count per 32bit word in Mode M2b

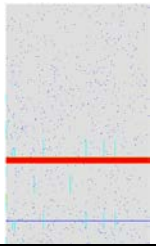
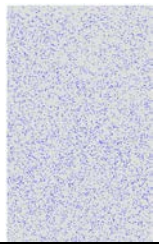
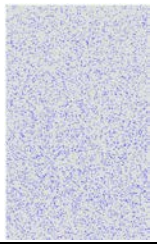
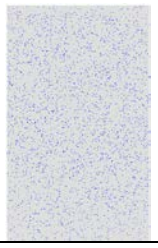
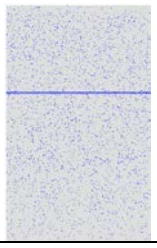
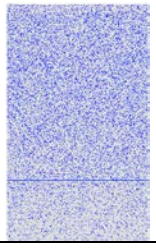
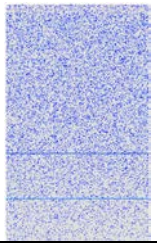
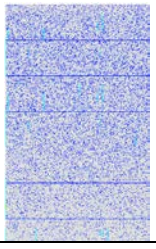
15N4+				
20Ne6+				
40Ar12+				
56Fe15+				
82Kr22+				
131Xe35+				

Tab. 11: Error Maps in Mode M3b (Read after Storage with Initialisation)

15 N 4+				
20Ne6+				
40Ar12+				
56Fe15+				
82Kr22+				
131Xe35+				

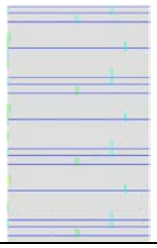
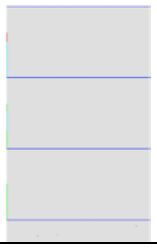
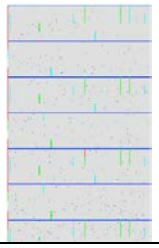
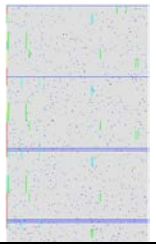
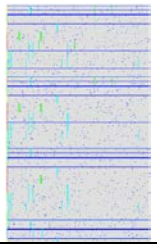
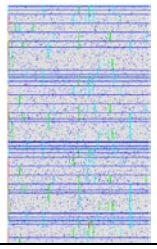
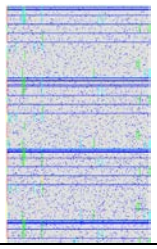
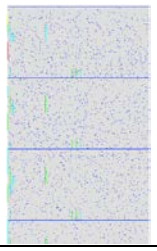
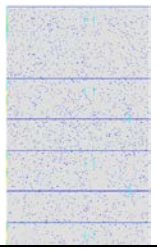
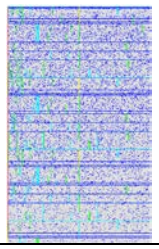
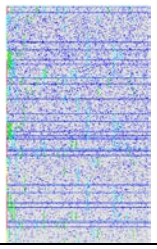
Tab. 12: Error Maps in Mode M1a (Read only without Initialisation)

Notice: The error maps do not show the complete operated adress range of 32M, but only up to about 29M.

15N4+				
20Ne6+				
40Ar12+				
56Fe15+				
82Kr22+				
131Xe35+				

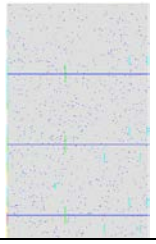
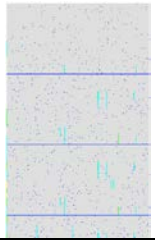
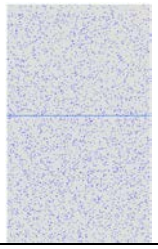
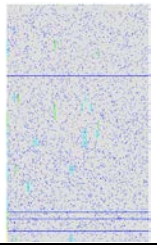
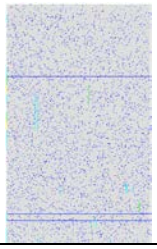
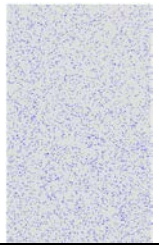
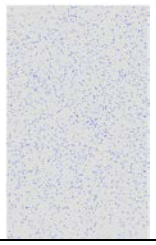
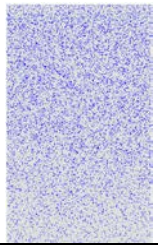
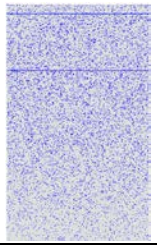
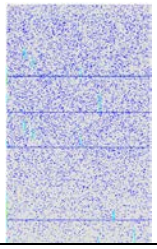
Tab. 13: Error Maps in Mode M1b (Read only with Initialisation)

Notice: The error maps do not show the complete operated adress range of 32M, but only up to about 29M.

15N4+				
20Ne6+				
40Ar12+				
56Fe15+				
82Kr22+				
131Xe35+				

Tab. 14: Error Maps in Mode M2a (Marching without Initialisation)

Notice: The error maps do not show the complete operated adress range of 32M, but only up to about 29M.

15N4+				
20Ne6+				
40Ar12+				
56Fe15+				
82Kr22+				
131Xe35+				

Tab. 15: Error Maps in Mode M2b (Marching with Initialisation)

Notice: The error maps do not show the complete operated adress range of 32M, but only up to about 29M.

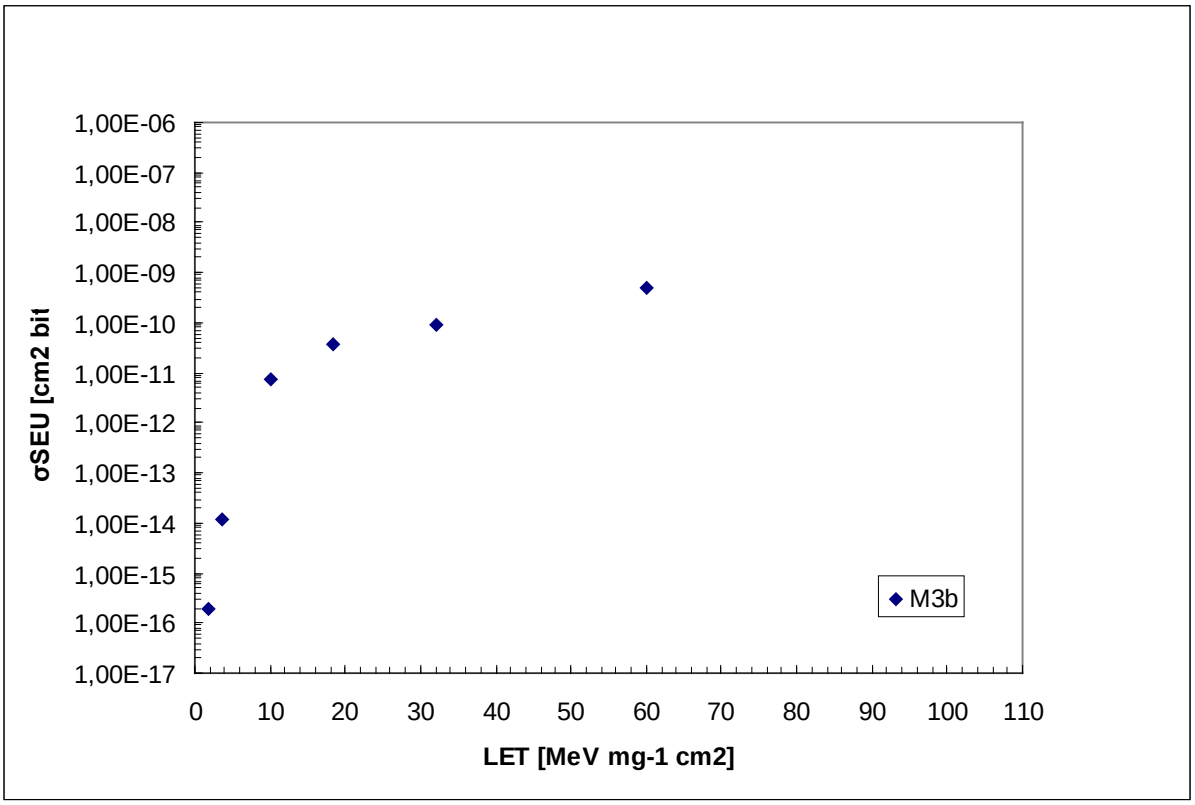


Fig. 1: Raw Cross section of single bit errors in Mode M3b

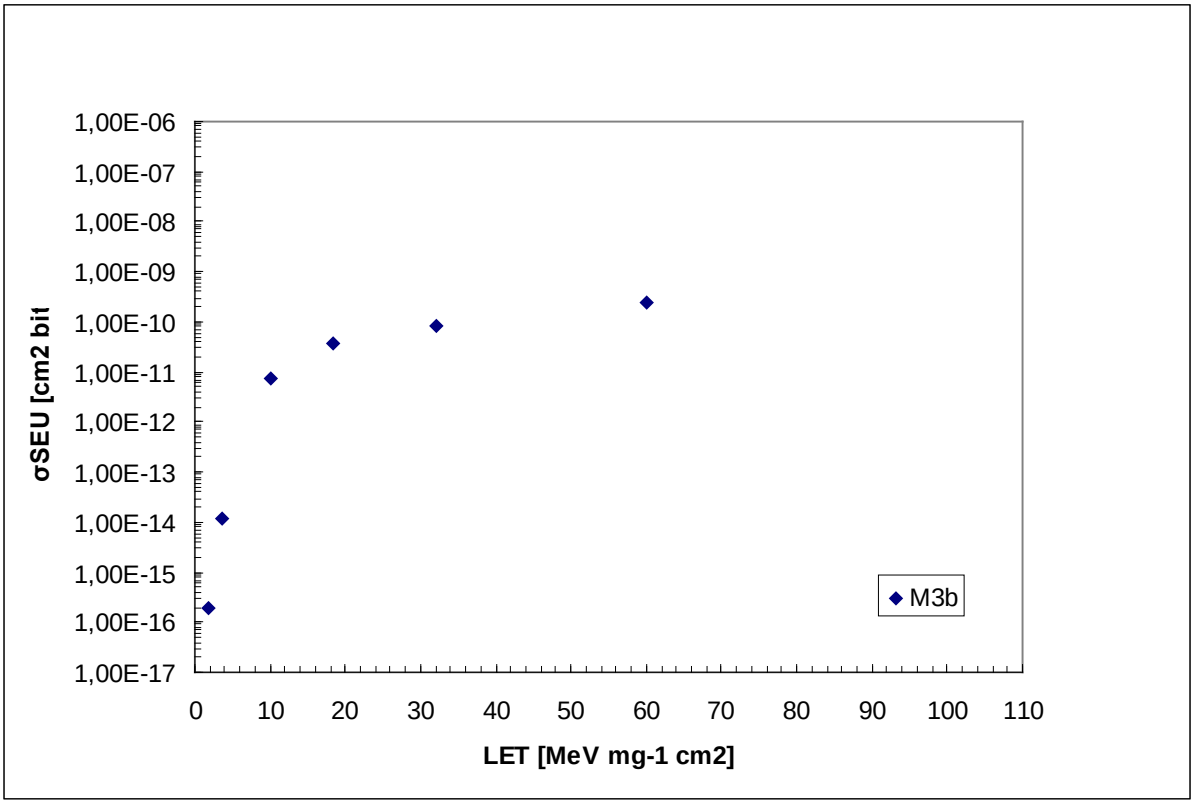


Fig. 2: Cleaned Cross section of single bit errors in Mode M3b

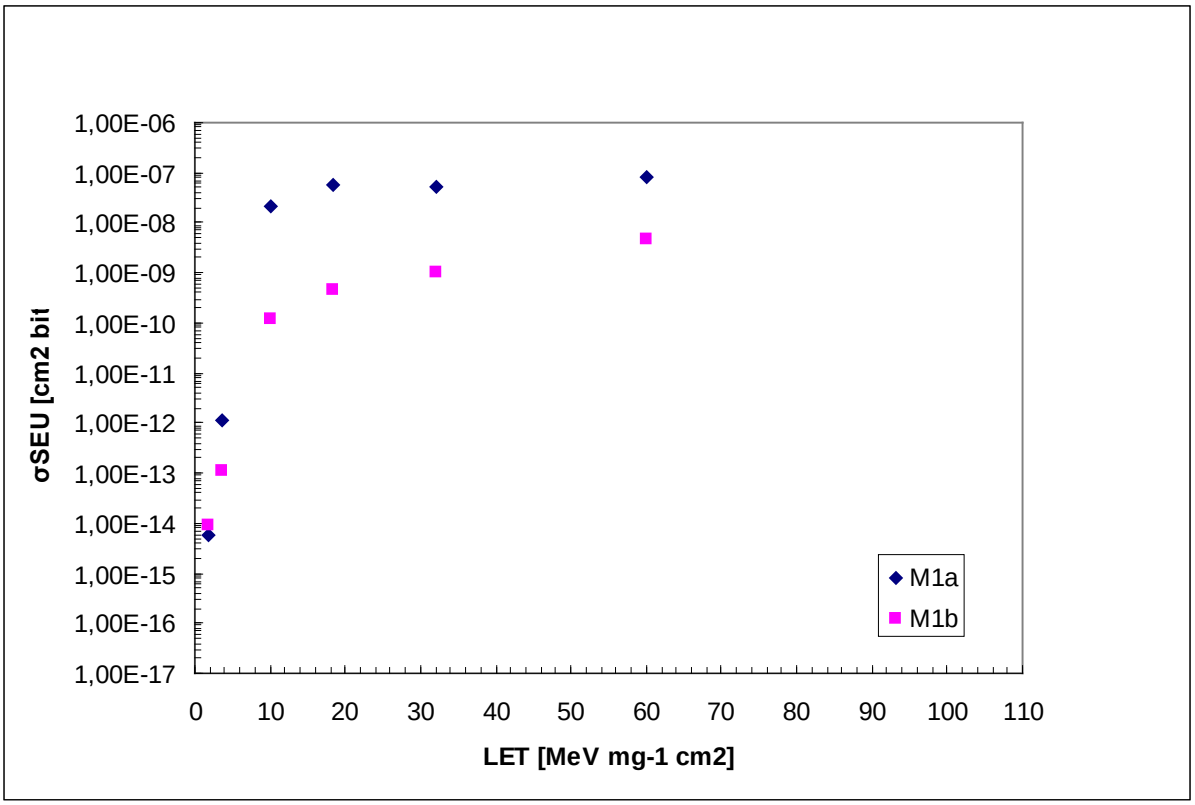


Fig. 3: Raw Cross section of single bit errors in Mode M1

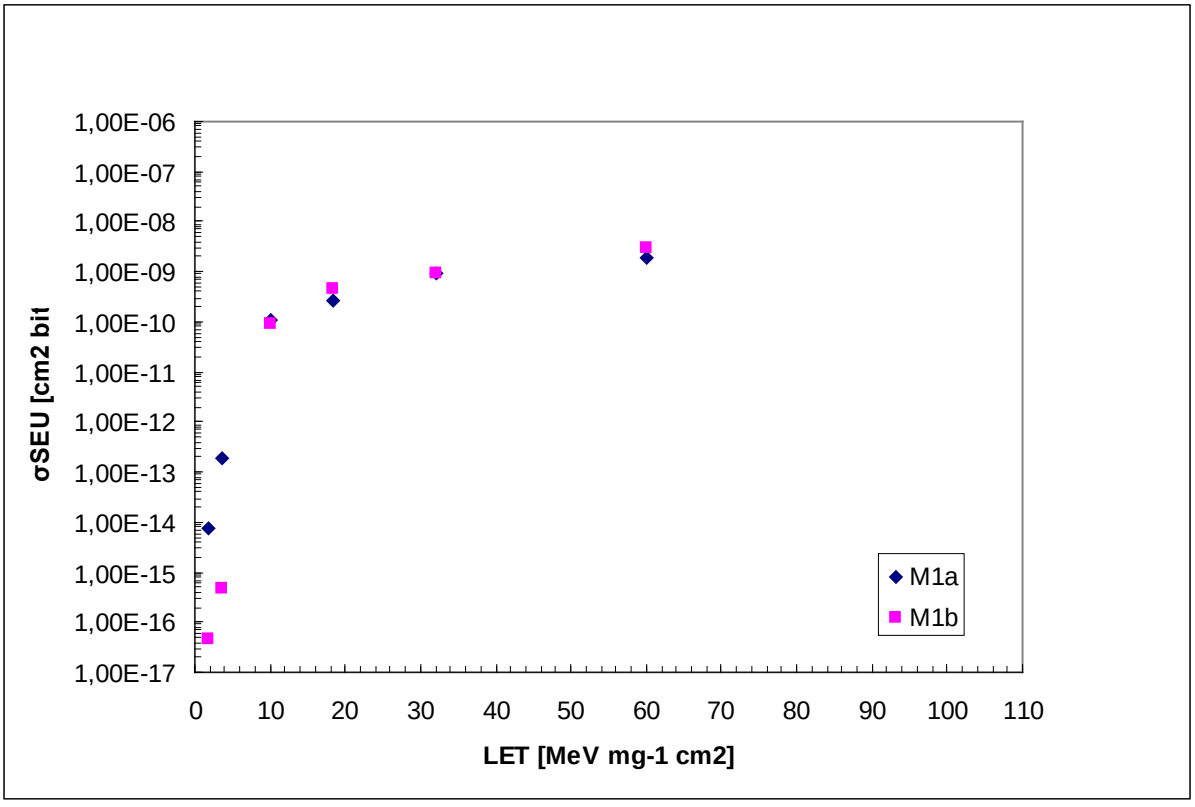


Fig. 4: Cleaned Cross section of single bit errors in Mode M1

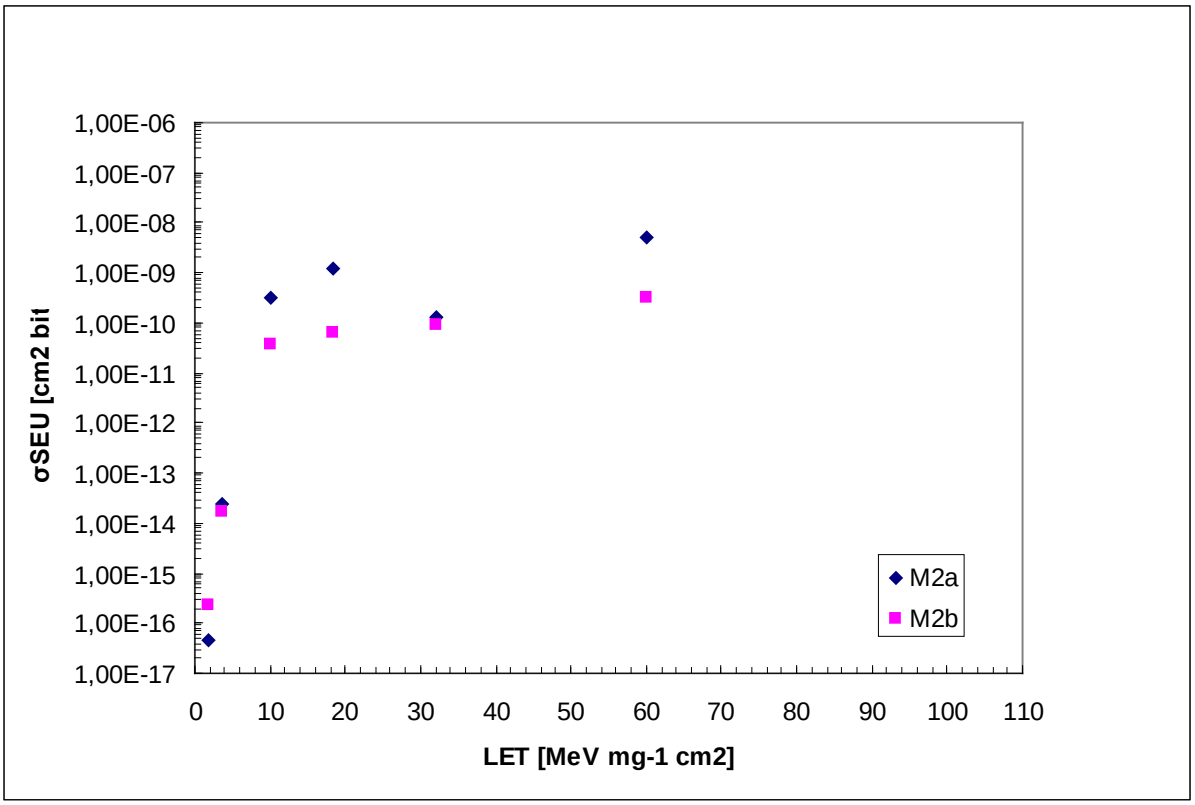


Fig. 5: Raw Cross section of single bit errors in Mode M2

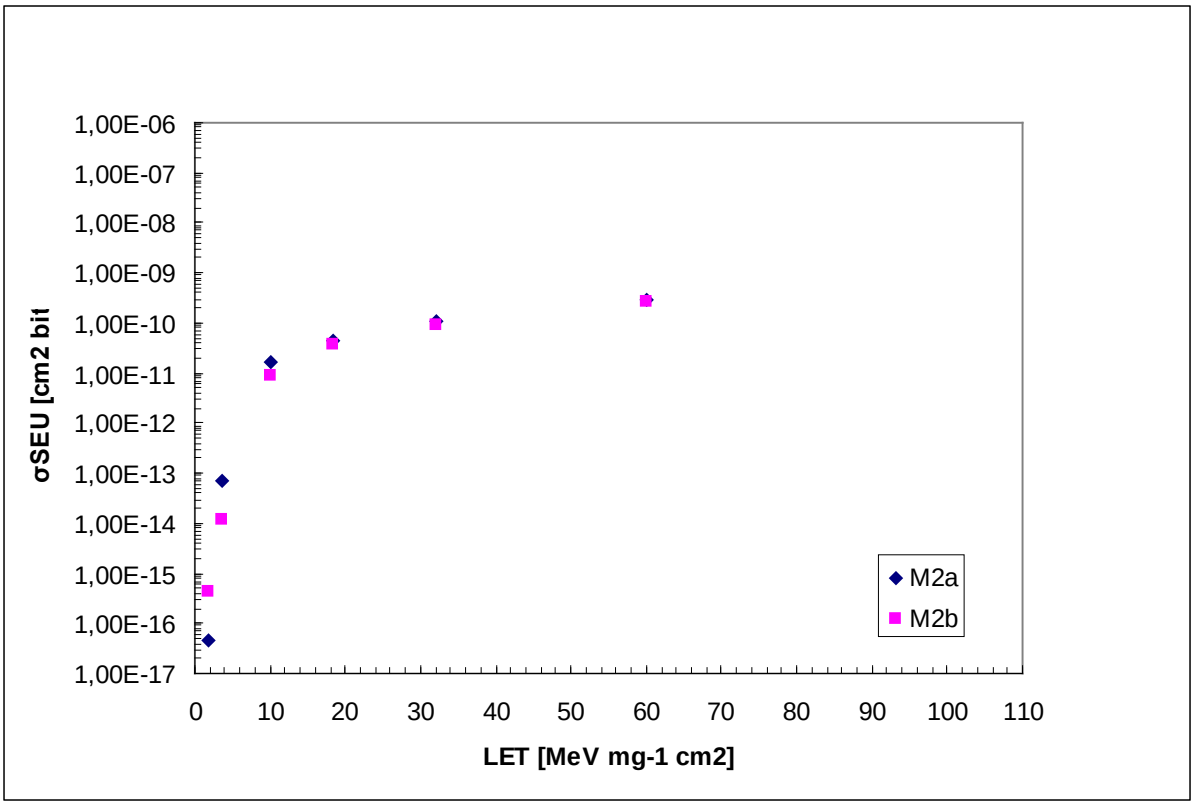


Fig. 6: Cleaned Cross section of single bit errors in Mode M2

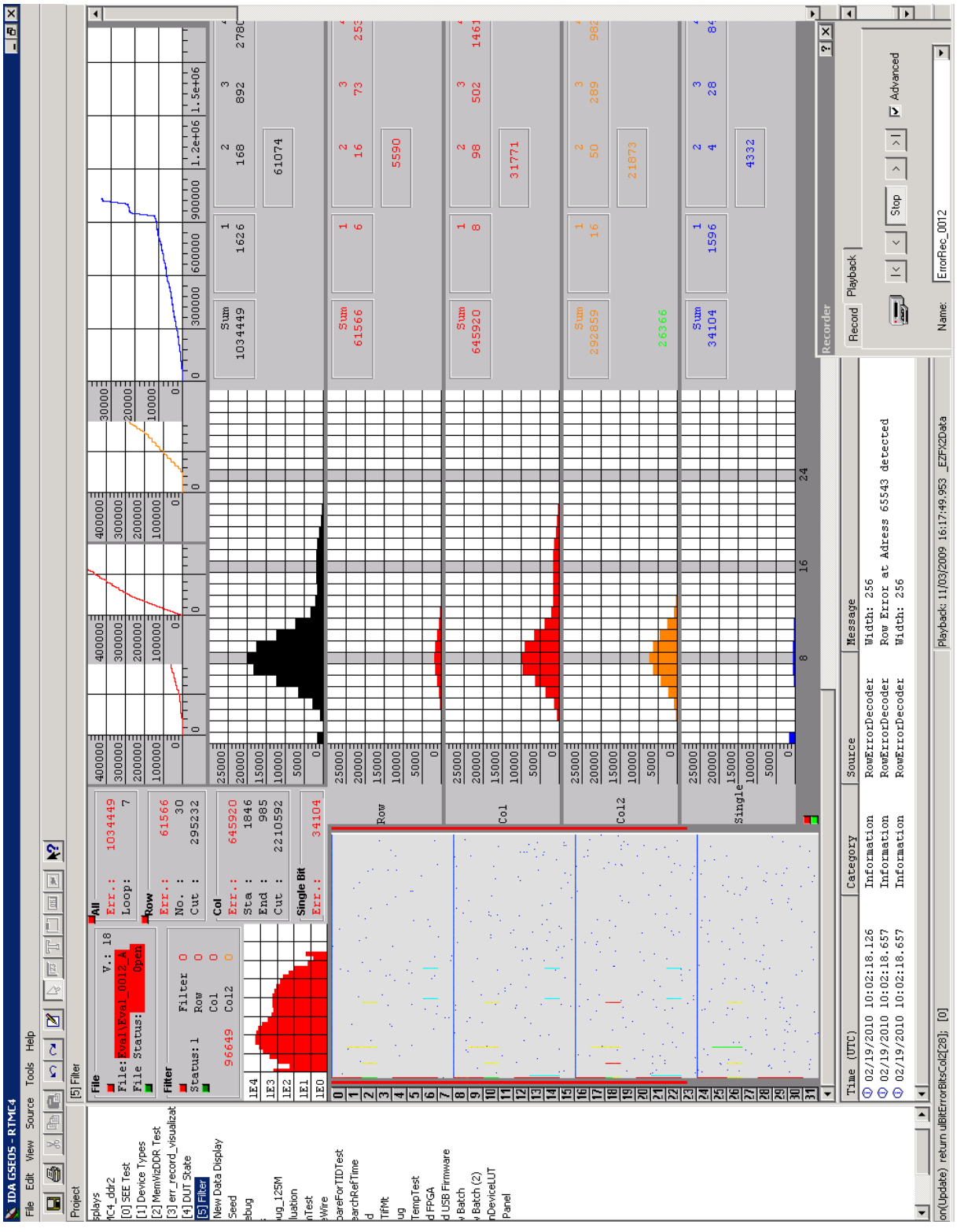


Fig. 7: Screen of the GSEOS Filter Program

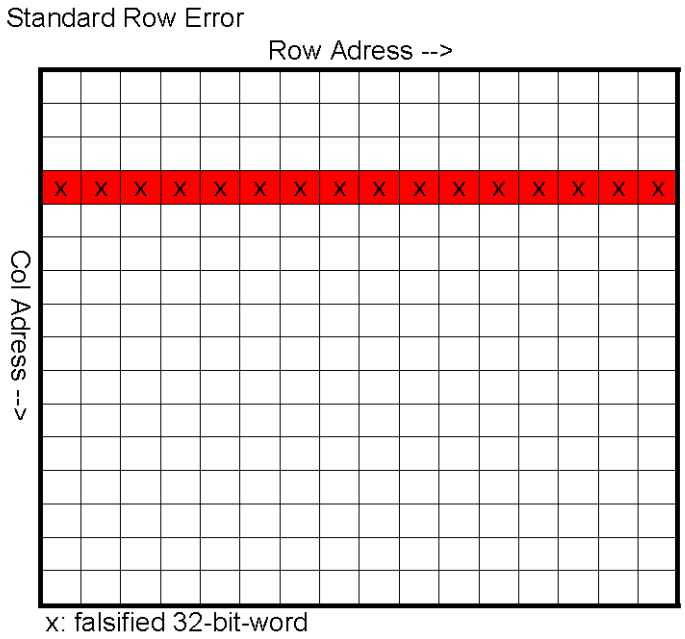


Fig. 8: Standard Row Error

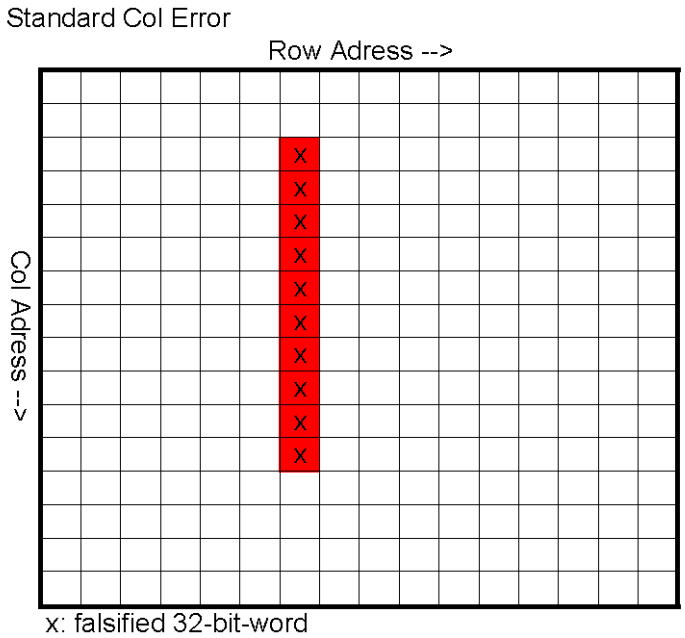


Fig. 9: Standard Col Error

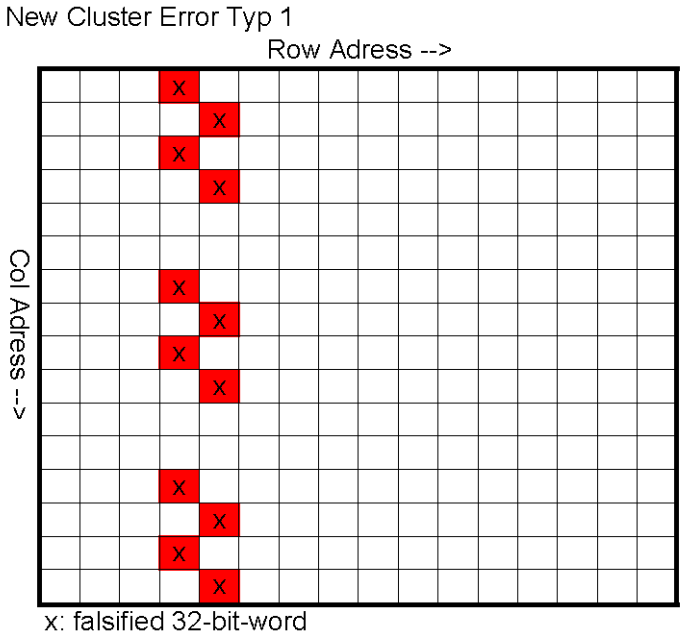


Fig. 10: New Cluster Error Typ 1

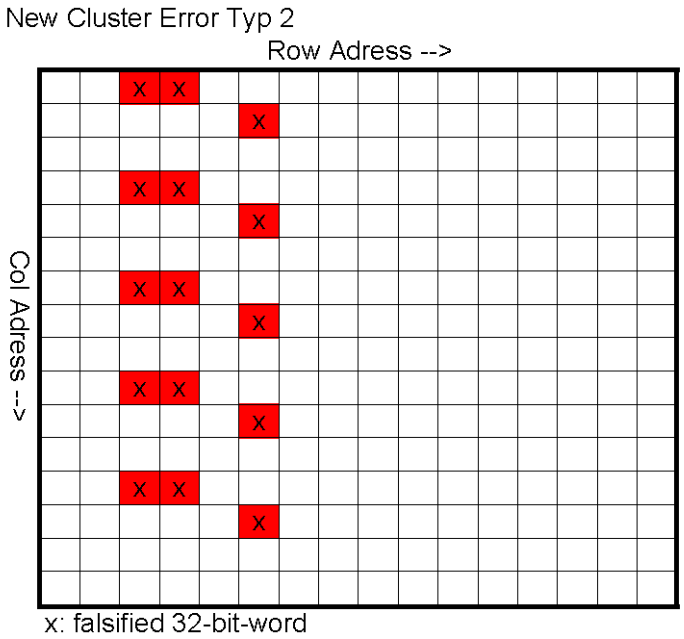


Fig. 11: New Cluster Error Typ 2