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TN-IDA-RAD-10/6C

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Dependence of the Samsung and Micron 8-Gbit NAND-Flash SEU Rate on the Incidence Angle of Heavy Ions

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Contents

Change Record

TN-IDA-RAD 10/6A:	Chapter8: Fig. 34 and Tab. 13 added
TN-IDA-RAD-10/6B	Chapter 3: Fig. 1a added, Chapter 10: references added
TN-IDA-RAD-10/6C	Chapter 10: Reference 3 corrected

1. Introduction

NAND-Flash provides non-volatility and the highest storage density of today’s semiconductor memory technologies. Therefore, for space borne mass memories NAND-Flash became a serious competitor to the traditional DRAM technology. Alike DRAM devices the NAND-Flash devices are sensitive also to Single Event Effects induced by energetic particles of the space environment.

In space the particle flux is omni-directional. In contrast, on ground most heavy ion tests are performed with ion incidence normal to the surface of the DUT. Sometimes, the memory die is tilted by $\alpha = 45^\circ$ or 60° around one die axes, mostly in order to simulate ions of larger LET according to the cosine law $LET_{eff} = LET / \cos \alpha$. This relation has been derived for sensitive volumes of planar shape and is very in question for today’s 3-D structures [1].

In April 2010 we tested the angular dependence of the SEU cross section of state of the art 8-Gbit NAND-Flash devices. For that purpose we mounted the DUTs on a remote controlled gimballed fixture for particle incidence selectable within a cone of 75° aperture angle. Accordingly, the particle direction is described by two angles, namely the azimuth angle θ and the elevation angle ψ (Fig. 1).

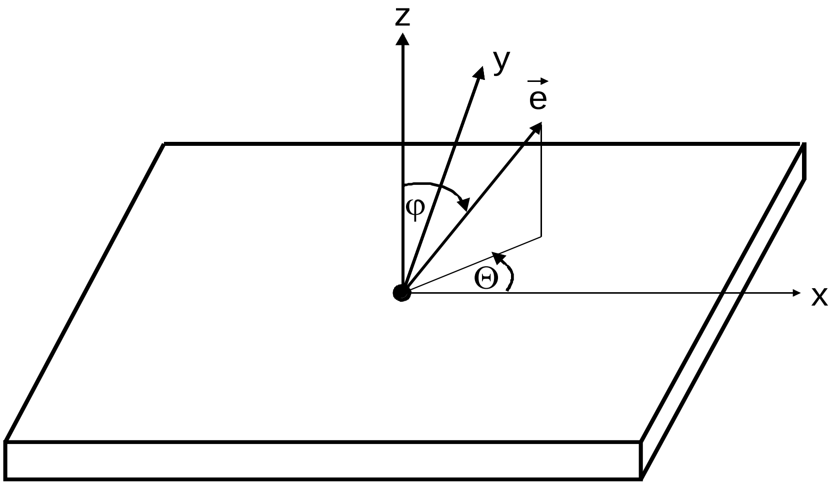

Fig. 1: Definition of the Polar Coordinate System

The unity vector $\mathbf{e}(\theta, \psi)$ is in parallel to the incident particles. The direction $\theta = 0^\circ$, $\psi = 90^\circ$ coincides with the long die axes x.

2. Test Preparation and Execution

Samples of the 8-Gbit Samsung NAND-Flash and of the 8-Gbit Micron NAND Flash (Tab. 1) were opened by nitric acid etching. The proper function was tested before and after the opening procedure.

These devices are organized into 4096 blocks of 64 pages, each. The page contains 4kbytes plus some spare bytes.

Due to the limited beam time only a fraction of the blocks (either 256 or 128 or 64 blocks out of 4k blocks) of only one sample of one Samsung and one Micron sample could be tested with only one ion species (40Ar12+, E = 372 MeV, LET = 10.1 MeV cm^2 mg^{-1}, Range = 118 µm).

DUT ID	Device Type	Date Code
SI18	Samsung K9WBG08U1M	0837
MC6	Micron MT29F8G08AAA	0846

Tab. 1: List of DUTs

The tests were performed at the RADEF facility of the University of Jyväskylä, Finland [2]. Before exposure the DUT is rotated into its new position, the blocks to be exercised are erased and a checkerboard pattern is written into these blocks. No access operations are performed during exposure of the biased device (Storage Mode M3a). After beam stop the data are read and checked for errors. All error vectors are recorded for later evaluation. Quick Look displays (error map, error counts, and error statistics) provide real time control of the test execution.
The applied static mode operation tests only the array of Floating Gate Transistors, but not the peripheral circuitry. It simulates the typical situation in space applications.

3. Angular Dependence of the SEU Cross Section of the Samsung 8-Gbit NAND-Flash

The SEU Cross Section is calculated as

$$\begin{aligned}\sigma &= \frac{SEU\ Count}{Fluence} * \frac{Total\ Count\ of\ Blocks}{Count\ of\ \mathrm{Re}ad\ Blocks}\left[cm^2/dev\right]\\ &= \frac{SEU\ Count}{1.0E6\,cm^{-2}} * \frac{4096}{either\ 256\ or\ 128\ or\ 64}\left[cm^2/dev\right]\end{aligned} \qquad (3.1)$$

The fluence was chosen to 1.0 E+6 cm^{-2} ions. Mostly 64 blocks were exercised, and 256 blocks in case of low SEU counts. The SEU count ranged between 50 and several thousands, which limits the error bars to maximum ± 15 %.

Tab. 2 shows the exposure sequence.

Each fluence portion of 1.0E+6 cm^{-2} Ar ions delivered a dose portion of

$$\begin{aligned}\Delta\ \mathrm{TID} &= 1.6\mathrm{E}{-5} * \mathrm{LET}\ [\mathrm{MeV\ cm^2\ mg^{-1}}] * \mathrm{F}\ [\mathrm{cm^{-2}}]\ \mathrm{rad}\\ &= 1.6\mathrm{E}{-5} * 10.1 * 1.0\mathrm{E}{+6}\ \mathrm{rad} = 162\ \mathrm{rad}\end{aligned}$$

Including the exposure at normal incidence the DUT accumulated in the course of 121 exposures a total dose of

$$\mathrm{TID} = 121 * \Delta\,\mathrm{TID} = 121 * 162\ \mathrm{rad} = 19.6\ \mathrm{krad}$$

Azimuth Quadrant	Elevation Angle ψ	Azimuth Angles Θ
I	15°	Θ = 0°, 15° , 30°, 45°, 60°, 75°
	30°	Θ = 0°, 15° , 30°, 45°, 60°, 75°
	45°	Θ = 0°, 15° , 30°, 45°, 60°, 75°
	60°	Θ = 0°, 15° , 30°, 45°, 60°, 75°
	75°	Θ = 0°, 15° , 30°, 45°, 60°, 75°
III	15°	Θ = 180°, 195° , 210°, 225°, 240°, 255°
	30°	Θ = 180°, 195° , 210°, 225°, 240°, 255°
	45°	Θ = 180°, 195° , 210°, 225°, 240°, 255°
	60°	Θ = 180°, 195° , 210°, 225°, 240°, 255°
	75°	Θ = 180°, 195° , 210°, 225°, 240°, 255°
IV	15°	Θ = 345°, 330° , 315°, 300°, 285°, 270°
	30°	Θ = 345°, 330° , 315°, 300°, 285°, 270°
	45°	Θ = 345°, 330° , 315°, 300°, 285°, 270°
	60°	Θ = 345°, 330° , 315°, 300°, 285°, 270°
	75°	Θ = 345°, 330° , 315°, 300°, 285°, 270°
II	15°	Θ = 165°, 150° , 135°, 120°, 105°, 90°
	30°	Θ = 165°, 150° , 135°, 120°, 105°, 90°
	45°	Θ = 165°, 150° , 135°, 120°, 105°, 90°
	60°	Θ = 165°, 150° , 135°, 120°, 105°, 90°
	75°	Θ = 165°, 150° , 135°, 120°, 105°, 90°

Tab. 2: Exposure Sequence of the Samsung 8-Gbit NAND-Flash

The measured cross sections $\sigma(\theta,\psi)$ are listed in Tab. 3.

Θ [°]		σ [1E-3 cm^2]					Av. 15° -60°
	ψ =0°	15°	30°	45°	60°	75°	
0	7.86	6.22	8.18	7.30	6.14	(14.7)	
15		5.53	9.14	6.27	7.56	(24.5)	
30		5.47	7.10	5.50	7.81	(35.5)	
45		5.18	5.56	4.54	8.38	(41.2)	
60		5.63	5.12	3.26	4.86	55.4	
75		7.61	2.85	1.47	1.50	14.9	
Av. I		*5.94*	*6.32*	*4.72*	*6.04*	*31.2*	*5.76*
90		6.71	3.08	1.44	1.10	1.38	
105		6.27	2.34	1.12	1.38	8.41	
120		4.99	3.20	1.22	3.07	30.7	
135		4.61	5.50	3,84	5.76	38.8	
150		4.74	6.27	5.44	6.66	33.4	
165		5.18	6.14	6.53	5.67	19.6	
Av. II		*4.30*	*4.42*	*3.27*	*3.94*	*22.0*	*3.98*
180		5.06	7.30	7.17	5.18	14.7	
195		6.72	6.66	6.40	6.66	24.5	
210		5.76	7.74	5.16	6.72	35.5	
225		5.18	4.99	3.33	6.08	41.2	
240		6.27	3.58	2.69	3.90	31.9	
255		5.70	3.14	1.06	1.44	9.82	
Av. III		*5.78*	*5.57*	*4.40*	*4.83*	*26.3*	*5.13*
270		5.86	3.25	1.17	(1.10)	1.36	
285		5.54	2.37	1.31	1.12	9.18	
300		3.71	3.39	1.86	4.74	33.3	
315		5.12	5.44	4.03	6.34	(41.2)	

330		5.50	5.57	5.63	7.17	(35.5)	
345		4.54	6.72	6.85	6.08	(24.5)	
Av. IV		*5.05*	*4.46*	*3.48*	*4.42*	*24.2*	*4.35*
Av. I – IV	*7.86*	*5.27*	*5.19*	*3.97*	*4.81*	*25.9*	

Tab. 3: Measured SEU Cross Sections σ(Θ,ψ) [1E-3 cm^2] of the Samsung 8-Gbit NAND-Flash

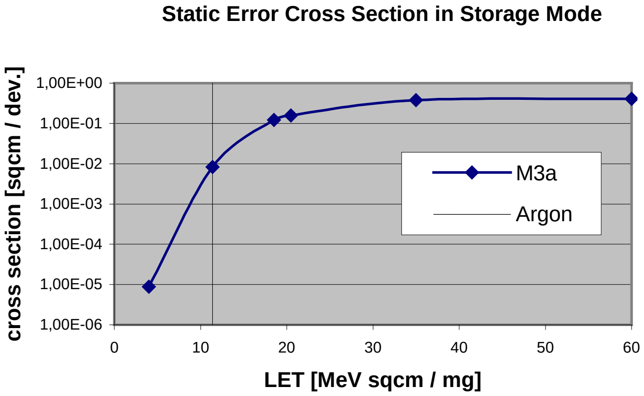

Fig. 1a: Static Cross Section of the Samsung 8-Gbit NAND-Flash K9WBG08U1M, lot code FFC04X1 at normal incidence [source TN-IDA-RAD-09/3C, Fig 6, sqcm / bit converted into sqcm / dev.]

Fig. 1a shows the Static Cross Section of the Samsung 8-Gbit NAND-Flash at normal ion incidence. In the following we focus on the angular dependence of the cross section at Argon.

The five polar diagrams in Fig. 2 – 6 show the cross section for the five elevation angles ψ = 15°, 30°, 45°, 60° and 75°

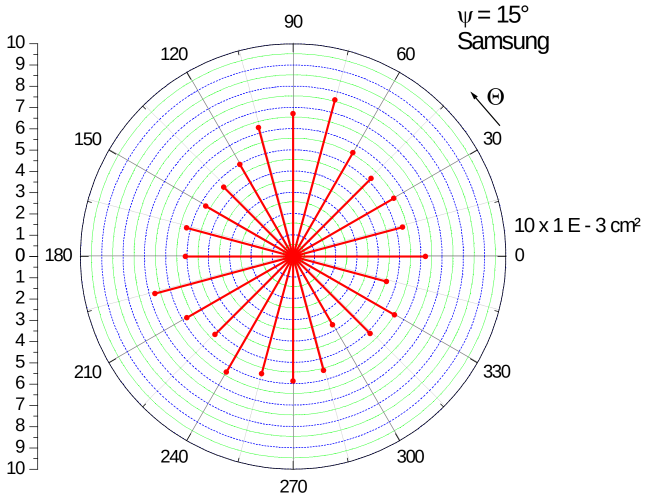

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Fig.2: SEU Cross Section σ(θ) [1E-3 cm^2] at ψ = 15° of the Samsung 8-Gbit NAND-Flash

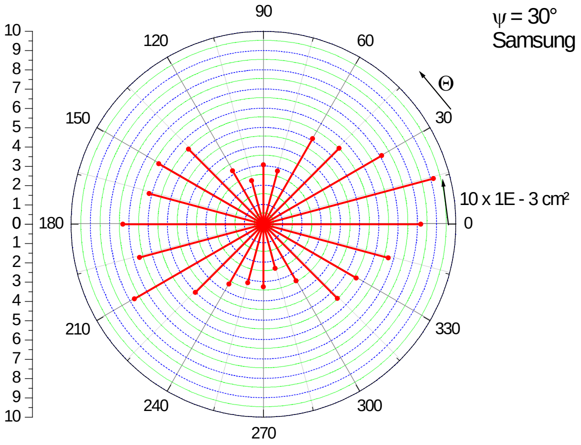

Fig.3: SEU Cross Section σ(θ) [1E-3 cm^2] at ψ = 30° of the Samsung 8-Gbit NAND-Flash

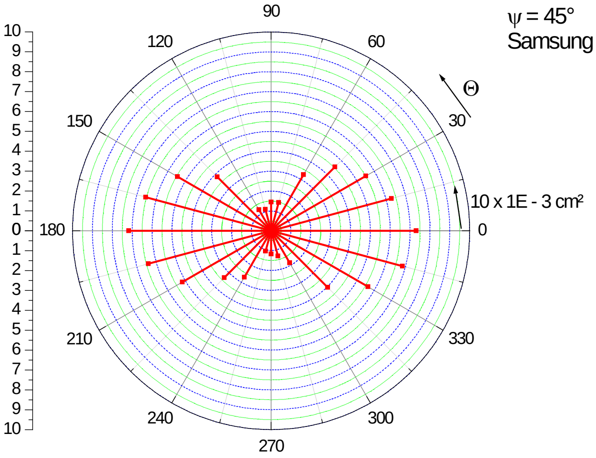

Fig.4: SEU Cross Section σ(θ) [1E-3 cm^2] at ψ = 45° of the Samsung 8-Gbit NAND-Flash

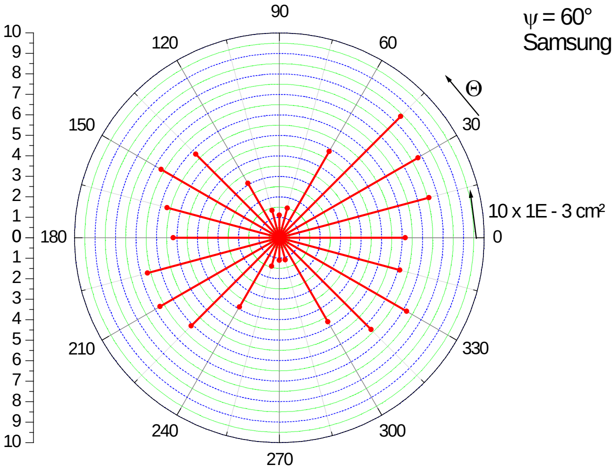

Fig.5: SEU Cross Section σ(θ) [1E-3 cm^2] at ψ = 60° of the Samsung 8-Gbit NAND-Flash

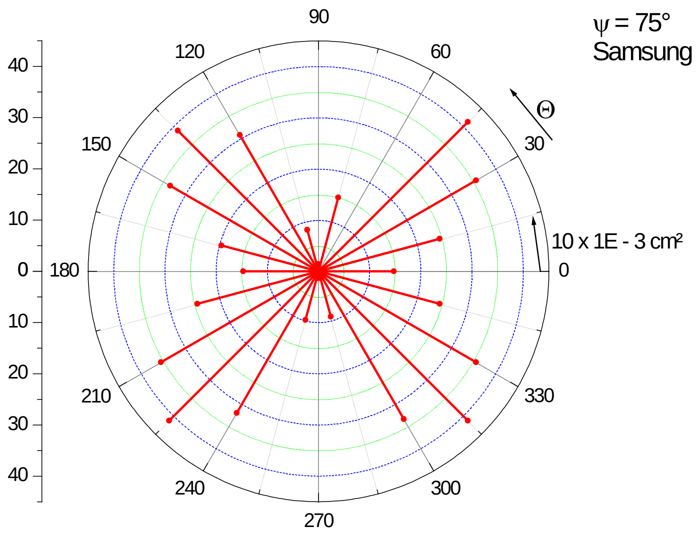

Fig.6: SEU Cross Section σ(θ) [1E-3 cm^2] at ψ = 75° od the Samsung 8-Gbit NAND-Flash

Fig. 7 … 11 show the cross section profile σ(ψ) for a given azimuth angle θ.

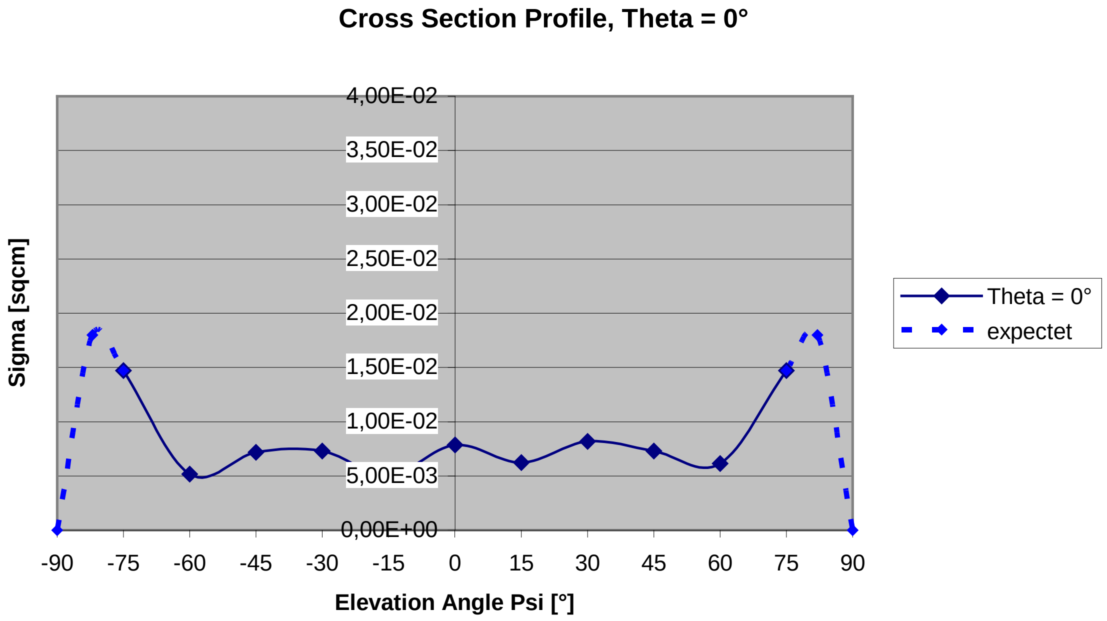

Fig. 7: Cross Section profile σ(ψ), θ = 0°, Samsung 8-Gbit NAND-Flash
Notice: ψ = - 45°, θ = 0° is equivalent to ψ = + 45°, θ = 180°

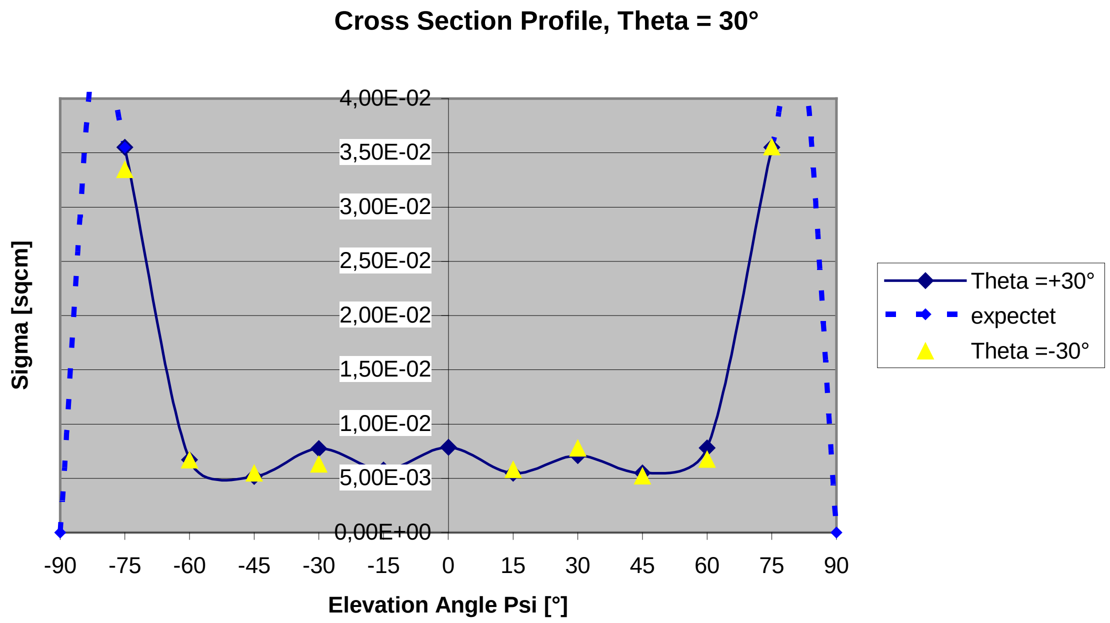

Fig. 8: Cross Section profile $\sigma(\psi)$, $\theta = 30°$, Samsung 8-Gbit NAND-Flash
Notice: $\psi = -45°$, $\theta = +30°$ is equivalent to $\psi = +45°$, $\theta = 210°$,
$\psi = -45°$, $\theta = -30°$ is equivalent to $\psi = +45°$, $\theta = 150°°$

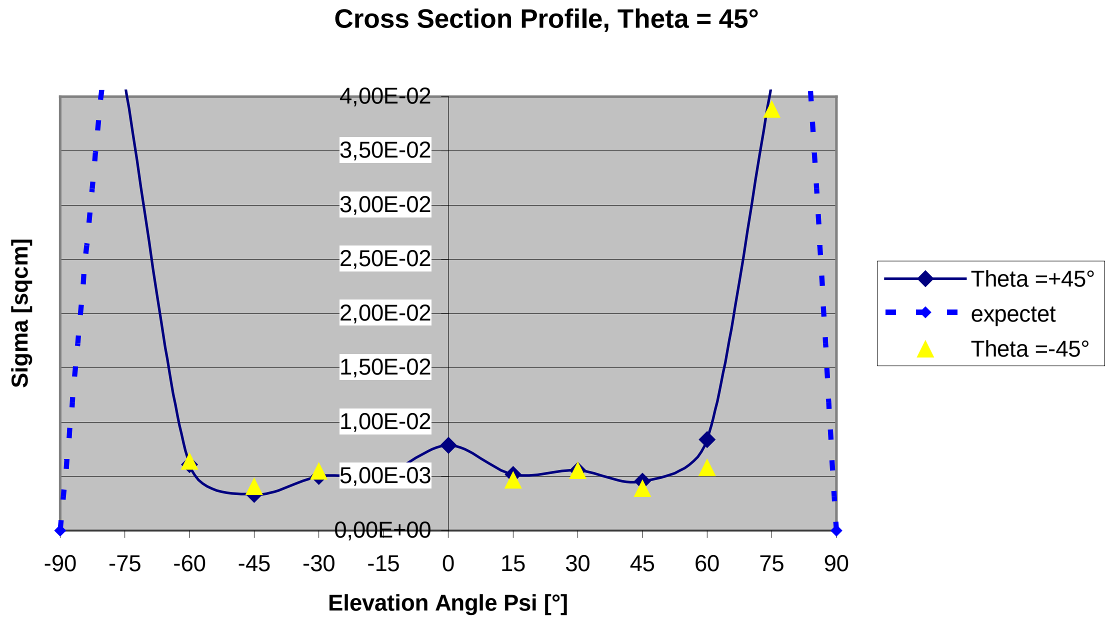

Fig. 9: Cross Section profile $\sigma(\psi)$, $\theta = 45°$, Samsung 8-Gbit NAND-Flash
Notice: $\psi = -45°$, $\theta = 45°°$ is equivalent to $\psi = +45°$, $\theta = 225°$
$\psi = -45°$, $\theta = -45°°$ is equivalent to $\psi = +45°$, $\theta = 135°$

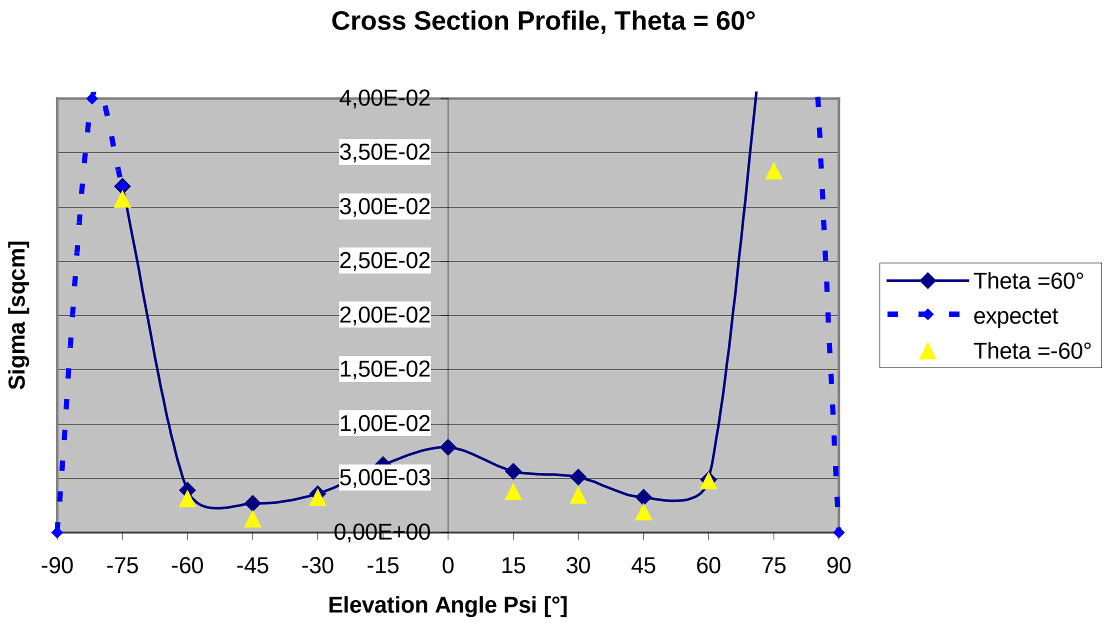

Fig. 10: Cross Section profile σ(ψ), θ = 60°, Samsung 8-Gbit NAND-Flash
Notice: ψ = - 45°, θ = 60° is equivalent to ψ = + 45°, θ = 240°
ψ = - 45°, θ = -60° is equivalent to ψ = + 45°, θ = 120°°

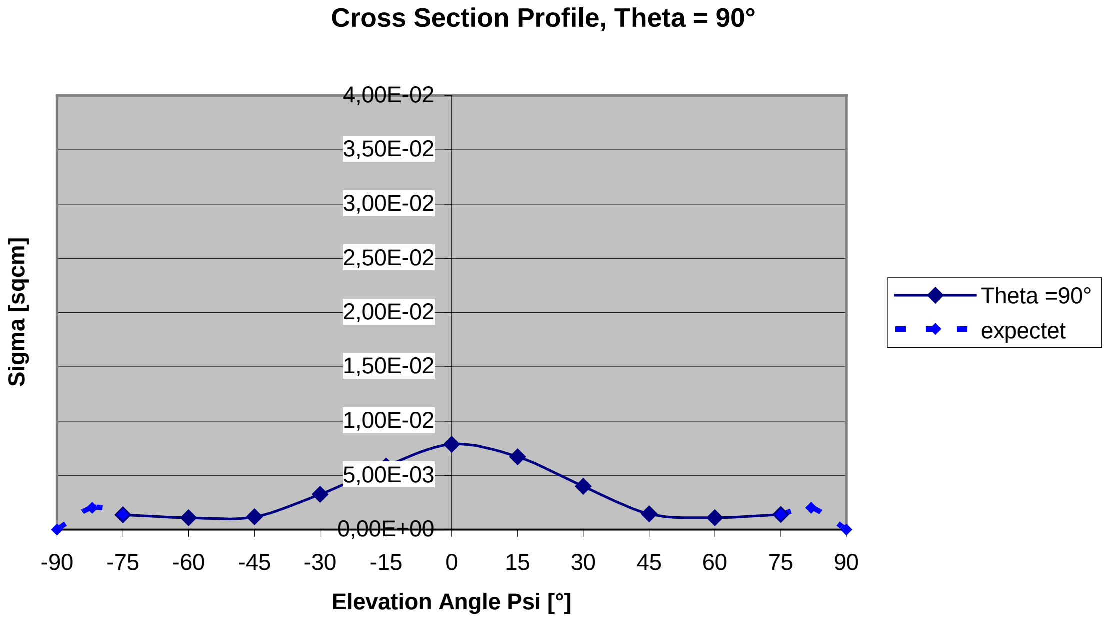

Fig. 11: Cross Section profile σ(ψ), θ = 90°, Samsung 8-Gbit NAND-Flash
Notice: ψ = - 45°, θ = 90° is equivalent to ψ = + 45°, θ = 270°

The polar SEU cross section diagram at the low inclination of ψ = 15° is nearly a circle.
The radius vectors shrink slightly in line with the applied fluence, i.e. from quadrant I to quadrant III, quadrant IV and finally to quadrant II.
This effect is more pronounced for the Micron device and therefore, will be discussed there.

With increasing inclination the diagram mutates to an “antenna diagram” with maximum cross section at $\theta = 0^\circ$ and 180° (= long die axes) and minimum cross section at 90° and 270° (= short die axes).

At very slant incidence ($\psi = 60^\circ \rightarrow 75^\circ$) the cross section increases significantly, but maintains the directional sensitivity of the “antenna diagram”.

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At $\psi = 75^\circ$ the cross sections from $\theta = -45^\circ$ until $+45^\circ$ could not be measured because of obstruction by the cabling. Also, inclinations of more than 75° could not be reached with the used tilting set up.

Most likely this part in the right half plane will be more or less symmetrical to the left half plane.

Meanwhile an improved tilting set up has been built for non-obstructed tilting for all azimuth angles up to 90° elevation, in order to investigate the cross section diagram at gracing incidence angles..

Fig. 7 – 11 show profiles of the SEU cross section along the azimuth axes

$\Theta = 180^\circ, 0^\circ$		(Fig. 7)
$\Theta = 210^\circ, 30^\circ$	and $150^\circ, -30^\circ$	(Fig. 8)
$\Theta = 225^\circ, 45^\circ$	and$135^\circ, -45^\circ$	(Fig. 9)
$\Theta = 240^\circ, 60^\circ$	and$112^\circ, -60^\circ$	(Fig. 10)
$\Theta = 270^\circ, 90^\circ$		(Fig. 11)

For $\Theta = \pm 30^\circ$ until $\pm 60^\circ$ we see “butterfly” profiles with minor variations until $|\psi| \leq 60^\circ$.

$\Theta = 0^\circ$ shows also a “butterfly” profile, but with a less pronounced wing size.

$\Theta = 90^\circ$ shows a “Gauss” profile with stunted wings.

The device shows a pronounced dependence of the SEU cross section on the direction of the incident particles.

Maximum sensitivity is reached for directions within the forward and backward $\theta = \pm 60^\circ$ sector.
Minimum sensitivity is reached for directions within the forward and backward $\theta = 90^\circ \pm 30^\circ$ sector.

For the profiles crude assumptions (depicted by broken lines) have been made for very slant incidence ($\psi > 75^\circ$).

Cross sections of this grazing incidence region still have to be measured. This can be done by means of our new upgraded DUT fixture.

4. Angular Dependence of the SEU Cross Section of the Micron 8-Gbit NAND-Flash

The test of the Micron device delivered the polar cross section diagrams in Fig. 12 – 16.

Apparently the SEU cross section (Tab. 4, Fig. 12 – 16) shrinks with the progress in exposure (Tab. 3), i.e. with increasing fluence, but much more significantly than it was already noticed for the Samsung device (Fig. 2 – 6). This behaviour points to a TID related effect, which surprisingly improves the cross section during the dose increase up to about 20 krad. Possibly this behaviour is caused by minor threshold shift with favourable effect at least at room temperature.

Azimuth Quadrant	Elevation Angle ψ	Azimuth Angles Θ
I	15°	Θ = 0°, 15° , 30°, 45°, 60°, 75°,90°
	30°	Θ = 0°, 15° , 30°, 45°, 60°, 75°,90°
	45°	Θ = 0°, 15° , 30°, 45°, 60°, 75°,90°
	60°	Θ = 0°, 15° , 30°, 45°, 60°, 75°, 90°
	75°	Θ = 60°, 75°, 90°
II	15°	Θ = 180°, 165° , 150°, 135°, 120°, 105°
	30°	Θ = 180°, 165° , 150°, 135°, 120°, 105°
	45°	Θ = 180°, 165° , 150°, 135°, 120°, 105°
	60°	Θ = 180°, 165° , 150°, 135°, 120°, 105°
	75°	Θ = 180°, 165° , 150°, 135°, 120°, 105°
III	15°	Θ = 195° , 210°, 225°, 240°, 255°
	30°	Θ = 195° , 210°, 225°, 240°, 255°
	45°	Θ = 195° , 210°, 225°, 240°, 255°
	60°	Θ = 195° , 210°, 225°, 240°, 255°
	75°	Θ = 195° , 210°, 225°, 240°, 255°
IV	15°	Θ = 165°, 150° , 135°, 120°, 105°
	30°	Θ = 165°, 150° , 135°, 120°, 105°
	45°	Θ = 165°, 150° , 135°, 120°, 105°
	60°	Θ = 165°, 150° , 135°, 120°, 105°
	75°	Θ = 165°, 150° , 135°, 120°, 105°

Tab. 3: Exposure Sequence, Micron 8-Gbit NAND-Flash

Θ [°]		σ [1E-2 cm²]											Av. 15° - 60° meas
		ψ =0°	15°		30°		45°		60°		75°		
			meas.	corr.	meas.	corr.	meas.	corr.	Meas.	corr.	Meas.	corr.	
I	0	7.90	7.35		7.03		6.53		6.24				
	15		6.99		6.68		6.21		5.52				
↓	30		7.18		6.10		5.32		5.35				
	45		6.69		5.71		4.72		4.93				
	60		6.61		4.72		4.08		3.94		7.14		
	75		6.13		4.67		3.17		2.67		4.64		
	90		6.48		4.35		2.80		1.55		1.83		
	Av. I		*6.78*	*6.78*	*5.61*	*5.61*	*4.69*	*4.69*	*4.31*	*4.31*			*5.35*
II	90		3.78	5.56	2.65	3.90	1.63	2.40	0.93	1.37	1.04	1.53	
	105		3.87	5.69	2.90	4.26	1.98	2.91	1.69	2.48	3.00	4.41	
↑	120		3.78	5.56	3.34	4.91	2.60	3.82	2.84	4.17	4.81	7.07	
	135		4.17	6.13	3.90	5.73	3.80	5.59	3.82	5.62	5.49	8.07	
	150		4.45	6.54	4.40	6.47	4.08	6.00	4.02	5.91	5.91	8.69	
	165		4.66	6.85	4.65	6.84	4.59	6.75	4.23	6.22	4.91	7.22	
	180°		4.59	6.74	4.65	6.84	5.02	7.38	4.98	7.32	3.97	5.83	
	Av. II		*4.19*	*6.15*	*3.78*	*5.56*	*3.39*	*4.98*	*3.22*	*4.72*	*4.16*	*6.12*	*3.65*
III	195		3.21	6.42	3.71	7.42	3.38	6.76	3.62	7.24	4.35	8.70	
↓	210		3.26	6.52	3.17	6.34	2.98	5.96	3.28	6.56	4.46	8.92	
	225		2.75	5.50	2.82	5.64	2.64	5.28	2.65	5.30	4.24	8.48	
	240		2.72	5.44	2.35	4.70	1.89	3.78	2.08	4.16	4.44	8.88	
	255		2.49	4.98	1.94	3.88	1.39	2.78	1.27	2.54	2.37	4.74	
	Av. III		*2.89*	*5.78*	*2.80*	*5.60*	*2.46*	*4.91*	*2.58*	*5.16*	*3.97*	*7.94*	*2.68*
IV	270												
	285		2.43		1.73		1.27		1.16		2.16		
↑	300		2.46		2.02		1.89		2.07		3.97		
	315		2.68		2.45		2.59		3.05				

	330		2.89		3.24		2.84		3.29				
	345		3.00		3.31		3.35		3.62				
	Av. IV		*2.69*	*5.60*	*2.55*	*5.30*	*2.39*	*4.97*	*2.64*	*5.49*	*3.07*	*6.38*	*2.57*
	Av. I – IV			*6.08*		*5.52*		*4.89*		*4.92*			

Tab. 4: Measured and Corrected SEU Cross Sections σ(Θ,ψ) [**1E-2** cm^2]

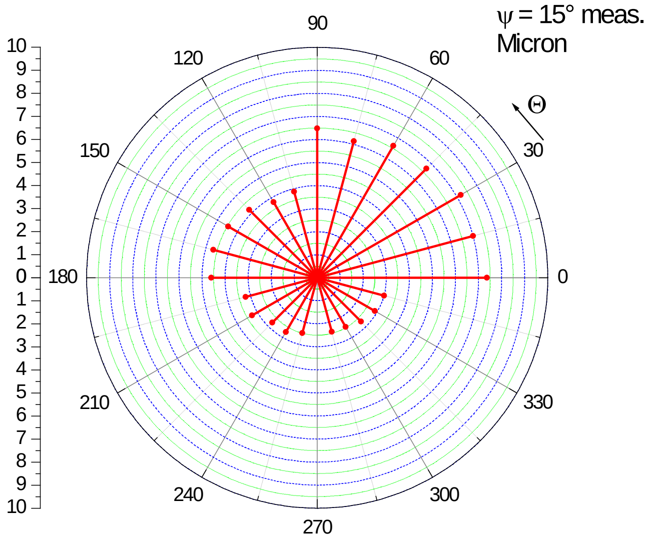

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Fig.12: Measured SEU Cross Section σ(θ) [**1E-2 cm^2**] at ψ = 15° of the Micron 8-Gbit NAND-Flash

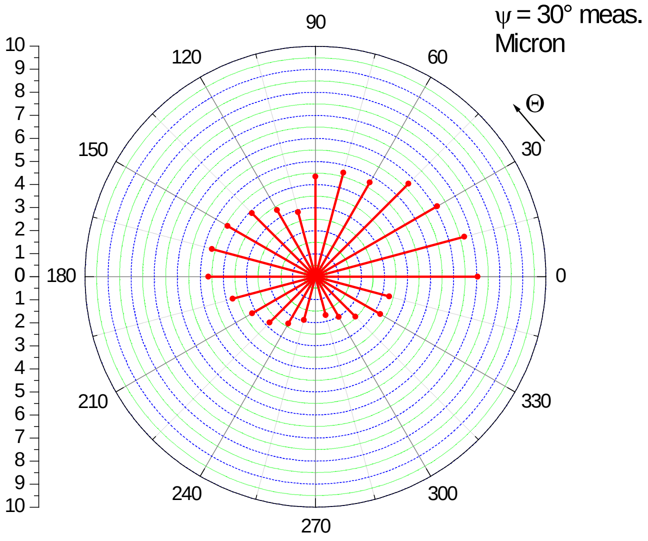


Fig.13: Measured SEU Cross Section σ(θ) [**1E-2 cm^2**] at ψ = 30° of the Micron 8-Gbit NAND-Flash

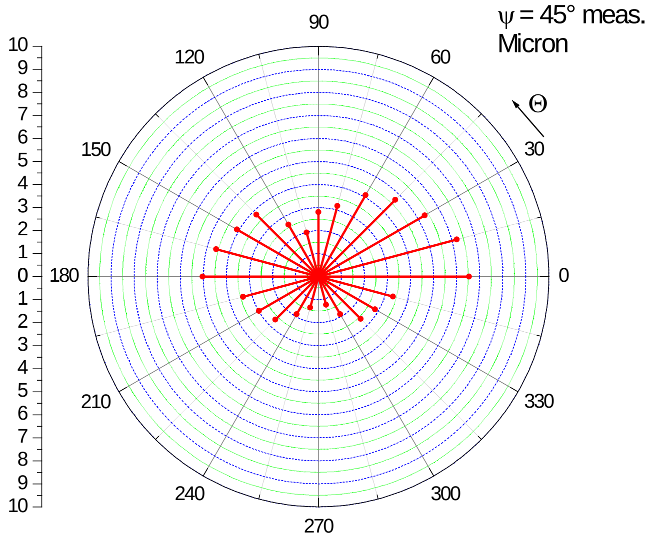


Fig.14: Measured SEU Cross Section σ(θ) [**1E-2 cm^2**] at ψ = 45°
of the Micron 8-Gbit NAND-Flash

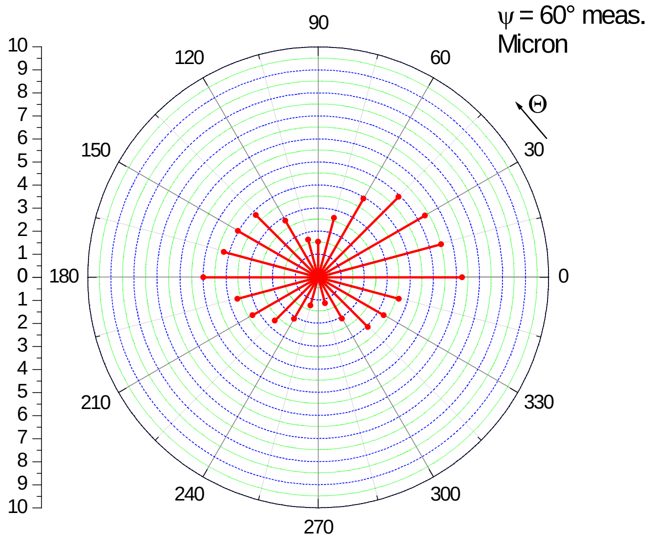


Fig.15: Measured SEU Cross Section σ(θ) [1E-2 cm^2] at ψ = 60°
of the Micron 8-Gbit NAND-Flash

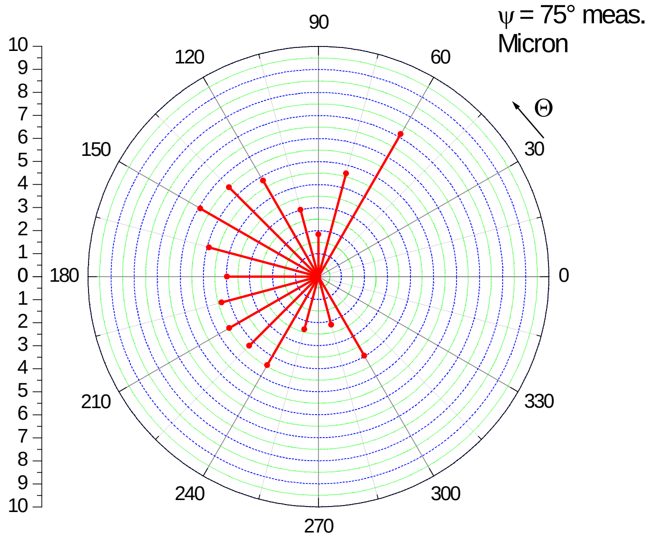


Fig.16: Measured SEU Cross Section $\sigma(\theta)$ [**1E-2 cm^2**] at $\psi = 75°$
of the Micron 8-Gbit NAND-Flash

5. Fluence / TID Dependence of the SEU Cross Section

In order to get a polar cross section diagram for fresh devices we corrected the polar measured cross section diagrams of the Micron device under the assumption of a four quadrant symmetry.

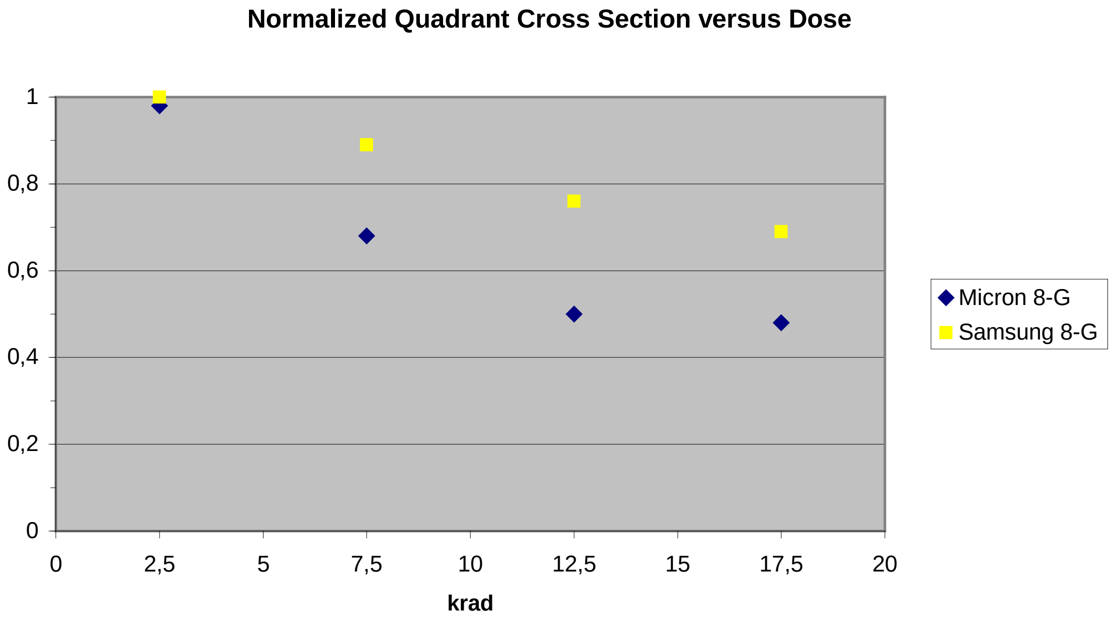
The average over the measured cross section of each azimuth quadrant σ_{qu} is shown in the last column of Tab. 4. In case of symmetry all four averages should be of the same value. But the average values shrink from quadrant to quadrant, i.e. in line with the applied fluence (Fig. 17). To compensate this fluence / dose dependent shrinkage we blew up the quadrants II, III and IV of the measured polar diagram by the correction factors

$$K_{II} = \sigma_{qu,I} / \sigma_{qu,II} = 5.35 / 3.65 = 1.47$$

$$K_{III} = \sigma_{qu,I} / \sigma_{qu,III} = 5.35 / 268 = 2.00$$

$$K_{IV} = \sigma_{qu,I} / \sigma_{qu,IV} = 5.35 / 2.57 = 2.08$$

Fig 18 – 22 show the corrected cross section diagrams and Fig. 23 – 27 the respective corrected cross section profiles along selected azimuth axes.



Micron:	I	II	III	IV
Samsung:	I	III	IV	II

Fig. 17: SEU Cross Section averaged over one quadrant versus accumulated Dose, and normalized to the average cross section of quadrant I.

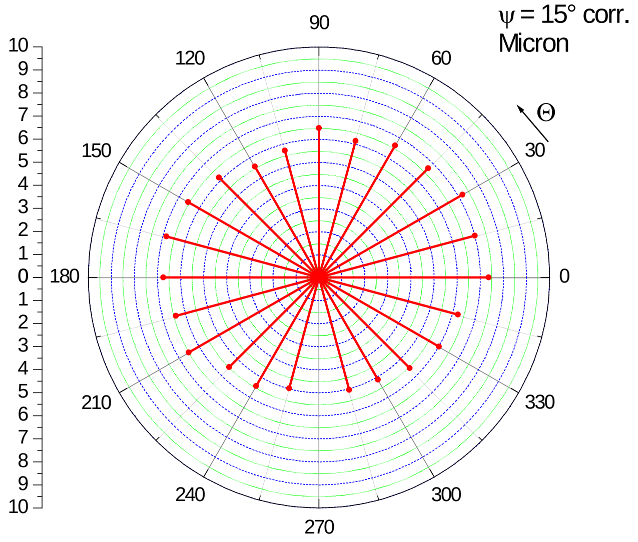


Fig.18: Corrected SEU Cross Section σ(θ) [1E-2 cm^2] at ψ = 15° of the Micron 8-Gbit NAND-Flash

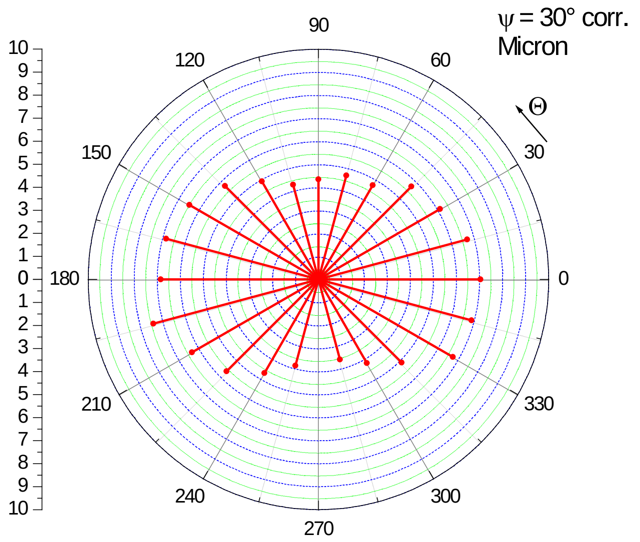


Fig.19: Corrected SEU Cross Section σ(θ) [1E-2 cm^2] at ψ = 30° of the Micron 8-Gbit NAND-Flash

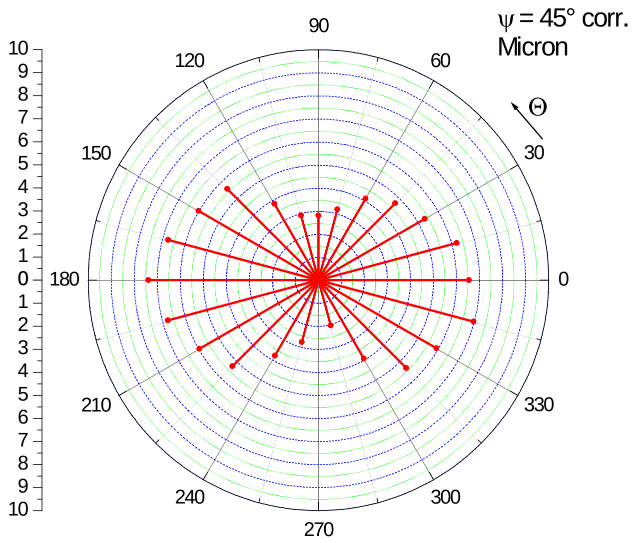


Fig.20: Corrected SEU Cross Section σ(θ) [1E-2 cm^2] at ψ = 45° of the Micron 8-Gbit NAND-Flash

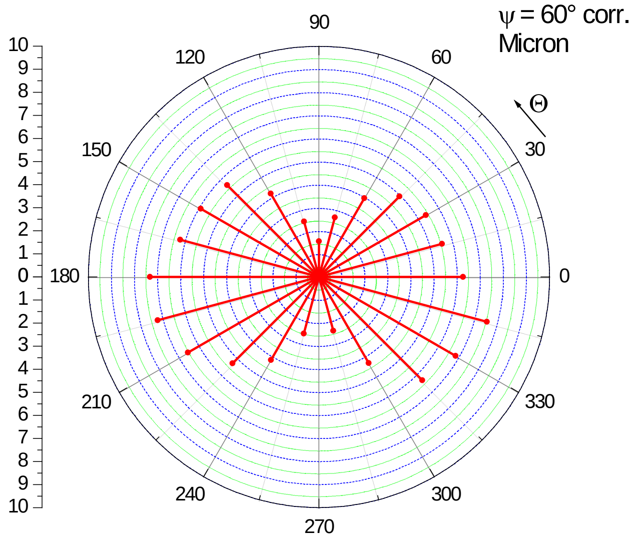


Fig.21: Corrected SEU Cross Section σ(θ) [1E-2 cm^2] at ψ = 60° of the Micron 8-Gbit NAND-Flash

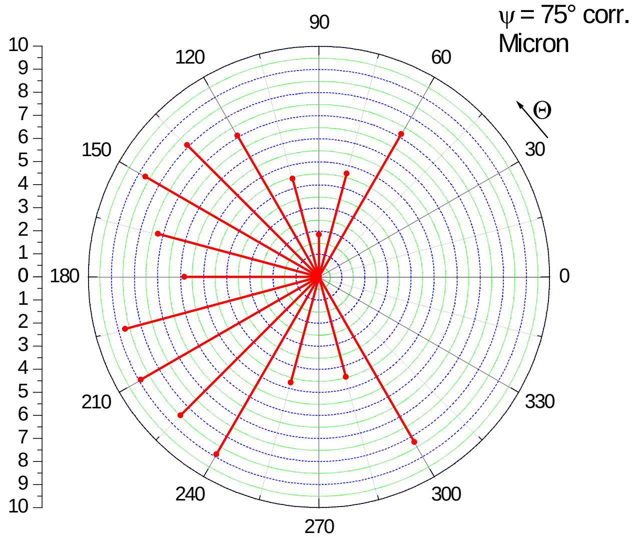


Fig.22: Corrected SEU Cross Section σ(θ) [1E-2 cm^2] at ψ = 75° of the Samsung 8-Gbit NAND-Flash

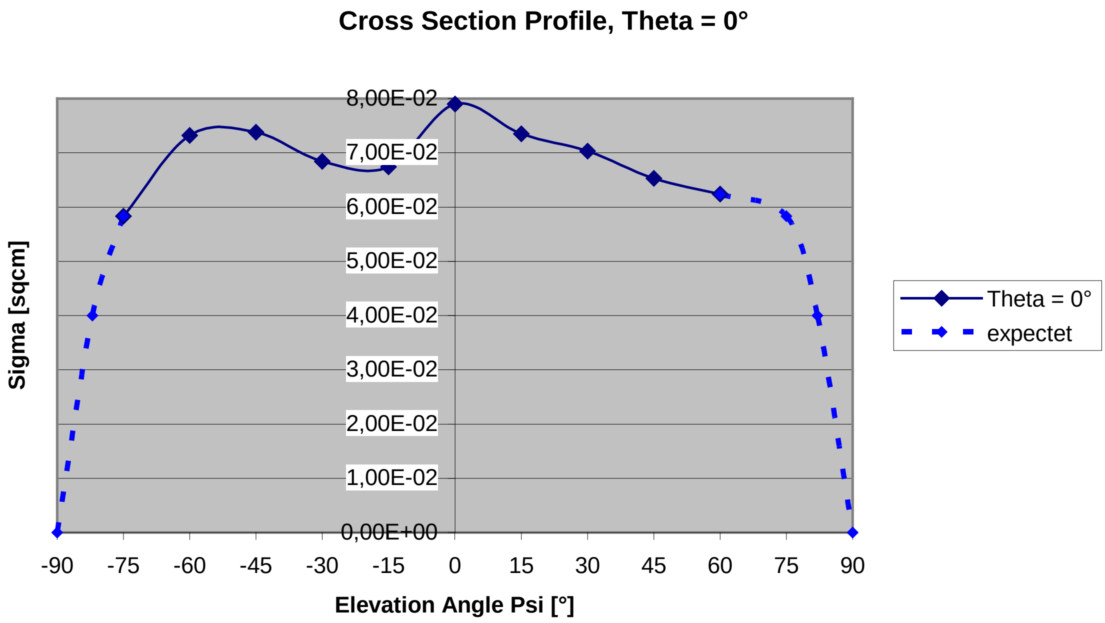


Fig. 23: Cross Section profile σ(ψ), θ = 0°, Micron 8-Gbit NAND-Flash
Notice: ψ = - 45°, θ = 0° is equivalent to ψ = + 45°, θ = 180°

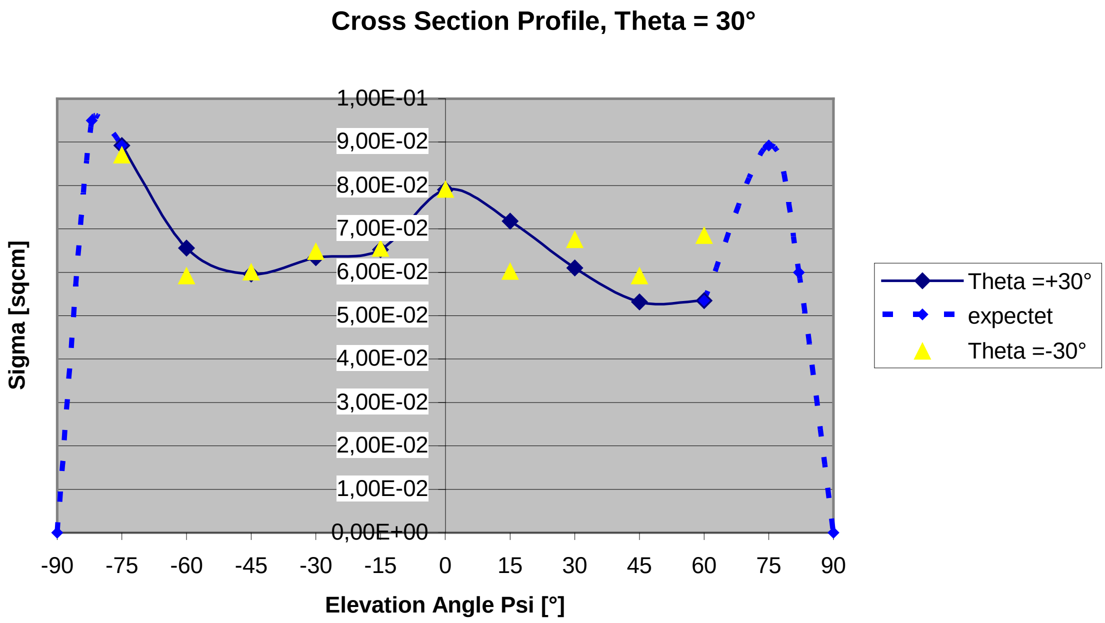


Fig. 24: Cross Section profile σ(ψ), θ = 30°, Micron 8-Gbit NAND-Flash
Notice: ψ = - 45°, θ = +30° is equivalent to ψ = + 45°, θ = 210°,
ψ = - 45°, θ = -30° is equivalent to ψ = + 45°, θ = 150°°

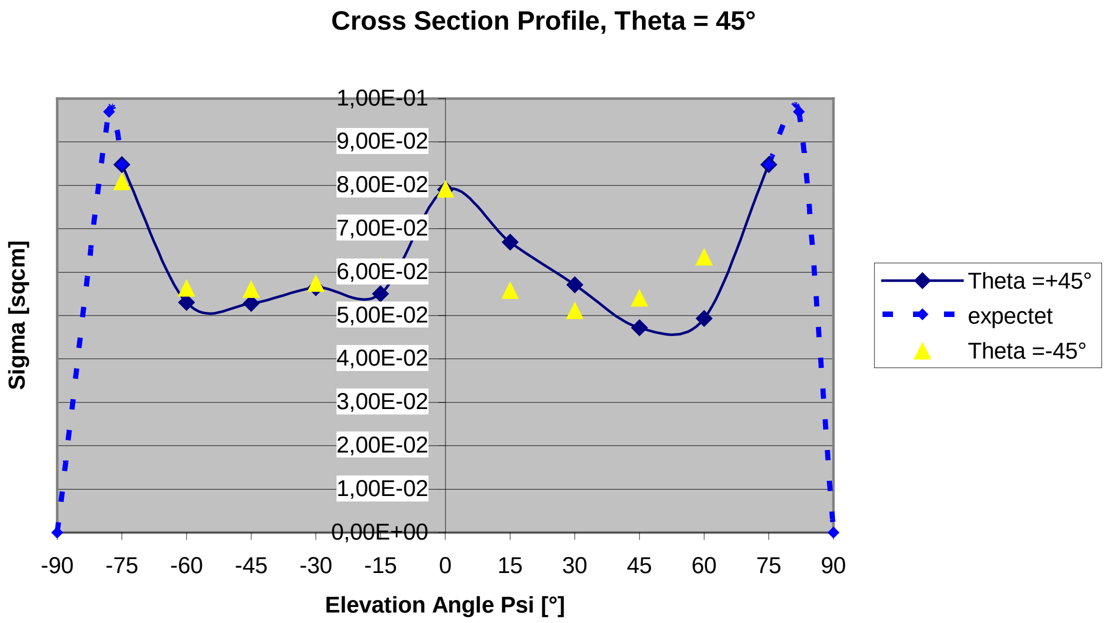


Fig. 25: Cross Section profile σ(ψ), θ = 45°, Micron 8-Gbit NAND-Flash
Notice: ψ = - 45°, θ = 45°° is equivalent to ψ = + 45°, θ = 225°
ψ = - 45°, θ = -45°° is equivalent to ψ = + 45°, θ = 135°

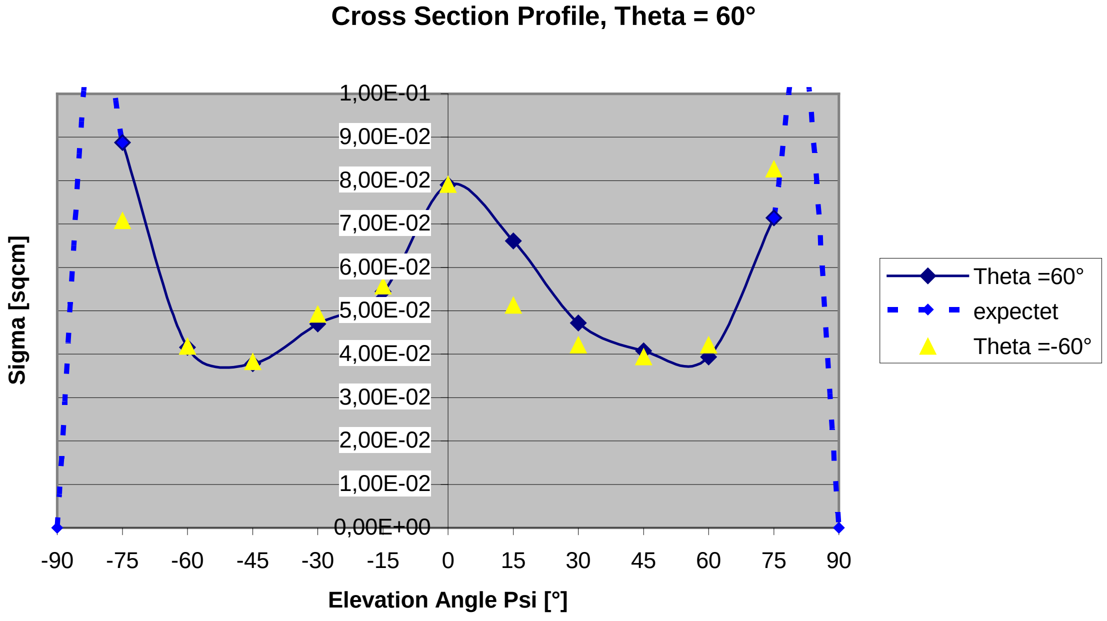


Fig. 26: Cross Section profile σ(ψ), θ = 60°, Micron 8-Gbit NAND-Flash
Notice: ψ = - 45°, θ = 60° is equivalent to ψ = + 45°, θ = 240°
ψ = - 45°, θ = -60° is equivalent to ψ = + 45°, θ = 120°°

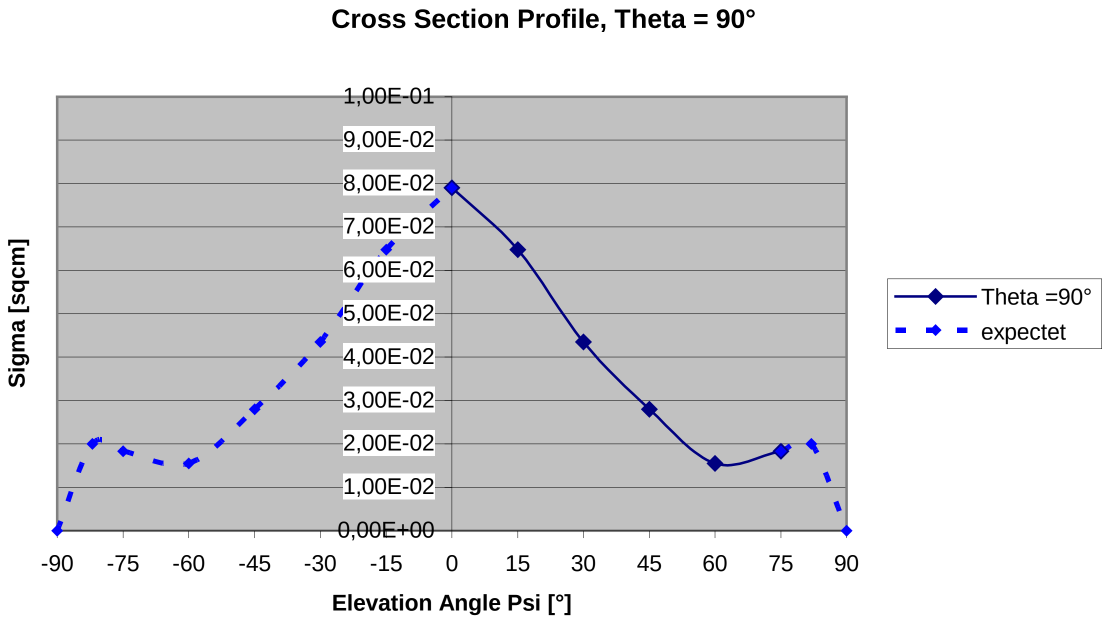


Fig. 27: Cross Section profile σ(ψ), θ = 90°, Micron 8-Gbit NAND-Flash
Notice: ψ = - 45°, θ = 90° is equivalent to ψ = + 45°, θ = 270°

For elevations down to 60° the Micron SEU cross section exceeds that of the Samsung device by roughly one order of magnitude. The principal shape of the Micron cross section profiles is very similar to that of the Samsung device. Its butterfly wings at very slant incidence (ψ > 60°) are substantially smaller compared to the Samsung device.

The Samsung device shows in principal the same tendency of cross section improvement with increasing dose (Fig. 17), but significantly less pronounced than the Micron device. Therefore, we abstained from a correction of the measured cross sections.

Looking on the development of the cross section over the fluence one might suspect that at roughly 20 krad the improvement comes to an end or even might change from improvement to worsening.

This is still an open issue. Generally the effect of the accumulated dose on the SEE behaviour is a widely unexplored field, in particular for DDR and Flash memory devices.

6. Multibit Errors

6.1 Contribution of Multi Bit Errors to the Omni-directional Error Cross Section

The substantial increase of the SEU cross section at very slant ion incidence might originate from Multi Bit Errors (MBUs), i.e. from the falsification of physically neighbouring storage cells. A respective mechanism is described and discussed in [1]. Therefore, we inspected the error maps for MBU occurrence. The outcome of this inspection is (i) that nearly no MBUs occur at normal incidence, as it was expected, and (ii) that even at 75° incidence angle MBUs represent only a minor part of the error population. The majority of errors are randomly distributed over the address space. We found no in-page corruptions of neighbouring column addresses, but some corruptions of neighbouring column addresses of neighbouring page addresses. The spectrum of page address distances showed significant peaks only at address distances ≤ 4. This means that error coupling is limited to short page address distances.

From these results we conclude that the increase of the error cross section at very slant incidence can not be explained by MBUs.

6.2 Samsung MBU Pattern

All errors are single bit errors in 0 → 1 direction, which can be interpreted as loss of FG charge.

The example run with $\Theta = 240°$, $\psi = 75°$ delivered the large cross section of 3.19E-2 cm^2.

Block 1 until block 64 delivered 498 single bit errors.

The first error pair appears in block 2 after 13 non-correlated errors. Page 30, column 3899 delivers ae instead of aa, and page 32, column 3901 also ae instead of aa.

Page 31 is not affected. Because of the column address distance of 2 we call this error type “O(ffset)-2 Error”.

The next error pair appears in block 4, page 21 and 23. In this O-2 error the columns 4035 and 4033 are falsified from 55 to 57. Again the same bit position is corrupted.

In block 5 the pages 29 and 33 are falsified in column 109 and column 105, both from 55 to 57.This error type is called O-4 error.

Tab. 5 displays all 29 MBUs of this example run.

Block	Page	Column	Corrected Byte	Falsified. Byte	Δ Page	Δ Column	Δ Bit	MBU Type				
								O-0	O-1	O-2	O-3	O-4
2	30 32	3899 3901	aa aa	ae ae	+2	+2	+04			X		
4	21 23	4035 4033	55 55	57 57	-2	-2	+02			X		
5	29 33	109 105	55 55	57 57	+4	-4	+02					X
7	30 32	3555 3553	aa aa	ea ea	+2	-2	+40			X		
	39 41	1527 1529	55 55	57 57	+2	+2	+02			X		
8	2 4	2588 2590	55 55	57 57	+2	+2	+02			X		
	10 12	2720 2722	55 55	57 57	+2	+2	+02			X		
9	9 11	369 367	55 55	57 57	+2	-2	+02			X		
12	28 30	2239 2237	aa aa	ab ab	+2	-2	+01			X		
13	22 24	1035 1033	aa aa	ae ae	+2	-2	+04			X		
20	27 31	2693 2689	55 55	75 75	+4	-4	+20					X
24	23 25	2107 2105	55 55	75 75	+2	-2	+20			X		
25	39 41	3296 3294	aa aa	ab ab	+2	-2	+01			X		
26	42 44	2229 2231	aa aa	ae ae	+2	+2	+04			X		
28	21 23	1179 1181	55 55	d5 d5	+2	+2	+80			X		
29	11 13	2366 2364	aa aa	ae ae	+2	+2	+04			X		
32	12 14	2300 2302	55 55	5d 5d	+2	+2	+08			X		
36	17	3606	aa	ae	+2	+2	+04			X		

	19	3608	aa	ae								
	28 32	563 567	aa aa	ae ae	+4	+4	+04					X
	55 57	1504 1502	aa aa	ae ae	+2	-2	+04			X		
38	37 39	2061 2063	55 55	d5 d5	+2	+2	+80			X		
39	34 36	2631 2629	aa aa	ae ae	+2	+2	+04			X		
	42 44	3753 3751	aa aa	ab ab	+2	-2	+01			X		
46	31 33	1283 1281	55 55	57 57	+2	-2	+02			X		
54	35 37	337 335	55 55	d5 d5	+2	-2	+80			X		
55	13 17	2816 2820	aa aa	ab ab	+4	+4	+01					X
59	7 9	1618 1616	aa aa	ea ea	+2	-2	+40			X		
62	33 35	4031 4033	55 55	75 75	+2	+2	+20			X		
63	26 28	727 729	aa aa	ab ab	+2	+2	+01			X		
Σ:										**25**		**4**

Tab. 5: MBUs at Θ = 240°, ψ = 75°, Samsung 8-Gbit NAND-Flash

All 29 MBUs are limited to a pair of falsified bytes in neighbouring pages.

Both affected bytes show the same falsification, always only one identical bit and always from 0 to 1.

The page distance of all MBU pattern is even (2 or 4).

The majority of 25 MBUs are of type O-2 and the remaining 4 MBUs are of type O-4.

The MBUs of type O-2 experience the same distance of two between affected pages and affected columns.

The MBUs of type O-4 also show the same distance of four between affected pages and affected columns.

In consequence, error coupling occurs only between even and even or odd and odd page addresses, and also only between even and even or odd and odd column addresses.

From this we conclude that even addresses and odd addresses point to physically distant array locations.

The test run delivered a total of 498 errors. The 29 MBUs contribute 2 * 29 = 58 errors = 11.6 % of all errors. The majority of the SEUs are randomly distributed over the address space.

In consequence, the steep increase of the SEU cross section at 75° elevation angle can not be attributed to the occurrence of MBUs.

Tab. 6 and Fig. 28 and 29 show the result of an automatic O-0 until O-4 screening of the ψ = 75° and 60° error records. O-0 until O-4 error pattern up to a page distance of four is considered to be generated by a single hit. O-0 until O-4 error pattern of larger page distance is very rare. Those – as well as pattern with a column distance of more than four – are considered to be caused by independent hits.

Elevation Angle ψ	Column Offset					Σ MBUs	Σ SEUs	Percentage of MBU-SEUs
	O-0	O-1	O-2	O-3	O-4			
0°	0	0	0	0	0	0	492	0%
15°	0	1	2	1	1	5	3435	0.29%
30°	0	1	0	2	1	4	2312	0.35%
45°	1	1	1	0	0	3	1683	0.12%
60°	4	1	1	0	1	7	1938	0.36%
75°	12	4	256	4	54	330	7110	9.3%

Tab. 6: MBU total versus elevation angle ψ, θ = 0°, 15° ... 345°
Samsung 8-Gbit NAND-Flash

The 492 errors at normal incidence (ψ = 0) do not contain any MBU.

At ψ = 75° we counted 7110 SEUs. The included 330 MBU situations contribute 2 * 330 = 660 SEUs = 9.3 % of the overall SEU count.

The largest MBU percentage of 32.5 % was detected at ψ = 75°, θ = 75°. It coincides with the largest angular cross section of σ= 5.5E-2 cm^2. This coincidence could indicate that at gracing incidence (ψ > 75°) MBUs might dominate the SEU population.

The very small MBU share at $\psi \leq 45°$ might indicate that these MBU pattern are caused by two independent hits instead of a single hit.

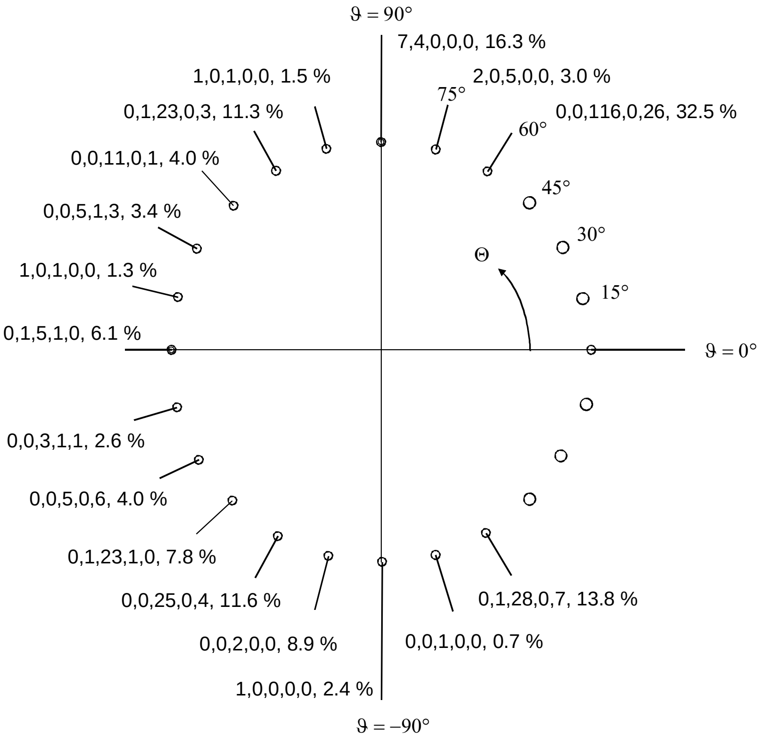


Fig. 28: MBU population at ψ = 75°, Samsung 8-Gbit NAND-Flash
Count of O-0, O1, O2, O3, O4 MBUs, percentage of MBU-SEUs

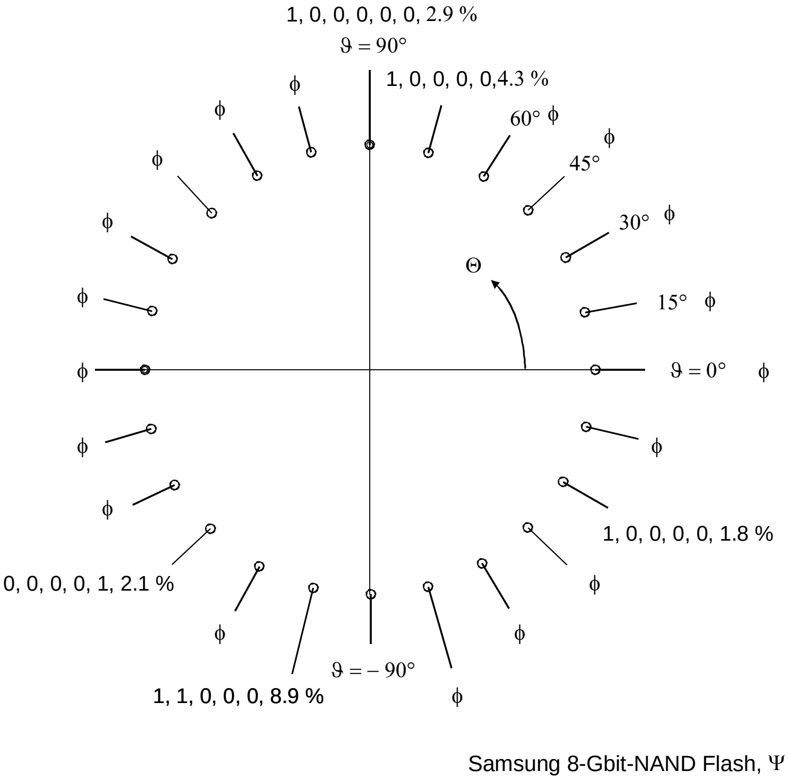


Fig. 29: MBU population at ψ = 60°, Samsung 8-Gbit NAND-Flash
Count of O-0, O1, O2, O3, O4 MBUs, percentage of MBU-SEUs

6.3 Micron MBU Pattern

Tab. 6 shows for the six elevation angels ψ the total count of SEUs and of MBUs, accumulated over all azimuth angles θ, and also the respective percentage of MBU-SEUs.

Each MBU delivers two MBU-SEUs.

Ψ [°]	0	15	30	45	60	75
SEUs	1235	16340	14444	12667	12311	18881
MBUs	6	35	39	49	552	1292
Percentage of MBU-SEUs [%]	1.0	0.42	0.54	0.78	9.0	13.6

Tab. 6: Percentage of MBU-SEUs versus elevation angle

Up to ψ = 45° MBUs deliver only a negligible contribution to the SEU count.

Tab. 7 displays all 51 MBUs of the Θ = 300°°, ψ = 75° error record.

The first MBU appears in block 5. It differs from the Samsung MBUs by two features: (i) the column offset is zero (Type O-0) and (ii) different bits of both affected bytes are falsified.

The MBU in block 10, page 29/31 is also of a new type (O-1) because of the column offset of one.

The second O-0 MBU in block 16 and the O-0 MBU in block 47 are remarkable because they affect not only two pages but three neighbouring pages.

The MBUs of the Samsung device showed only the page distances two and four. In contrast, the MBUs of the Micron device show all page distances between one and four.

Only few Micron error records are MBU free because of the larger SEU count compared to the Samsung device.

Block	Page	Column	Corrected Byte	Falsified. Byte	Δ Page	Δ Column	Δ Bit	MBU Type				
								O-0	O-1	O-2	O-3	O-4
5	5 9	3576 3576	aa aa	Ae ba	4	0	04 10	X				
7	31 35	3843 3843	55 55	75 d5	20 80	4	0	X				
9	12 16	3075 3075	aa aa	Ba ea	4	0	10 40	X				
	60 61	3231 3231	aa 55	Ea d5	1	0	40 80	X				
10	11 15	1402 1402	aa aa	Ea ba	4	0	40 10	X				
	19 20	3385 3383	55 aa	D5 ae	1	-2	80 04			X		
	29 31	294 295	aa 55	Ab d5	2	1	01 80		X			
	51 52	1368 1369	aa aa	Ea ab	1	1	40 01		X			
11	4 6	3063 3062	aa 55	Ab d5	2	-1	01 80		X			
13	27 28	1811 1811	55 aa	75 ba	1	0	20 10	X				
14	31 33	2360 2361	aa 55	Ab d5	2	1	01 80		X			
15	9 13	3389 3389	55 55	57 5d	4	0	02 08	X				
16	15 19	335 336	55 aa	57 ab	02 01	4	1		X			
	52 55 56	3262 3262 3262	55 aa 55	57 ae 5d	02 04 08	3 4	0 0	X				
19	43 44	2939 2939	55 aa	75 ea	20 40	1	0	X				
21	36 38	0 0	64 66	66 67	02 01	2	0	X				
23	11 15	2863 2863	55 55	75 d5	20 80	4	0	X				

	39 42	3836 3836	aa 55	Ba 5d	10 08	3	0	X				
24	13 14	3745 3745	55 aa	5d ba	08 10	1	0	X				
	58 62	459 459	aa aa	Ba ea	10 40	4	0	X				
25	4 8	324 324	55 55	5d 75	08 20	4	0	X				
	23 25	2856 2857	aa 55	Ab d5	01 80	2	1		X			
26	5 9	165 165	55 55	5d 75	08 20	4	0	X				
	51 55	1256 1256	aa aa	Ae ba	04 10	4	0	X				
27	44 45	1590 1590	55 aa	57 ae	02 04	1	0	X				
29	44 47	1207 1207	aa 55	Ea 75	40 20	3	0	X				
31	29 30	3174 3177	aa aa	Ab ab	01 01	1	3				X	
32	42 45	3841 3841	aa 55	Ea 75	40 20	3	0	X				
33	18 22	845 845	aa aa	Ba ae	10 04	4	0	X				
	21 22	3671 3671	55 aa	D5 ea	80 40	1	0	X				
	38 41	3641 3641	aa 55	Ae 5d	04 08	3	0	X				
38	23 27	1759 1759	55 55	5d 75	08 20	4	0	X				
	57 61	1010 1010	aa aa	Ba ea	10 30	4	0	X				
39	19 23	1063 1064	55 aa	57 ab	02 01	4	1		X			
	34 36	4214 4215	55 aa	57 ab	02 01	2	1		X			
40	27 30	1682 1682	Aa 55	Ea d5	40 80	3	0	X				
41	17	1694	Aa	Ab	01	1	1		X			

	18	1695	aa	ea	40							
44	37 41	554 554	Aa aa	Ab ae	01 04	4	0	X				
	52 56	3198 3201	55 aa	57 ab	02 01	4	3				X	
46	47 49	1558 1559	Aa 55	Ab d5	01 80	2	1		X			
47	1 2 5	3328 3328 3328	Aa 55 aa	Ab 57 ae	01 02 04	1 4	0	X				
49	28 29	4112 4112	55 aa	57 ab	02 01	1	0	X				
51	41 45	2127 2127	55 55	75 5d	20 08	4	0	X				
52	12 13	2999 2999	Aa 55	Ae 5d	04 08	1	0	X				
56	27 31	3246 3249	Aa 55	Ab 57	01 02	4	3				X	
57	42 44	3222 3223	55 aa	D5 ab	80 01	2	1		X			
60	22 24	3171 3170	Aa 55	Ab d5	01 80	2	-1		X			
61	30 31	2936 2936	55 aa	5d ae	08 04	1	0	X				
	60 61	3230 3230	55 aa	75 ea	20 40	1	0	X				
63	34 38	3680 3680	55 55	5d 75	08 20	4	0	X				
64	2 6	3465 3465	Aa aa	Ae ab	04 01	4	0	X				
Σ:								**35**	**12**	**1**	**3**	**0**

Tab. 7: MBUs at Θ = 300°, ψ = 75°, Micron 8-Gbit NAND-Flash

Fig. 30 and 31 show the result of the automatic MBU screening of the ψ = 75° and 60° error records.

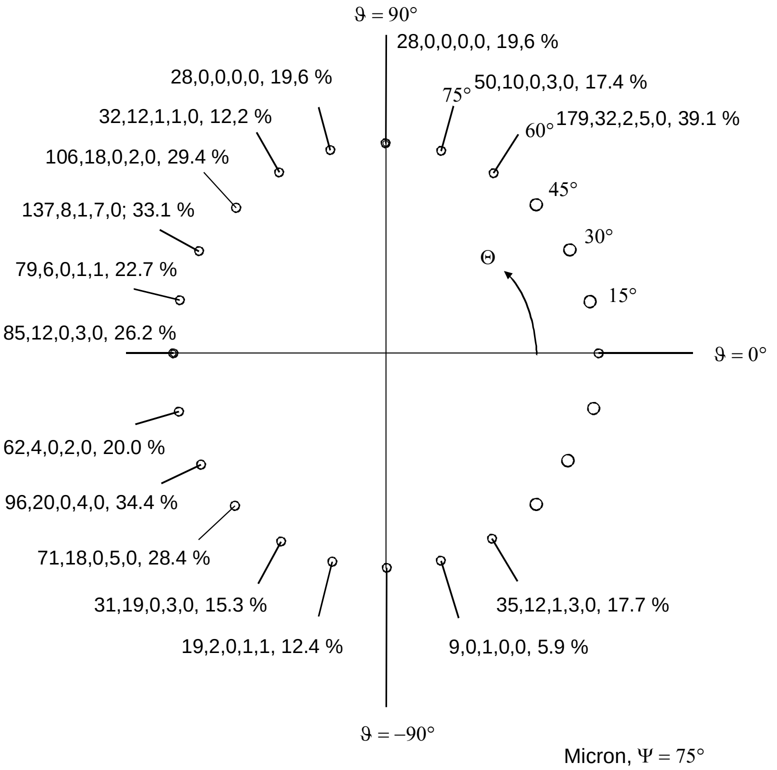


Fig. 30: MBU population at ψ = 75°, Micron 8-Gbit NAND-Flash
Count of O-0, O1, O2, O3, O4 MBUs, percentage of MBU-SEUs

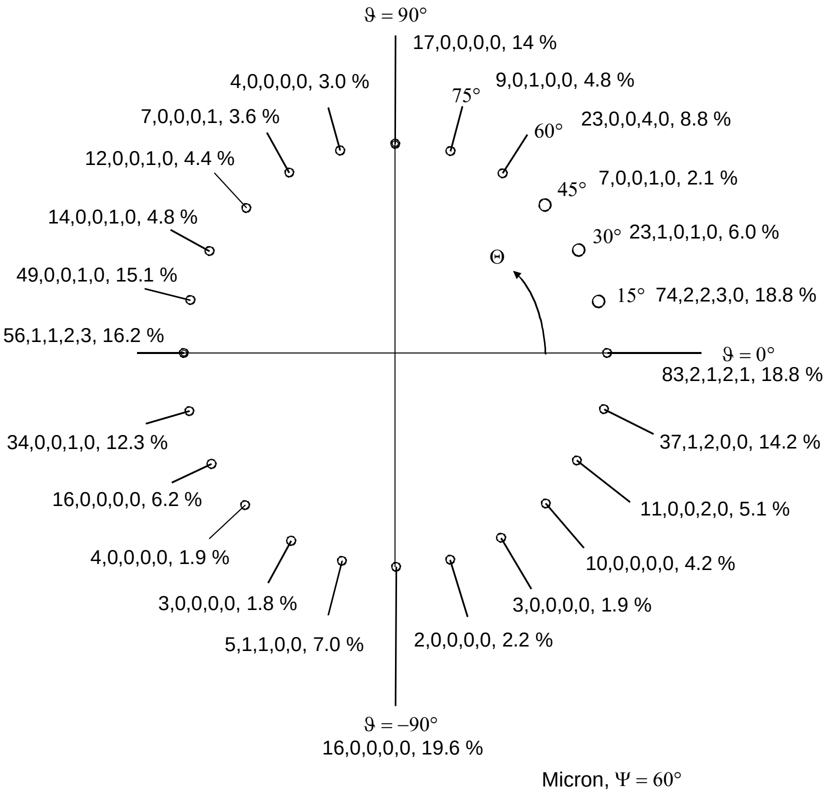


Fig. 31: MBU population at ψ = 60°, Micron 8-Gbit NAND-Flash
Count of O-0, O1, O2, O3, O4 MBUs, percentage of MBU-SEUs

Fig. 32 shows the MBU-SEU percentage versus the elevation angle ψ
for the horizontal azimuth direction θ = 0, the diagonal directions θ = ± 45° and the vertical direction θ = 90°.

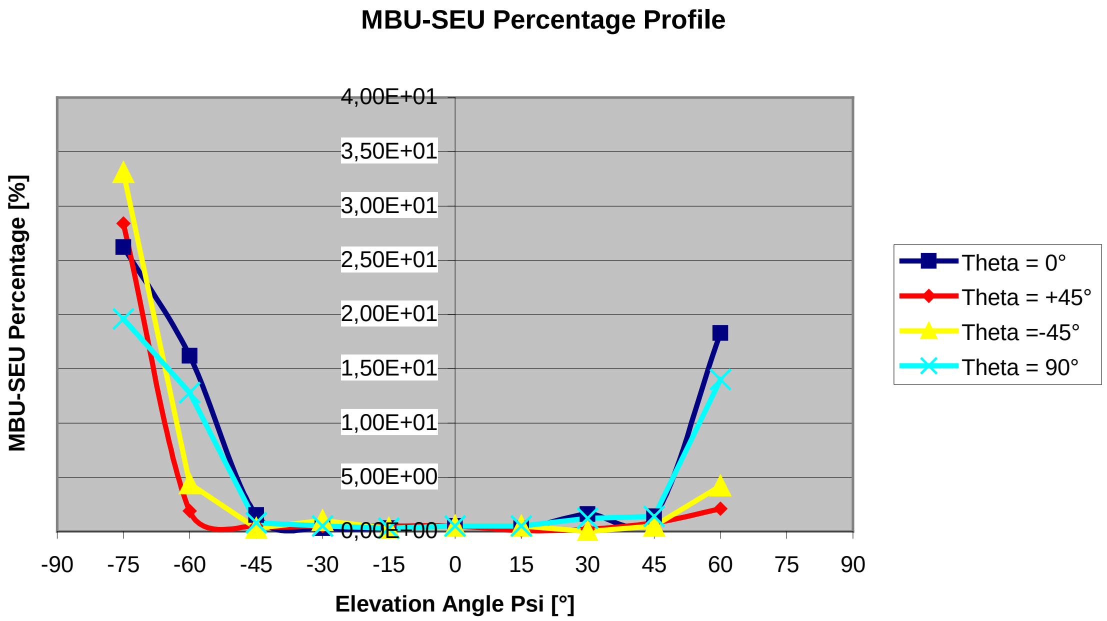


Fig. 32: MBU-SEU percentage versus elevation angle ψ.

6.4. Discussion

(A) Common Features of the Samsung and the Micron Device

(i) Tilting increases the percentage of MBUs such as expected. Up to elevation angels ψ ≤ 45° the share of MBU-SEUs remains below 2%. At least a fraction of these MBUs are pseudo-MBUs, i.e. MBUs produced by two independent hits.

(ii) At ψ ≥ 60° the percentage of MBU-SEUs increases steeply.
The increase at ψ ≥ 75° could not be measured during this campaign because of an imperfection of the tilting set up. The lacking test data should be gained during the next test campaign by means of our new upgraded tilting set up.

(iii) Even at ψ = 75° the MBUs represent only a minority of the SEUs, at least at LET = 10 MeV cm2 mg-1.

(iv) The dependence of the cross section on the angle of incidence and also of the contribution of MBUs still has to be investigated for higher LET ions (Kr, Xe).

(v) All MBUs showed only 1 → 0 falsifications.

(vi) MBUs corrupting several bits of the same byte did not occur. This indicates that in the array the bit planes are physically separated.

(vii) MBUs corrupting several bytes (columns) of the same page did not occur.

(viii) Only very few MBUs corrupted bits over a distance of more than 4 pages.

(ix) Only very few MBUs corrupted bits over a distance of more than 4 columns

(x) The angular distributions of the MBU-SEU percentage peak at ± 30° right and left from the vertical axes ($\theta = 60°$, 120°, 240° and 300°).

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(B) Differing Features of the Samsung and the Micron Device

(i) The Samsung device showed only MBUs of a page distance of 2 or 4, and with few exceptions, with a column distance of 0, 2 or 4. This indicates that even and odd pages are separated in the array, and also even and odd columns.
In contrast the Micron device delivered both, even and odd distances.

(ii) The Samsung MBU population is dominated by MBUs with a column distance of 2 or 4. Only vertical incidence ($\theta = 90°$, 270°) produces MBUs with zero column distance.
In contrast the Micron MBU population is dominated by MBUs with zero column distance.

(iii) Overall the Samsung device shows a smaller percentage of MBU-SEUs. But the peak percentage of both devices is quite similar (Samsung: 32.5%, Micron 39.1 %, both at $\theta =$ 60°).

7. SEU Cross Section for Omni-directional Flux

7.1 Approximate Calculation

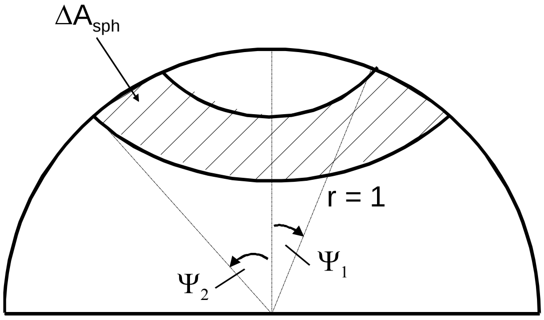
The integration of the uni-directional cross section $\sigma(\Theta,\psi)$ over the half unity sphere delivers the cross section for omni-directional exposure

$$\Delta\sigma_{sph} = \frac{1}{2\pi}\int_{0}^{2\pi}\int_{0}^{\pi/2} \sigma(\theta,\psi)\, d\theta\, d\psi \qquad (7.1)$$

To approximate the value of this integral we divide the surface of the half sphere into latitude bands (Fig.33). The width of these latitude bands is $\Delta\psi = 15°$, for the polar cap and for the equatorial band $\Delta\psi = 7.5°$.

We regard the cross section for normal incidence $\sigma(\Theta = 0, \psi = 0)$ to be representative for the whole polar cap,
the average $\sigma_{av,\psi=15°}$ over the cross sections $\sigma(\Theta = 0° - 360°, \psi = 15°)$ to be representative for the whole latitude band between $\psi_l = 7.5° \leq \psi < \psi_u = 22.5°$,
the average $\sigma_{av,\psi} = \sigma_{av,30}$ over the cross sections $\sigma(\Theta = 0° - 360°, \psi = 30°)$ to be representative for the whole latitude band between $\psi_l = 22.5° \leq \psi < \psi_u = 37.5.5°$,

...



$$\Delta A_{sph} = 2\pi r^2 \cdot \left(\cos\Psi_1 - \cos\Psi_2\right)$$

Fig. 33: Latitude Band on the Surface of the Unity Sphere

The surface area of the latitude band between ψ_l and ψ_u amounts to $2\pi * (\cos\psi_l - \cos\psi_u)$. It contributes

$$\Delta\sigma_{sph} = \frac{1}{2\pi} * \sigma_{av,\psi} * 2\pi * (\cos\psi_l - \cos\psi_u)$$

$$= \sigma_{av,\psi} * (\cos\psi_l - \cos\psi_u) \qquad (7.2)$$

to the omni-directional cross section $\sigma_{av,\psi}$.

Tab. 8 shows for the Samsung device (i) the average SEU cross section over one azimuth quadrant at a given elevation angle ψ and (ii) the average $\sigma_{av,\psi}$ over all four quadrants.

Azimuth Quadrant	Elevation Angle ψ					
	0°	15°	30°	45°	60°	75°
0° ≤ Θ < 90°	7.86	5.94	6.32	4.72	6.04	31.2
90° ≤ Θ < 180°		4.30	4.42	3.27	3.94	22.0
180° ≤ Θ < 270°		5.78	5.57	4.40	4.83	26.3
270° ≤ Θ < 360°		5.05	4.46	3.48	4.44	24.2
$\sigma_{av,\psi}$	7.86	5.27	5.19	3.97	4.81	25.9

Tab. 8: Average Cross Section in **1E-3 cm^2** versus Elevation Angle ψ,
Samsung 8-Gbit NAND-Flash

Tab. 9 shows the same for the Micron device.

Azimuth Quadrant	Elevation Angle ψ					
	0°	15°	30°	45°	60°	75°
$0° \leq \Theta < 90°$	7.90	6.74	5.73	5.01	4.78	7.39
$90° \leq \Theta < 180°$		6.18	5.44	4.65	4.11	6.25
$180° \leq \Theta < 270°$		6.05	5.92	5.43	5.63	7.75
$270° \leq \Theta < 360°$		5.75	5.21	4.67	4.95	6.89
$\sigma_{av,\psi}$	7.90	6.18	5.58	4.94	4.87	7.07

Tab. 9: Average Cross Section in **1E-2 cm^2** versus Elevation Angle ψ,
Micron 8-Gbit NAND-Flash

Tab. 10 displays the numerical calculation of σ_{sph} for the Samsung device, and Tab. 11 for the Micron device.

For the not yet measured unidirectional cross section $\sigma_{av,\psi}$ at ψ >75° three crude assumptions are made, one of them over-optimistic, one possibly realistic and one pessimistic.

Ψ	ψ_l	ψ_u	$\sigma_{av,\psi}$	$\cos \psi_l - \cos \psi_u$	$\Delta\ \sigma_{sph}$	σ_{sph}
0°	0°	7.5°	7.86E-3	8.555E-3	6.724E-5	
15°	7.5°	22.5°	5.27E-3	6.757E-2	3.561E-4	
30°	22.5°	37.5°	5.19E-3	1.305E-1	6.774E-4	
45°	37.5°	52.5°	3.97E-3	1.846E-1	7.328E-4	
60°	52.5°	67.5°	4.81E-3	2.261E-1	1.087E-3	
75°	67.5°	82.5°	2.59E-2	2.522E-1	6,531E-3	9.152E-3
86°	82.5°	90°	0 3.0E-2 6.0E-2	1.305E-1	0 3.916E-3 7.832E-3	9.152E-3 1.337E-2 1.698 E-2

Tab. 10: Numerical Calculation of the Omni-directional SEU Cross Section σ_{sph},
Samsung 8-Gbit NAND-Flash, σ = 7.86 **E-3** cm^2 at normal incidence

Ψ	ψ_l	ψ_u	$\sigma_{av,\psi}$	$\cos\psi_l - \cos\psi_u$	$\Delta\ \sigma_{sph}$	σ_{sph}
0°	0°	7.5°	7.90E-2	8.555E-3	6.759E-4	
15°	7.5°	22.5°	6.18E-2	6.757E-2	4.176E-3	
30°	22.5°	37.5°	5.58E-2	1.305E-1	7.283E-3	
45°	37.5°	52.5°	4.94E-2	1.846E-1	9.119E-3	
60°	52.5°	67.5°	4.87E-2	2.261E-1	1.101E-2	
75°	67.5°	82.5°	7.07E-2	2.522E-1	1.783E-2	5.009E-2
86°	82.5°	90°	0 1.0E-1 2.0E-1	1.305E-1	0 1.305E-2 2.610E-2	5.009E-2 6.314E-2 7.619E-2

Tab. 11: Numerical Calculation of the Omni-directional SEU Cross Section σ_{sph},
Micron 8-Gbit NAND-Flash, $\sigma = 7.90$ **E-2** cm^2 at normal incidence

7.2 Discussion

Ions with very slant incidence ($\psi \geq 60°$) contribute more than 50% to the omni-directional SEU cross section. This illustrates the necessity for cross section measurments at large tilting angles.

The Samsung device experiences a steep increase of the cross section at very slant ion incidence. In consequence, its omni-directional cross section exceeds its cross section for normal incidence, in case of our over-optimistic assumption by 16 % and in case of our pessimistic assumption by more than 100 %.

But despite of its steep sensitivity increase at very slant incidence the omni-directional cross section of the Samsung device remains below that of the Micron device.

8. Open Issues

(1) SEU Cross Section at very slant incidence ($\psi \geq 75°$, Samsung and Micron 8_Gbit NAND-Flash, Ar, LET = 10)

(2) SEU Cross Section dependence on accumulated Dose at normal incidence
  (a) Irradiation of DUTs until given dose values for subsequent Heavy Ion SEE test
  (b) Heavy Ion test (Ar) up to higher dose values (> 20 krad)

(3) SEU Cross Section dependence on incidence direction at Kr and Xe
(Larger percentage of MBUs ?)

(4) Update of the SEU Annealing Characterization for ≥8-G NAND-Flashs

The measurements (1) and (3) at gracing incidence possibly suffer from the non-sufficient vertical penetration of the available test ions compared to ions in space. Ions of range s achieve a vertical penetration of d = s * cos ψ (Fig. 34, Tab. 13).

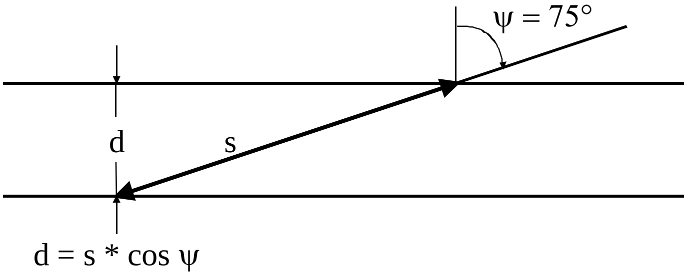


Fig. 34: Vertical penetration at slant incidence

Ψ [°]	d [µm]					
	$^{15}N^{4+}$	$^{20}Ne^{6+}$	$^{30}Si^{8+}$	$^{40}Ar^{12+}$	$^{56}Fe^{15+}$	$^{82}Kr^{22}$
0	202	146	130	118	97	94
15	195	141	126	114	94	91
30	175	126	113	102	84	81
45	143	103	92	83	69	66
60	101	73	65	59	49	47
75	52	38	34	31	25	24
80	35	25	23	20	17	16
85	18	13	11	10	8	8

Tab. 13: Vertical ion penetration at slant incidence,
RADEF 9.3 MeV/amu Ion Coctail

Due to the possibly non-sufficient vertical penetration the measured cross section values are minimum values and therefore, best case values.

9. Summary

We investigated the angular dependence of the SEU cross section for Samsung and Micron 8-Gbit NAND-Flash memories. The DUTs were tilted in the azimuth plane by 360° in steps of 15°, and in the elevation plane from 0° to 75° in steps of 15°.

The polar diagram of the SEU cross section is shaped like an antenna diagram with its main axes coinciding with the long die axes. Tilting from normal incidence (0° elevation) to slant incidence produces at first a moderate decrease of the cross section and thereafter, starting between 45° and 60°, a steep increase of the cross section for most of the azimuth angles, with the exception of the azimuth angels close to the short die axes.

We observed a decrease of the SEU cross sections with the applied fluence, which imposed a dose of up to 20 krad. This effect is very apparent for the Micron device, but also observable for the Samsung device. Surprisingly it seems that a dose increase up to 20krad improves the SEU sensitivity. We believe that this unexpected effect needs a more thorough investigation.

Further we studied the angular dependence of the share of MBUs within the SEU population. Up to about 60° inclination the contribution of MBUs to the overall SEU population is below 2 %. But for very slant incidence the share of MBU-SEUs increases substantially, at 75° inclination and specific azimuth angles up to 30 – 40 %. But, randomly distributed SEUs still dominate the error population.

In space the particle flux is omni-directional, and therefore the relation between the cross section for normal incidence and the cross section for omni-directional incidence is of interest. We calculated the omni-directional cross section under some assumptions for the still unknown angular cross section at elevation angles between 75° and 90° (gracing incidence).

Depending on the taken assumptions the omni-directional SEU cross section of the Samsung device exceeds the cross section for normal incidence by a factor between 1.2 and 2.0.

In contrast the omni-directional SEU cross section of the Micron device remains below its cross section for normal incidence for all our assumptions. But because of its significantly higher SEU cross section at normal incidence its omni-directional cross section can not match that of the Samsung device.

The main results have been and will be published at several opportunities [3, 4, 5].

10. References

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