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Heavy Ion SEE Test
of
2 -Gbit DDR2 SDRAM Devices

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Contents

1. General Scope

Future space borne mass memories are expected to be based on two different memory technologies: (i) DDR2/3 SDRAMs preferably for the high data rate / moderate capacity memory domain and (ii) NAND-Flashs preferably for the moderate data rate / high capacity memory domain.

In consequence SEE and TID radiation test campaigns of DDR2/3 memory devices have to be performed in addition to the already running NAND-Flash radiation test efforts.

In preparation of DDR2 tests an advanced memory testbed (RTMC4) has been developed and upgraded to 125 MHz DLL ON operation.

2. Goal of the DDR SDRAM SEE Tests

The tests focused on the SEFI behaviour of Micron and Elpida DDR2 SDRAMs and the efficiency of countermeasures.
Randomly distributed Single Errors are of minor concern. These errors can be easily coped even by Hamming error correction.
But, clustered errors are prone to exhaust the capability of the error correction. In consequence, the characterization of the various types of clustered errors and the evaluation of respective cross section curves are of major importance.

Clustered errors can be differentiated into two main categories:

a) Those, which directly are caused by a single hit of adjacent structures of the cell array, and
b) SEFIs, which originate from particle induced malfunctions of the control circuitry.

A related aspect is the study of countermeasures against SEFIs. Re-initialization of the device is known to be an effective countermeasure. But, it slows down the effective access rate. Which re-initialization rate should be applied? How much resistant SEFIs withstand the re-initialization?

Another related aspect is whether SEFI induced cluster errors will be induced during non-access periods. Refresh is still running and the generation of cluster errors due to particle induced disturbances of the refresh circuitry is imaginable.

Relevant questions are (i) whether those SEFIs occur, and in case (ii) whether they are only transient or even all / some of them persistent, and again in case (iii) whether re-initialization during non-access periods should be recommended.

Another point, often highlighted in the literature, is hard errors / weak cells. From published papers we see that these hard errors are a specific very rare type of distributed single errors, which can be wiped out easily by the usual error correction, together with the more frequent soft single errors.

Therefore, we plan to inspect our test data sets for hard errors, but this will not be an high priority task. In particular, at this time we don't plan to investigate the influence of the refresh period on the occurrence frequency of hard errors.

To summarize, at this time our main goals are partly related to the collection of test data, namely

a) Collection of test data sets in three test modes (M3 "Static" Storage, M1 Dynamic Read and M2 Write Read) at room temperature.
b) Studying the effect of re-initialization (Two initialization modes, several re-initialization periods)

and partly related to the improvements of the test bed S/W, namely

c) to improve the automatic detection, classification and extraction of the different cluster error / SEFI types in order to gain reliable SEFI type specific cross section curves,
d) to implement a zoom function to improve the resolution of the screen image
e) to extend the address range of the test bed to cover the full address range of up to 8 Gbit devices.

This report describes execution and results of two Heavy Ion test, which were performed at the RADEF facility of the University of Jyväskylä, Finland.
Both tests were aimed to gain SEU and SEFI cross sections of the Elpida and the Micron 2-Gbit DDR2 SDRAM device in DLL ON mode for normal ion incidence and room temperature.

3. Irradiation Facility

The RADEF facility is described in [1]. The ion cocktail used is given in Tab. 2.1. We irradiated with all of these ions with the exception of Si

Fig. 1 shows the LET versus range plots.

Ion	Energy [MeV]	Effective LET [MeV cm^2 mg^{-1}, SiO^2]	Range [µm]
$^{15}N^{4+}$	139	1.8	202
$^{20}Ne^{6+}$	186	3.6	146
$^{30}Si^{8+}$	278	6.4	130
$^{40}Ar^{12+}$	372	10.1	118
$^{56}Fe^{15+}$	523	18.5	97
$^{82}Kr^{22+}$	768	32.1	94
$^{131}Xe^{35+}$	1217	60	89

Tab. 3.1: RADEF 9.3 MeV/amu Ion Cocktail, DUT in vacuum

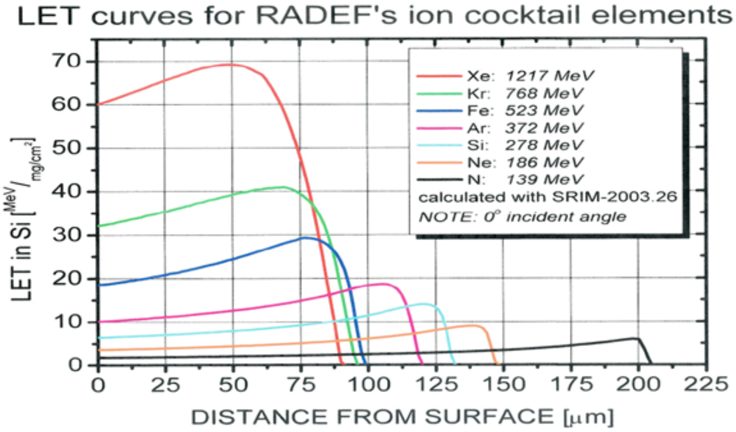


Fig.3.1: RADEF 9.3 MeV/amu Ion Cocktail, LET versus range

Irradiation in air delivers a slightly increased LET value at the DUT surface in expense of slight range reduction (Tab. 3.2)..

Ion	Energy in Vacuum [MeV]	LET @ DUT in Vacuum [MeV sqcm/mg]	Range in Vacuum [µm]	Air gap [mm]	Energy @ DUT in air [MeV]	LET @ DUTin air [MeV sqcm/mg]	Range @DUT in air [µm]
Ne	186	3.6	145.8	20	158.4	4	115.2
Ar	372	10.2	117.4	20	295.3	11.4	87.7
Fe	523	18.5	98	7	416	20.5	75.4
Kr	768	32.1	95.3	7	584.1	35.3	70.4
Xe	1217	60	89.5				

Tab. 3.1: LET and range for DUT in vacuum and DUT in air

4. DUT Preparation

During the two test campaigns the following Micron and Elpida devices were tested:

Manufacturer:	Micron	Elpida
Part Number:	MT47H256M8HG-37E	EDE2108ABSE-8G-E
Date Code:	0742	0811
Parts (Nov., 02 – 05, 2009):	Mic1a, Mic1d, Mic1f	Mic1k
Parts (March, 29 – Apr. 01 2010):	-	Elp1t
Density:	2 Gbit	2 Gbit
Depth x Width:	256Mb x 8	256Mb x 8
CAS Latency:	4	3
Package, Pin Count:	FBGA, 60-ball	FBGA, 68-ball
max. Clock:	267 MHz	667 MHz
max. Data Rate:	DDR2-533	DDR2-800
op. Temperature:	0°C – 85°C	0°C – 95°C
Die Size:	11.5 mm x 14 mm	10 mm x 19 mm
Original Die Thickness:	250 µm	350 µm

Tab. 2: Tested DDR2 devices

The dies of these DDR2 memory devices are housed in plastic encapsulated ball grid packages (60-ball FBGA) to accommodate the high data byte rate of up to more than 500MHz/s. Fig. 4.1 shows the conceptual package diagram

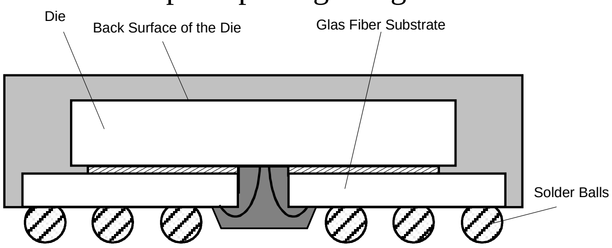


Fig. 4.1: Conceptual Diagram of the FPGA Package

The die is situated upside down. Bonding wires connect pads along the longitudinal die axis with their counterparts on a glass fiber substrate, which distributes the signals to the solder ball grid underneath the base plane of the package. The uncomfortable consequence is that removal of the cover plastic gives access only to the back surface of the die and not to its sensitive top surface. The penetration of the ion beams available at the Heavy Ion Facility (HIF) at Universite Catholique de Louvain (UCL), Belgium and at the Radiation Effects Facility (RADEF) at University of Jyväskylä (JYFL), Finland), is e.g. only 90 µm at LET ≈ 30 MeV cm^2 mg^{-1} (Fig.1), which is substantially below the die thickness of about 200 µm. In consequence ions irradiated from the backside can not reach the sensitive structures below the top surface of the die. To make this possible, the die has to be thinned down to 60 – 70 µm.

Both, unsuccessful and successful thinning efforts have been reported [2, 3]. After some unsuccessful attempts we exercised thinning from an initial die thickness of Micron 250 µm / Elpida 350 µm down to 70 µm without any impairment of the functionality. The opened device was fixed to a metallic support structure by few small adhesive pads (Fig. 4.2).

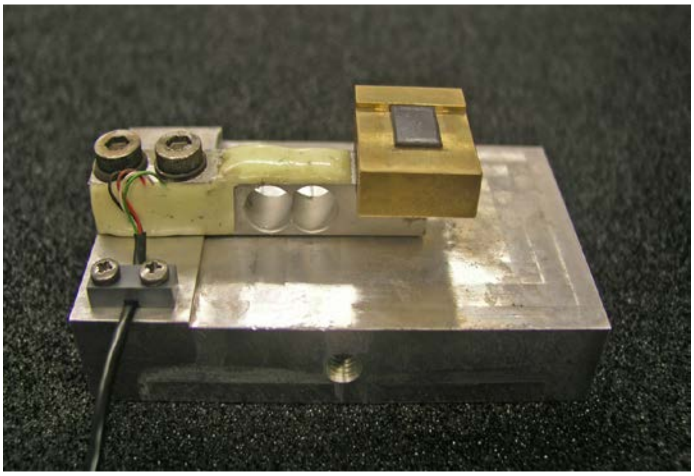


Fig. 4.2: Mechanical DUT Support Structure

The force applied by the grinding tools was monitored by a strain gage on top of the support lever. Grinding wheels were used such as applied for the separation of wafers: (i) diameter 52 mm, (ii) thickness 500 µm and (iii) a tip profile of 120° in order to reduce the contact volume and thereby, the grinding forces. The synthetic diamond grains with a medium grain diameter of 5 µm were supported by a bronze bond. Using the following grinding parameters the die could be machined from an initial thickness of 205µm to a final thickness of 70µm, (i) in-feed speed 100 mm/min, (ii) cutting speed 60 m/s, (iii) grinding width 20 µm. The grinding depth per path was varied in 6 steps: 25 µm for the first four steps, and for the final two passes 20 µm and 15µm, respectively. In the clamping the die showed a curvature of 5 µm in lateral extension and of 10µm in longitudinal extension. Therefore, the path of the grinding wheel had to be adapted to this curvature. By grinding in lateral direction the larger one of the two shape deviations could be reduced definitely. For the chosen setting parameters the grinding time took 8 hours per device.

After several machine-time consuming test runs a success rate of about 50% was achieved.

5. DDR2 Test Bed

The DDR2 Test Bed is structured into three subunits (Fig. 4): (i) DUT Test Adapter (DTA), (ii) Fast Test Unit (FTU) and (iii) Remote Control Unit (RCU).

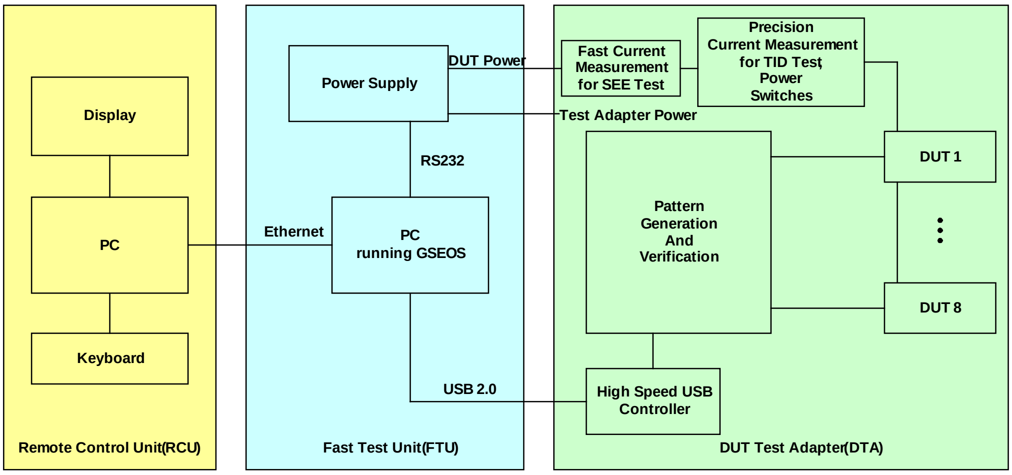


Fig: 5.1:.Overall Structure of the DDR2 Test Bed

Fig. 5.2 displays the DTA board. It is structured into two sections. In the lower section up to eight DUTs can be placed. In this case we see four thinned Micron 1-Gbit DDR2 devices. During Co-60 or Proton exposure the upper section will be shielded. This section contains all the circuitry, which needs to be situated close to the DUTs, mainly for speed reasons. The shown RCU board supports two DUT clock rates: 25 MHz for operation with DLL OFF and 125 MHz for operation with DLL ON.

The core functions of the DTA are implemented in a Xilinx Virtex-4 FPGA. The FPGA contains memory controller, pattern generation and verification and Latch-Up control. The maximum static address width is 28 bit and the maximum dynamic address width is 24 bit row + 24 bit column. The maximum data width is 16 bit.

For historical reasons the GSEOS S/W handles only an 128k address range, which allows to test the full address range of 1Gbit = 128k x 8 bit devices. In order to test the full address range of 2-Gbit= 256k x 8 bit SDRAM a H/W based control of the highest address bit has bin added for manual switch-over between the lower and the upper half of the 256k address space.

Several address patterns are selectable such as Read Background, Write Background and Marching, and also several data pattern such as Constant (128 bit word), Counting (Up and Down) and Pseudo-Random (128 bit seed). Each data pattern is selectable to be inverted.

For each error an error vector (128 bit) is produced in real time and is stored in an error buffer FIFO with a capacity of 128 k error vectors, for later transfer to the RCU hard disk.

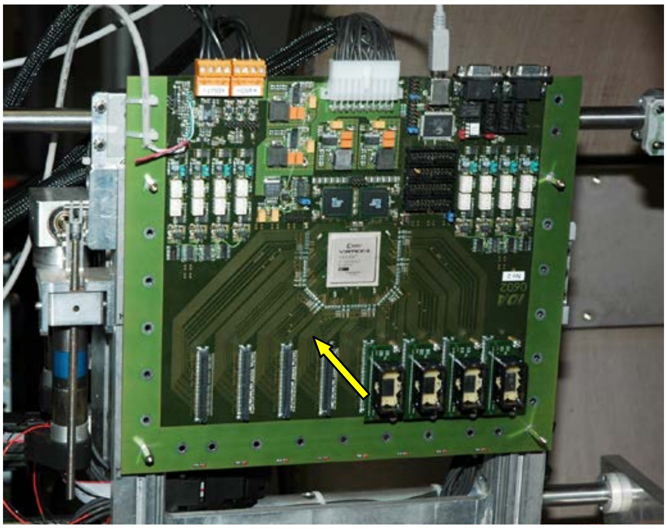


Fig. 5.2: DTA populated with four DUTs

During SEE test the DUT current is continuously monitored by a high speed low (4 mA) resolution ADC, and during TID tests by a low speed high resolution (switchable between 10 pA and 100 µA) ADC. The DUT supply voltage is adaptable between 1.5 and 5.0 V, and the I/O voltage between 1.5 and 3.3 V.

Fig. 5.3: RCU situated in the Control Room

Fig. 5.3 shows the RCU. Its display provides real time monitoring of all test parameter settings, error counts, error statistics as error distribution over the bit planes, percentage of zero to one and one to zero falsifications and in particular a map of the error distribution over the address space in real time.

5. SDRAM Test Modes

- Storage Mode (M3)
  Before irradiation a pattern (all ones, all zeros, checkerboard, random) is written into the DUT and verified. Default is the random pattern. Then the device is irradiated biased (M3a) or unbiased (M3b). Default is a random pattern. After exposure the content of the device is read and verified. Only Static data errors are delivered by this mode.
  In contrast to Flash DUTs not all ‘Static DRAM errors are caused by a direct cell hits. Due to the destructive storage mechanism it includes also errors induced during rewrite and refresh operations.
  During the storage time the DUT is performing refresh cycles. A particle hitting the device internal control circuitry can disturb or even lock the refresh process.
  S/W Conditioning, i.e. periodic refresh of the device status has been shown to reduce SEFI induced data corruption [2].
  Accordingly we differentiate between modes (a) without S/W conditioning and modes (b) with S/W conditioning.

- ./ Storage Mode, M3a/b
```
{
  write background pattern;
  verify background pattern;
  while (exposure)
  {
    perform repetitively initializing, once per second;  //optional, M3b
  }
  verify background pattern
}
```

- Read Mode (M1a/b)
  Before irradiation a pattern is written into the DUT and verified. During the exposure the content of the device is continuously read and verified. After beam stop another read cycle can be performed (M2a/bR) to differentiate between ‘Static’ and Dynamic errors.

```
// M1a/b
{
  write background pattern;
  verify background pattern;
  while (exposure)
  {
    perform initializing after x rows, each; , //optional, M1b, x configurable between
    1 and 4095
    verify background pattern;
  }
  verify background pattern;  // optional, M1a/bR
}
```

- Write Mode (M4a/b)
  The exposure is performed in dose increments ΔFluence
  .At least one background write should be fit within ΔFluence.
  During the respective fluence increment the content of the device is written once.
  After completion of the write operation the exposure is stopped, and the content is verified. Write Mode delivers Dynamic Write Errors plus some Static Errors, which have been induced during the short fluence interval taken for Background Write.
  Thereafter the next fluence increment is started.

  The DRAM Write operation is very similar to the DRAM Read operation.
  Therefore, mode M4 is not of first priority and should be executed only in case of ample beam time.

```
// M4a/b
{
 For(0, Final Fluence, ΔFluence++)
 {
    write background pattern,
    perform initializing after x rows, each; , //optional, M4b, x configurable between
    1 and 4095;
     stop exposure;
    verify background pattern;
     complete exposure until ΔFluence is reached;
   }
 }
}
```

- Write-Read Mode (M2a/b)
  During exposure ‘Write Background’ and ‘Read Background’ are cycled.
  A mixture of static and dynamic errors is delivered.
  Compared to M1 this mode could deliver additional ‘Write related’ SEFIs.
  In contrast to read mode persistent SEFIs can be cleared by power cycling.

```
// M2a/b
{
 While (exposure)
 {
   perform repetitively
   {
     power cycling;              // optional, M2b,PC
     initializing after x rows; each, // optional, M2b, x configurable between
    1 and 4095;
     write background pattern;
     initializing such as before;                    // optional, M2b
     verify background pattern;
   }
 }
}
```

6. Error Classification

The error classification scheme is similar to the scheme used for Flash errors (Fig. 6.1), with the exception that Block Errors are specific for Flash.
Due to the complex device structure, comprising a state machine and several registers, a large number of different error conditions can occur. These error conditions are classified according to Fig. 6.1 into four main classes and several subclasses.

In contrast to Dynamic Errors Static Errors remain at repeated read and are distributed randomly over the address space. The transient Dynamic Errors are differentiated further into those, which are distributed randomly and those, which are clustered. Static Errors originate from the array and Dynamic Errors from the peripheral data path. Spurious Data Errors can be handled easily with a conventional error correction scheme.

More challenging for the error correction are SEFIs. Transient SEFIs are caused by hits in the control circuitry such as in the State Machine or the spare address control register. Unlike Persistent SEFIs they disappear without the need of a device reset.

In particular the transient SEFIs are differentiated further into (i) Page Errors (*PE*) corrupting more than 100 bytes per page, (ii) Block Errors (*BE*) corrupting a series of 3…64 device pages up to the end of the respective device block and (iii) Vertical Errors (*VE*) corrupting the same byte position of subsequent device pages. Again, the VEs are split into those restricted or not restricted to one block. Additionally some characteristic error patterns are counted separately as Double PEs and Multiple BEs.

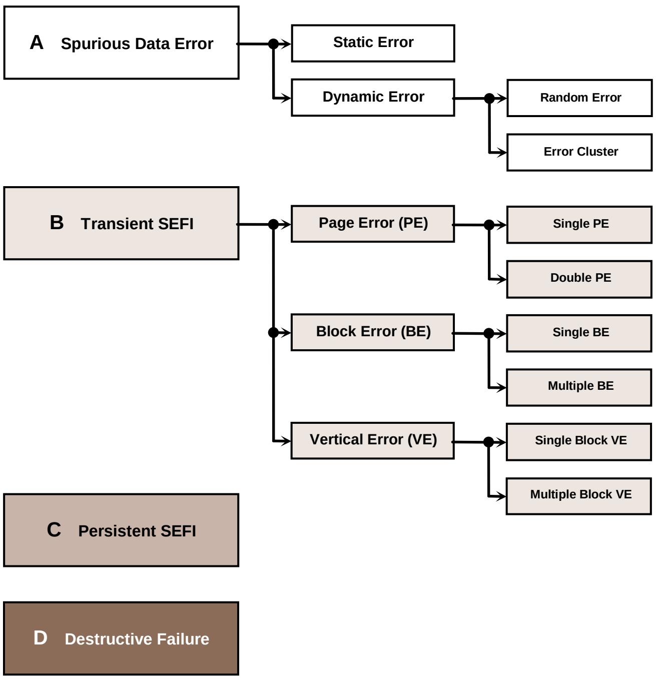


Fig.6.1: Error Classification Scheme

For the purpose of later detailed error analysis and classification all test vectors are stored. A quick look of the error distribution over the complete address space is displayed in real time. Fig. 6.2 shows an example quick look error image. Horizontal lines represent PEs, vertical lines VEs and the horizontal bar a series of block errors, which were stopped by manual power cycling.

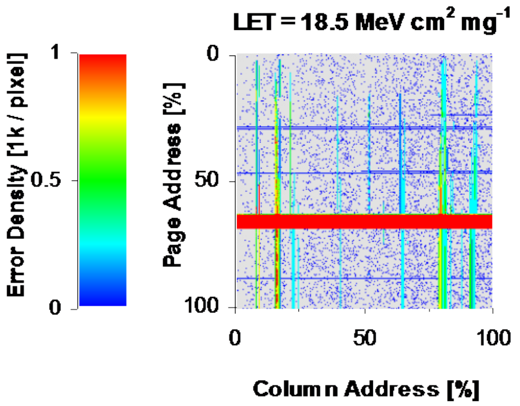


Fig. 6.2: Example Quick Look Error Image

7. Random SEU Cross Sections

7.1 General

As already mentioned the S/W of the test bed was restricted to an address range of 128M. Therefore, the test of 256Mx8bit DDR2 devices was executed only over one half of their address space. The equivalence of both parts in error counts was verified several times by manual switch-over from the default lower part of the address space to the higher part.

SDRAM show transient SEFIs (Class B) already at low LET values such as LET = 1.8 MeV cm^2 mg^{-1} of nitrogen. Therefore, the separation between the error counts by random SEUs on one hand and the SEFI induced error counts on the other hand is mandatory.

Another applied method is to restrict the calculation of the cross section to the error set until the occurrence of the first SEFI and the fluence up to this point. But, this limits the data base drastically, in particular at high LETs with more frequent SEFI occurrence.

The cross section is calculated as

$$\sigma_{SEU} = \frac{count\ of\ separated\ SEUs}{Fluence * 1.07E9} \qquad [cm^2 / bit]$$

$$\sigma_{SEFI} = \frac{count\ of\ SEFI\ pattern}{Fluence} \qquad [cm^2 / dev]$$

Very sophisticated filters for the separation of random SEUs and SEFI induced error pattern can be invented and applied. Here, we used a very simple criterion. All 32-bit data words showing one corrupted bit are counted as random SEU. All multi-bit errors are asserted to be SEFI induced.

The visual inspection of the error maps shows that this criterion is valid for nearly all error pattern. MBUs, namely multi-bit errors due to a single hit, are erroneously classified as SEFI induced. But, MBUs appeared very rarely with the exception of Xe. In consequence, the SEU rate at Xe is slightly underestimated, and the SEFI rate is slightly overestimated.

7.2 Storage Mode M3

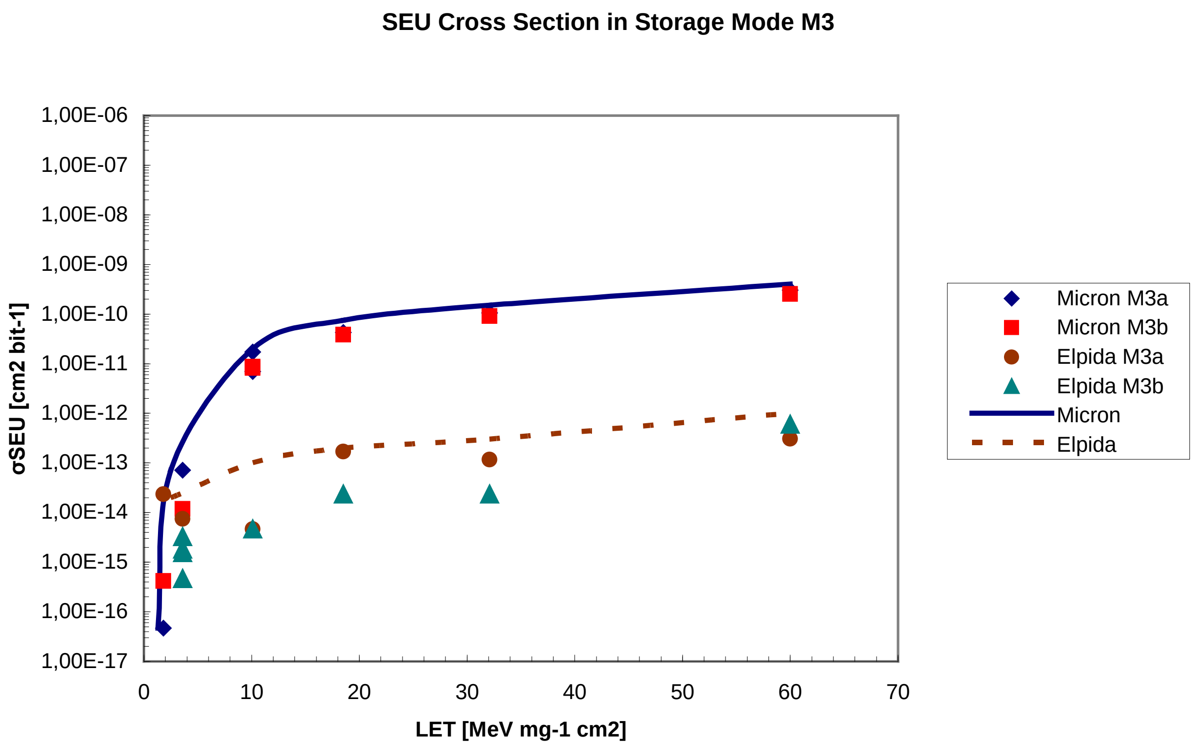


Fig. 7.1: SEU cross section in Storage Mode M3

In the Nov. 2009 campaign two Micron devices were tested in mode M3b over the full ion coctail (Nitrogen until Xenon).

Fig. 7.1 shows the SEU cross section versus LET
Tab.7.1 shows the test conditions, the error count and the calculated cross section values.

The differences in cross section between both DUTs are very minor.

In the April 2010 campaign one Micron device was tested in mode M3b only with Argon for comparison with the Nov. 2009 result, and also in mode M3a only with Argon.

Both Micron M3b Argon cross sections are in good agreement: 7.2 E-12 cm^2/bit in Nov. 09 and 8.2 E-12 cm^2/bit in April 10.

The respective M3a value is very close: 7.0 E-12 cm^2/bit.

The Micron DUTs showed only single bit errors, but no multi-bit-errors and no error clusters such as row or column errors, which could be caused by a transient SEFI (class B SEFI) of the refresh control circuitry during exposure.

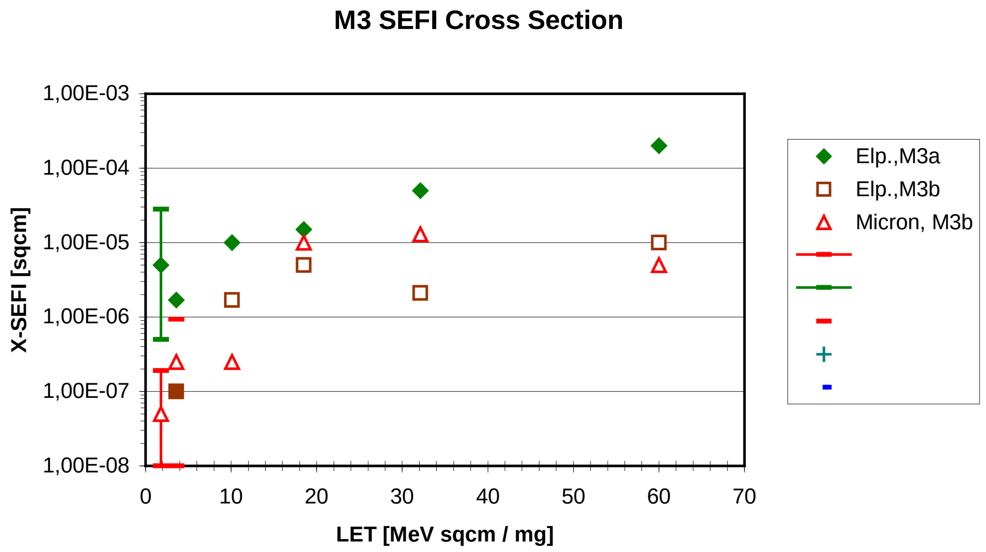


Fig. 7.2: SEFI cross section in Storage Mode M3
Open symbol indicates: No errors up to the applied fluence,
i.e. cross section ≤ indicated value

In the 2010 campaign one Elpida device was tested in both modes M3a and M3b over the full ion cocktail.

The Elpida test data differ from the Micron test data in two points:

(1) In contrast to the Micron DUTs the Elpida DUT showed SEFIs, in M3a at each run at each ion species and in M3b in the Ne-run, which exceeded all other runs by its substantially larger fluence of 2.0E7 cm^{-2}.

(2) In contrast to the Micron DUTs the Elpida DUT showed a roughly by two orders of magnitude lower SEU cross section.

In other words, the Elpida cell is less sensitive than the Micron cell,
but the Elpida control circuitry is more sensitive than the Micron control circuitry.

All SEFIs were row errors (X-SEFI = X_Row).

Fig. 7.2 shows the SEFI cross section of the Micron device in Mode M3b and of the Elpida device in both modes M3a and M3b.

For a future campaign it would be of interest to expose the Elpida device in Mode M3b to larger fluences, in case of no SEFI occurrence up to a fluence of 1.0E7 cm^{-2}.

In the Elpida M3a test the read after irradiation was followed by a second read and then by a short initialization and a third read. Tab. 7.2 shows the outcome of these repeated read actions.

Ion	N	Ne			Ar	Fe	Kr	Xe
LET [MeV sqcm / mg]	1.8	3.6			10.1	18.5	32.1	60
First Read	1	5	0	0	2	3	2	> 20 ?
Second Read	1	4	0	0	2	3	2	> 20 ?
Third Read after initialization	1	3	5	> 20 ?	2	3	1	> 20 ?

Tab. 7.2: Row errors in mode M3a, Elpida

In the Ar-run and in the Fe-run row errors showed up in all three read actions and withstood the initialization before the third read. This can be explained easily by a write access to a wrong row.

In the N-run and also in the Kr-run one of the row errors disappeared after initialization, and in the N run also another row error between the first and the second read. Here, the explanation is still open.

A curiosity is that Nitrogen delivers a larger SEU cross section than Neon with its larger LET value.. This is the case in all three modes Storage M3, Read M1 and Write-Read M2. Possibly this might be caused by a spoilage of the beam with few ions of larger LET.

For a future campaign it would be of interest to repeat the N and Ne runs.

7.3 Read Mode M1

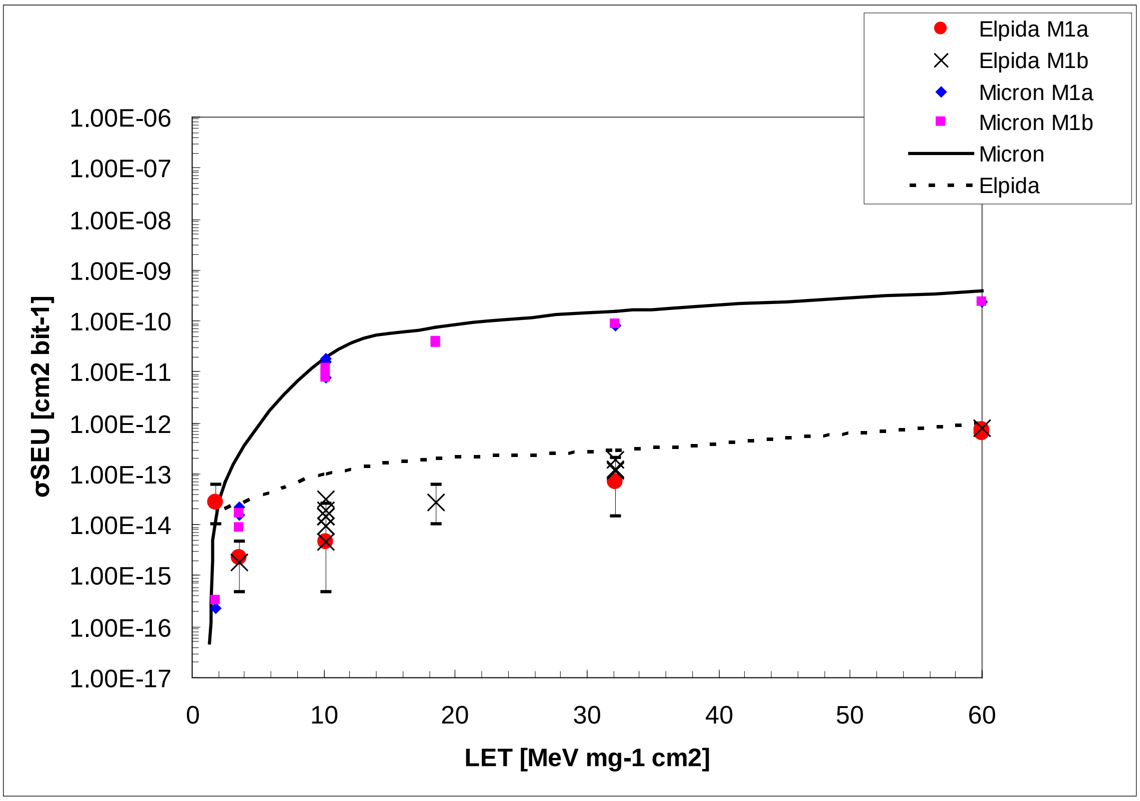


Fig. 7.3: Cross section of single bit errors in Read Mode M1

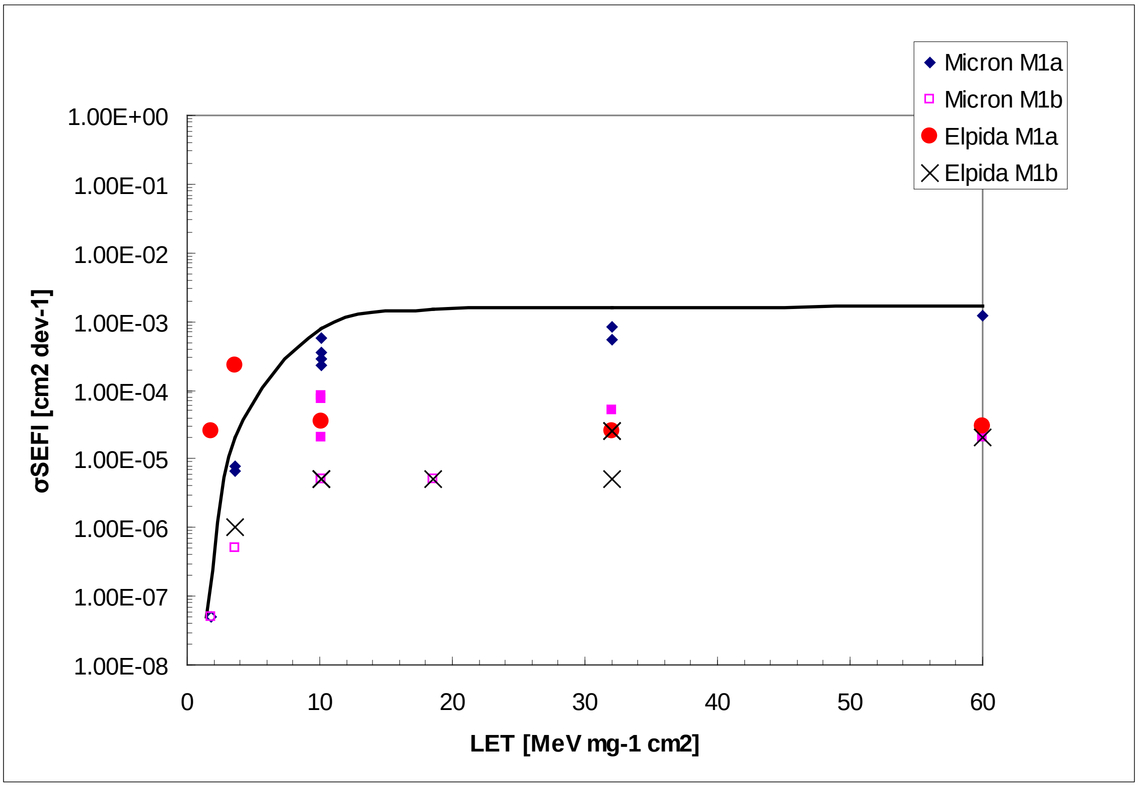


Fig.7.4: Class B SEFI Cross section in Read Mode M1

Fig. 7.1 exhibits the SEU cross section in Read Mode M1, and Fig. 7.2 the respective SEFI cross section.

The Elpida SEU cross section remains significantly below the Micron SEU cross section. The difference accounts to roughly two orders of magnitude.

For the initial test Argon was used. The substantial difference between the Micron and the Elpida SEU cross section gave occasion to repeat the M1b test several times.

Initializing every second does not influence the SEU count such as expected. A disturbance of a refresh action is very unlikely to produce distributed errors, but prone to produce cluster of corrupted 32-bit words containing more than one erroneous bit.

8.3 Storage Mode M3

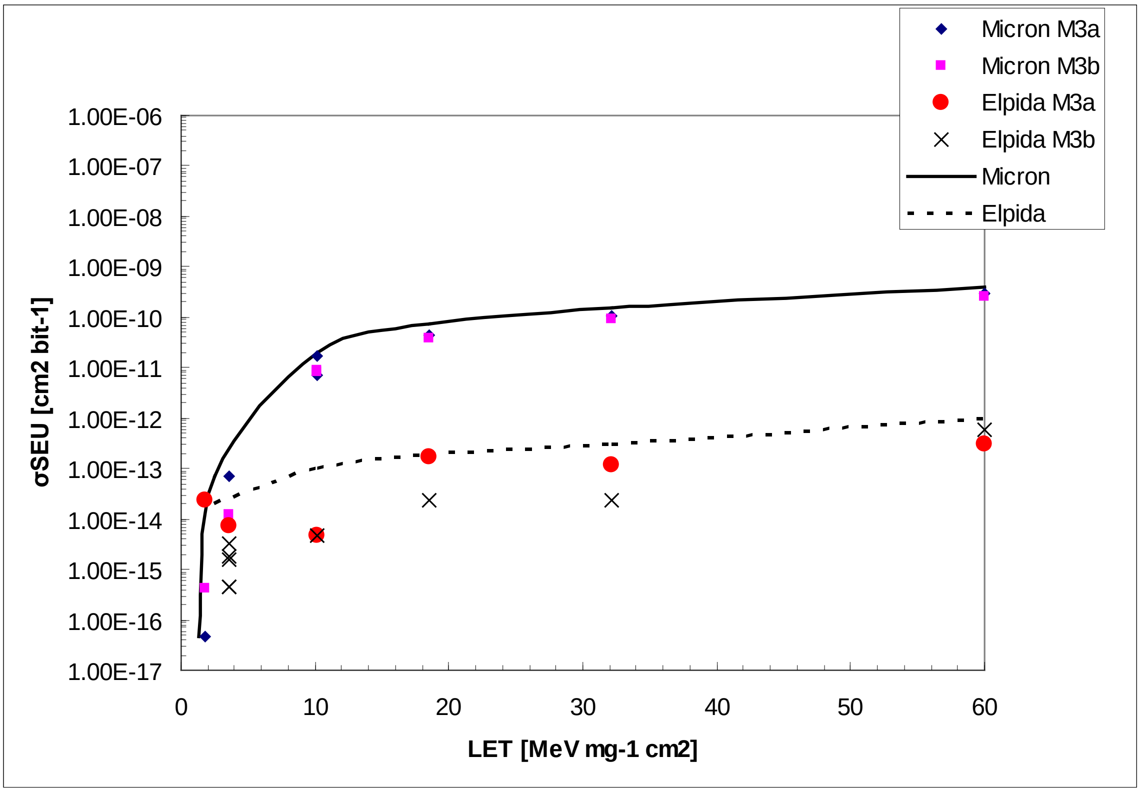


Fig. 1: Cross section of single bit errors on Storage Mode M3

The cross sections of Storage Mode M3 and Read Mode M1 are nearly identical. Nearly all SEUs are static. In M3 no SEFIs were observed.

8.4 Marching Mode M2

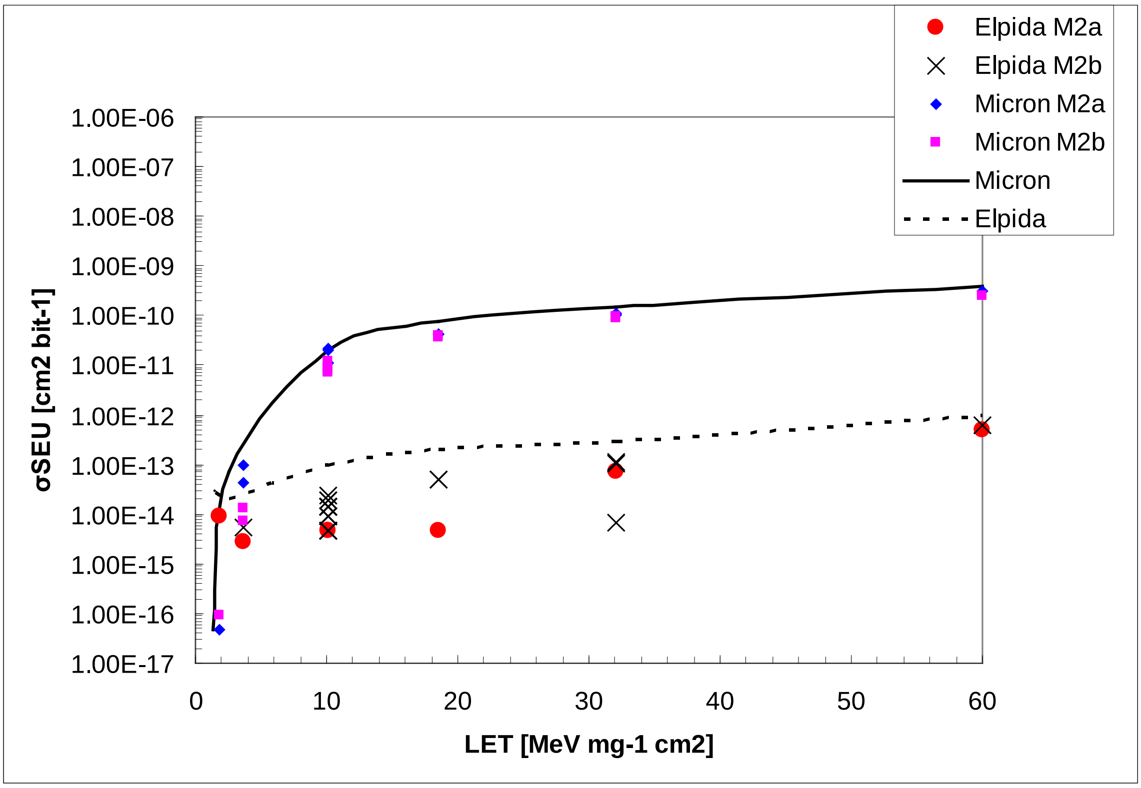


Fig. 2: Cross section of single bit errors in Marching Mode M2

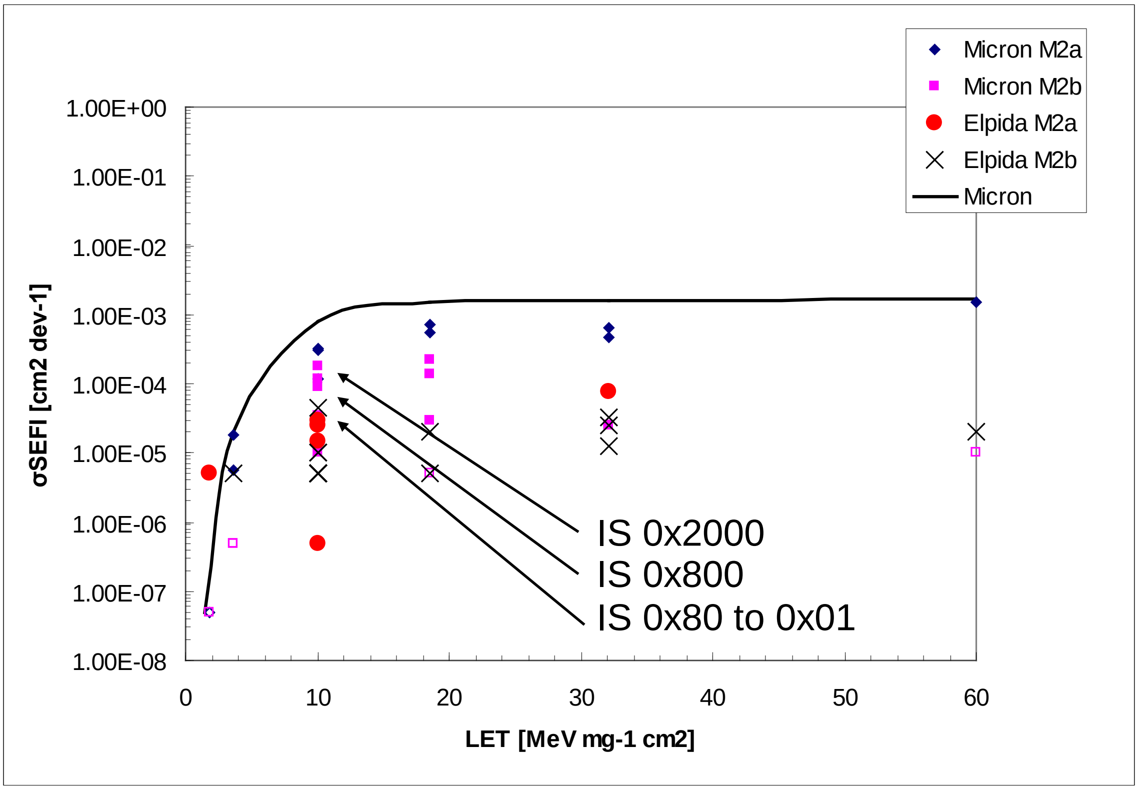
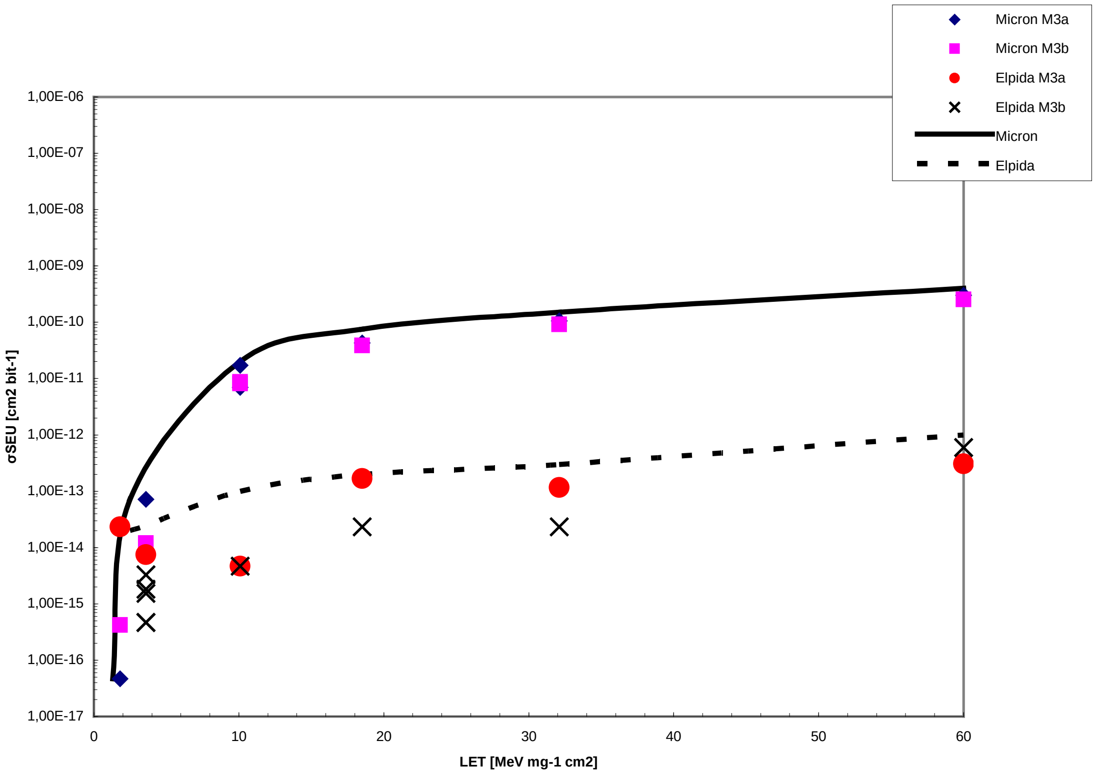
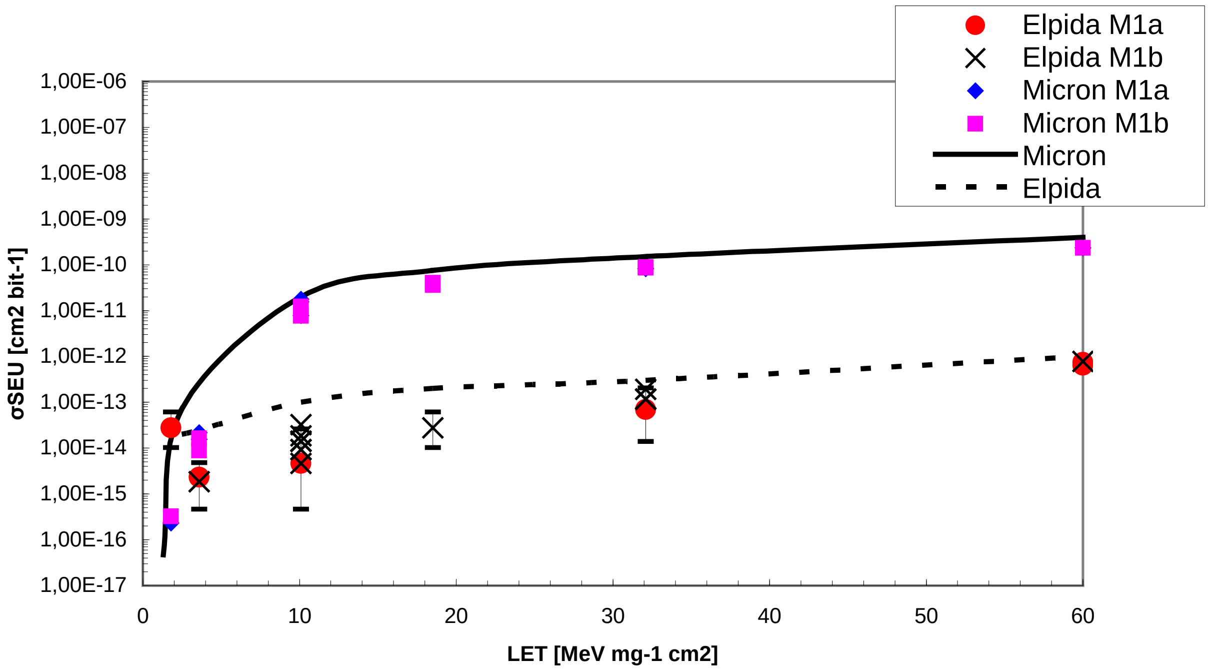
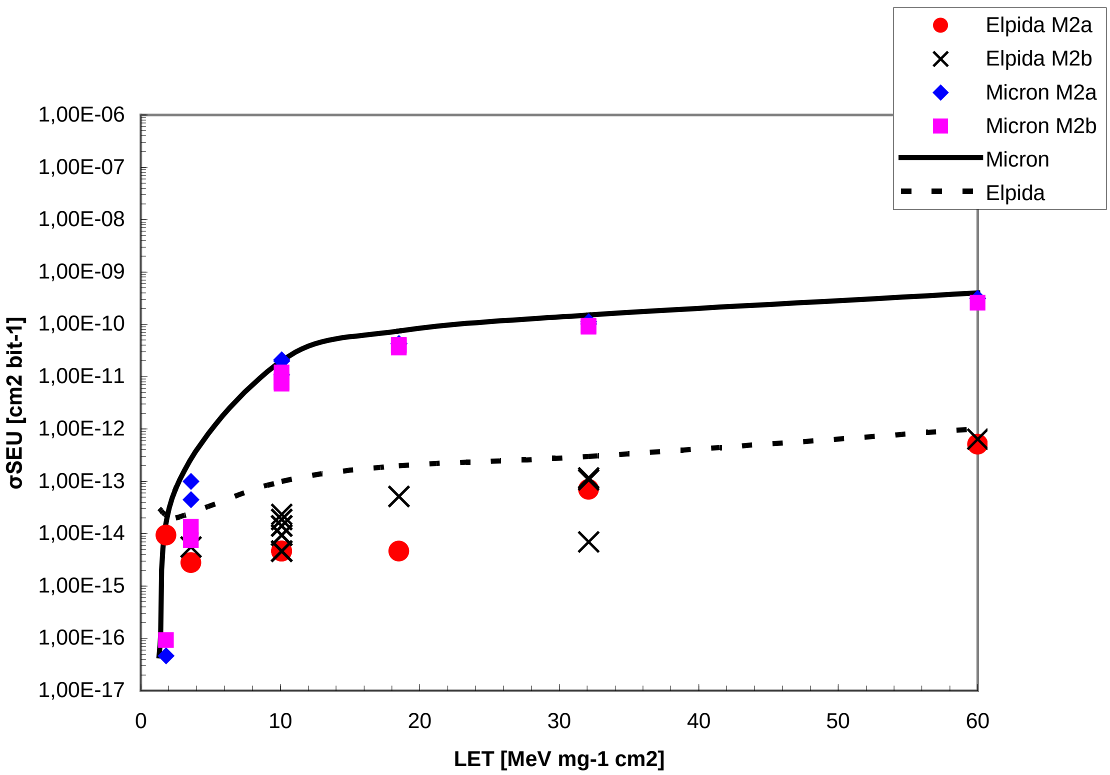


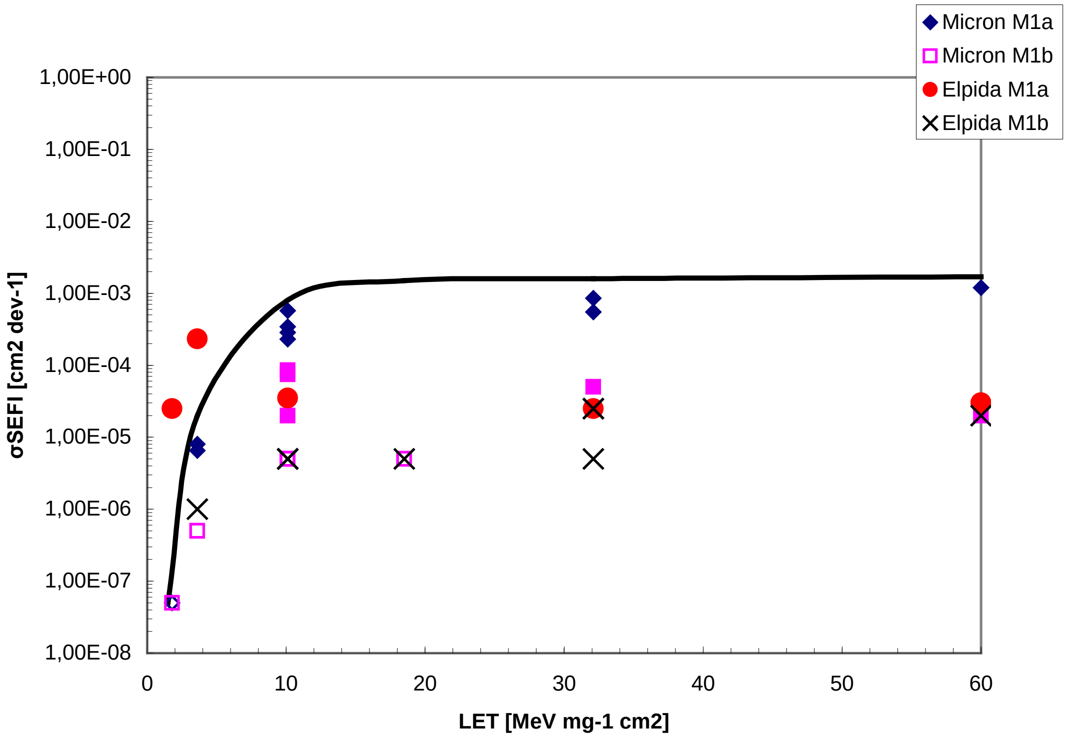
Fig. 3: Class B SEFI Cross section in Marching Mode M2

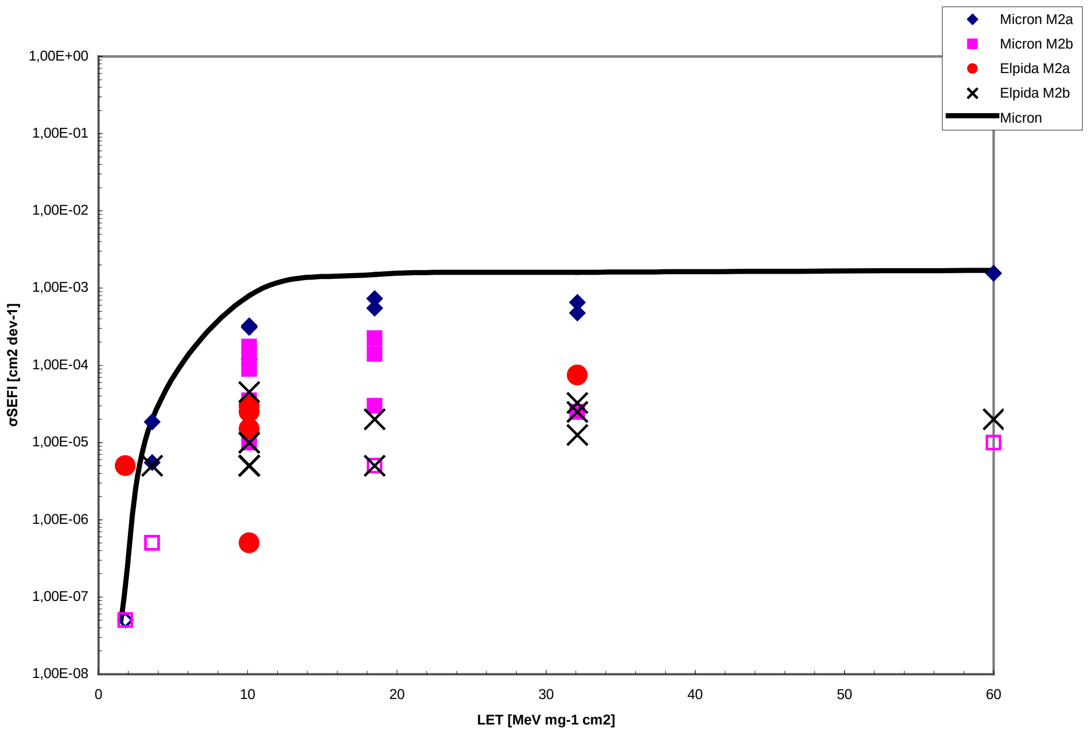
Short initialisation (IS) is very effective against SEFI-induced data corruption. The strongest reduction of SEFIs was observed with a initialisation period between 1 and 128 rows. If the initialisation period is elongated in the range of 2048 to 8192 rows the reduction of the SEFI count is only moderate.




Elpida M1a
Elpida M1b
Micron M1a
Micron M1b
Micron
Elpida
1,00E-06
1,00E-07
1,00E-08
1,00E-09
1,00E-10
1,00E-11
1,00E-12
1,00E-13
1,00E-14
1,00E-15
1,00E-16
1,00E-17
σSEU [cm2 bit-1]
0
10
20
30
40
50
60
LET [MeV mg-1 cm2]


Elpida M2a
Elpida M2b
Micron M2a
Micron M2b
Micron
Elpida
1,00E-06
1,00E-07
1,00E-08
1,00E-09
1,00E-10
1,00E-11
1,00E-12
1,00E-13
1,00E-14
1,00E-15
1,00E-16
1,00E-17
σSEU [cm2 bit-1]
0
10
20
30
40
50
60
LET [MeV mg-1 cm2]


Micron M1a
Micron M1b
Elpida M1a
Elpida M1b
σSEFI [cm2 dev-1]
1,00E+00
1,00E-01
1,00E-02
1,00E-03
1,00E-04
1,00E-05
1,00E-06
1,00E-07
1,00E-08
0
10
20
30
40
50
60
LET [MeV mg-1 cm2]


Micron M2a
Micron M2b
Elpida M2a
Elpida M2b
Micron
σSEFI [cm2 dev-1]
1,00E+00
1,00E-01
1,00E-02
1,00E-03
1,00E-04
1,00E-05
1,00E-06
1,00E-07
1,00E-08
0
10
20
30
40
50
60
LET [MeV mg-1 cm2]

8. Further Characterization of Micron 2-Gbit DDR2 SDRAMs

8.1 Test Goal

This test will be focused on the SEFI behaviour of Micron 2-Gbit DDR2 SDRAMS and the efficiency of countermeasures.

In the Nov. 2009 test we found that

1. no apparent SEFIs were introduced in Storage Mode M3.
   on the other hand one could imagine that this could be the case
   during refresh operations.
   The evaluation of Read Data showed the existence of minor SEFIs,
   which can not be recognized on the condensed error map.
   To validate the non-existence of SEFIs in Storage Mode we plan to run
   again an M3a/b test at Kr. Both tests should deliver the same SEU count and no SEU clusters.

2. In Read Mode M1 as well as in Write/Read Mode M2 we found – as expected – that re-initialization after each row access is very effective against SEFI-induced data corruption.
   But not all SEFI-induced error cluster did disappear with the next row.
   From the two applicable types of re-initialization we used the "short type", which restores the proper contents of the control registers.
   The "long type" additionally checks ad restores the proper timing of the sampling of the incoming address / data.
   Apparently falsifications of this internal flexible timing can not be excluded.

   In consequence we plan to run M1 and M2 tests

   a. Without re-initialization

   b. Using "short initialization" with different time periods as
      after each row,
      after 16 rows, each
      after 256 rows, each
      a.s.o , dependent on the outcome.

   c. Using "long initialization" after each complete address cycle

   d. Using "long initialization" after each address cycle
      plus "Short initialization" after each row.

8.2 Test Conditions

As already mentioned the S/W of the test equipment is restricted to an address range of 128 M. Therefore, the test of 2-Gbit DDR2 devices will be executed only over one half of their 2-Gbit address space. The similarity between both parts of the address space will be verified occasionally by manual switch-over from the default lower part to the higher part.
In contrast to NAND-Flashs the time needed for background write before irradiation and verification read after irradiation are nearly negligible in comparison to the beam time needed to impose an error prone fluence. Continuous Write or Read of the 256k x 8 organized device at a clock rate of 125 MHz takes 2s. In our test-bed Write and Read are done in bursts of 8 byte, with pauses in between. This extends the write and read time by a factor of four to 8 s of the full address range, and 4s to the one half of the address range tested..

In consequence, the duration of the test runs is mainly determined by the applied fluence-flux-combination.

The fluence / flux combinations will be chosen in accordance with the previous test in Nov. 2009, namely:

Ion Species	LET [MeV $cm^2 mg^{-1}$]	Fluence [cm^{-3}]	Flux [$cm^{-3} s^{-1}$}	Beam Time 8s]
N	1.8	2.0E7	8.0E4	250
Ne	3.6	2.0E6	2.0E4	100
Ar	10.1	2.0E5	2.0E3	100
Fe	18.5	2.0E5	2.0E3	100
Kr	32.0	4.0E4	4.0E2	100
Xe	60	Tbd	tbd	Tbd

8.3 DDR2 DUTs

DUT ID	Count	Type Code	Date Code
MIC1g – MIC1V	15	Micron 2-Gbit MT47H256M8HG-37E	0742
		Elpida 2_gbit EDE2108ABSE8G-E	0811

8.4 Test Sequences

Micron MT47H256M8HG-37E DDR2-SDRAM, Mode M1a

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initiali-sation	Loops	Time	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
09/133	140	15N4+	1,8	M1aR	Mic1d	none	58	264	2,0E+07	7,6E+04	2,65E+03	5	0	2,33E-16	0	0	5,00E-08	0
09/134						R	1		2,0E+07			5	0	2,33E-16	0	0	5,00E-08	0
10/290	328	15N4+	1,8	M1a	Mic1k	none	54	242	2,0E+05	8,3E+02	1,20E+03	6	0	2,79E-14	4	0	2,00E-05	0
10/291						none	1		2,0E+05			6	0	2,79E-14	4	0	2,00E-05	0
10/292						IS	1		2,0E+05			118	0	5,49E-13	0	0	5,00E-06	0
Σ		**15N4+**	**1,8**	**M1a**					**2,0E+07**	**7,7E+04**		**11**	**0**	**5,07E-16**	**4**	**0**	**1,98E-07**	**0**
09/100	127	20Ne6+	3,6	M1aR	Mic1a	none	13	55	2,0E+06	3,6E+04	7,23E+02	47	0	2,19E-14	4	12	8,00E-06	0
09/101						R	1		2,0E+06			47	0	2,19E-14	4	12	8,00E-06	0
09/102						ISR	1		2,0E+06			41	0	1,91E-14	0	0	5,00E-07	0
09/116	133	20Ne6+	3,6	M1aR	Mic1d	none	21	86	2,0E+06	2,3E+04	5,72E+02	33	0	1,54E-14	12	1	6,50E-06	0
09/117						R	1		2,0E+06			33	0	1,54E-14	12	1	6,50E-06	0
09/118									2,0E+06			69	0	3,21E-14	0	0	5,00E-07	0
Σ		**20Ne6+**	**3,6**	**M1a**					**4,0E+06**	**6,0E+04**		**80**	**0**	**1,86E-14**	**16**	**13**	**7,25E-06**	**0**
09/12	96	40Ar12+	10,1	M1aR	Mic1a	none	29	130	2,0E+05	1,5E+03	1,29E+02	403	0	1,88E-12	32	84	5,80E-04	0
09/13						none	1		2,0E+05			1725	0	8,03E-12	48	21	3,45E-04	0
09/14						IS	1		2,0E+05			2616	0	1,22E-11	0	0	5,00E-06	0
09/16	97	40Ar12+	10,1	M1aR	Mic1a	none	4	15	2,1E+04	1,4E+03	1,33E+02	402	52	1,78E-11	4	8	5,71E-04	0
09/53	112	40Ar12+	10,1	M1aR	Mic1d	none	24	104	2,0E+05	1,9E+03	1,29E+02	1679	9	7,82E-12	32	25	2,85E-04	0
09/54						R	1		2,0E+05			1678	0	7,81E-12	32	25	2,85E-04	0
09/55						ISR	1		2,0E+05			1687	0	7,86E-12	0	0	5,00E-06	0
09/72	118	40Ar12+	10,1	M1aR	Mic1f	none	22	99	2,0E+05	2,0E+03	9,70E+01	3374	893	1,57E-11	28	18	2,30E-04	0
09/73						R	1		2,0E+05			3410	0	1,59E-11	28	18	2,30E-04	0
09/74						ISR	1		2,0E+05			3293	0	1,53E-11	0	0	5,00E-06	0
10/32	12	40Ar12+	10,1	M1a	Mic1k	none	26	114	2,0E+05	1,8E+03	9,70E+01	2074	20	9,66E-12	51	9	3,00E-04	0
10/33						none	1		2,0E+05			2074	0	9,66E-12	51	9	3,00E-04	0
10/34						IS	1		2,0E+05			2195	0	1,02E-11	6	0	3,00E-05	0
10/35						IL	1		2,0E+05			2195	0	1,02E-11	6	0	3,00E-05	0
Σ		**40Ar12+**	**10,1**	**M1a**					**8,2E+05**	**8,6E+03**		**7932**	**974**	**9,00E-12**	**147**	**144**	**3,54E-04**	**0**
09/159	150	56Fe15+	18,5	M1aR	Mic1a	none	26	118	2,0E+05	1,7E+03	2,46E+03	7814	0	3,64E-11	100	76	8,80E-04	0
09/160						R	1		2,0E+05			7814	0	3,64E-11	100	76	8,80E-04	0
09/161						ISR	1		2,0E+05			8882	0	4,14E-11	0	0	5,00E-06	0
09/205	162	56Fe15+	18,5	M1aR	Mic1d	none	1	97	2,0E+05	2,1E+03	4,61E+03	0	0	4,66E-15	0	0	5,00E-06	1
09/206						ISR	1		2,0E+05			9334	0	4,35E-11	1	0	5,00E-06	0
Σ		**56Fe15+**	**18,5**	**M1a**					**4,0E+05**	**3,8E+03**		**7814**	**0**	**1,82E-11**	**100**	**76**	**4,40E-04**	**1**
09/228	170	82Kr22+	32,1	M1aR	Mic1d	none	23	109	4,0E+04	3,7E+02	4,95E+03	3517	18	8,19E-11	12	10	5,50E-04	0
09/229						R	1		4,0E+04			3576	0	8,33E-11	12	10	5,50E-04	0
09/230						ISR	1		4,0E+04			3737	0	8,70E-11	0	0	2,50E-05	0
09/247	176	82Kr22+	32,1	M1aR	Mic1a	none	21	96	4,0E+04	4,2E+02	2,82E+03	3597	3	8,37E-11	24	10	8,50E-04	0
09/248						R	1		4,0E+04			3654	0	8,51E-11	24	10	8,50E-04	0
09/249						ISR	1		4,0E+04			3807	0	8,86E-11	0	0	2,50E-05	0
Σ		**82Kr22+**	**32,1**	**M1a**					**8,0E+04**	**7,8E+02**		**7114**	**21**	**8,28E-11**	**36**	**20**	**7,00E-04**	**0**
09/267	234	131Xe35+	60	M1a	Mic1a	none	22	98	1,0E+05	1,0E+03	3,17E+03	24983	530	2,33E-10	93	27	1,20E-03	0
09/268						R	1		1,00E+05			25025	0	2,33E-10	92	27	1,19E-03	0
09/269						ISR	1		1,00E+05			26965	0	2,51E-10	0	0	1,00E-05	0
09/289	241	131Xe35+	60	M1a	Mic1d	none	21	126	1,00E+05	7,9E+02	5,40E+03			9,31E-15			1,00E-05	1
09/290						R	1		1,00E+05					9,31E-15			1,00E-05	1
09/291						ISR	1		1,00E+05					9,31E-15			1,00E-05	1

Micron MT47H256M8HG-37E DDR2-SDRAM, Mode M1b (1/2)

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initiali-sation	Loops	Time [s]	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
09/136	141	15N4+	1,8	M1bR	Mic1d	RAIS1	57	261	2,0E+07	7,7E+04	3,22E+03	7	0	3,26E-16	0	0	5,00E-08	0
09/137						RAIS1	1		2,0E+07			7	0	3,26E-16	0	0	5,00E-08	0
Σ		**15N4+**	**1,8**	**M1b**					**2,0E+07**	**7,7E+04**		**7**	**0**	**3,26E-16**	**0**	**0**	**5,00E-08**	**0**
09/104	128	20Ne6+	3,6	M1bR	Mic1a	RAIS1	15	66	2,0E+06	3,0E+04	8,38E+02	35	1	1,63E-14	0	0	5,00E-07	0
09/105						RAIS1	1		2,0E+06			33	0	1,54E-14	0	0	5,00E-07	0
09/120	134	20Ne6+	3,6	M1bR	Mic1d	RAIS1	20	90	2,0E+06	2,2E+04	6,87E+02	19	0	8,85E-15	0	0	5,00E-07	0
09/121						RAIS1	1		2,0E+06			18	0	8,38E-15	0	0	5,00E-07	0
Σ		**20Ne6+**	**3,6**	**M1b**					**4,0E+06**	**5,3E+04**		**54**	**1**	**1,26E-14**	**0**	**0**	**2,50E-07**	**0**
09/7	94	40Ar12+	10,1	M1bR	Mic1a	RAIS1	27	128	2,0E+05	1,6E+03	9,70E+01	1855	2	8,64E-12	0	0	5,00E-06	0
09/8						RAIS1	1		2,0E+05			1854	0	8,63E-12	0	0	5,00E-06	0
09/57	113	40Ar12+	10,1	M1bR	Mic1d	RAIS1	23	103	2,0E+05	1,9E+03	1,62E+02	1646	0	7,66E-12	0	0	5,00E-06	0
09/58						RAIS1	1		2,0E+05			1643	0	7,65E-12	0	0	5,00E-06	0
09/80	120	40Ar12+	10,1	M1bR	Mic1f	RAIS1	21	96	2,0E+05	2,1E+03	1,62E+02			4,66E-15			5,00E-06	1
09/81						RAIS1	1		2,0E+05			2545	0	1,19E-11	0	0	5,00E-06	0
09/83	121	40Ar12+	10,1	M1bR	Mic1f	RAIS1	22	98	2,0E+05	2,0E+03	1,94E+02	2630	0	1,22E-11	0	0	5,00E-06	0
09/84						RAIS1	1		2,0E+05			2628	0	1,22E-11	0	0	5,00E-06	0
10/53	17	40Ar12+	10,1	M1b	Mic1k	RAIS_0x2000	25	111	2,0E+05	1,8E+03	1,29E+02	1919	7	8,94E-12	6	11	8,50E-05	0
10/54						IS	1		2,0E+05			1920	0	8,94E-12	0	0	5,00E-06	0
10/56	18	40Ar12+	10,1	M1b	Mic1k	RAIS_0x1000	28	127	2,0E+05	1,6E+03	1,62E+02	1859	6	8,66E-12	0	16	5,00E-06	0
10/57						IS	1		2,0E+05			1871	0	8,71E-12	0	0	5,00E-06	0
10/59	19	40Ar12+	10,1	M1b	Mic1k	RAIS_0x800	23	94	2,0E+05	2,1E+03	1,94E+02	1859	5	8,66E-12	2	13	7,50E-05	0
10/60						IS	1		2,0E+05			1849	0	8,61E-12	0	0	5,00E-06	0
10/62	20	40Ar12+	10,1	M1b	Mic1k	RAIS_0x200	20	87	2,0E+05	2,3E+03	2,26E+02	1881	3	8,76E-12	0	1	5,00E-06	0
10/63						IS	1		2,0E+05			1882	0	8,76E-12	0	0	5,00E-06	0
10/65	21	40Ar12+	10,1	M1b	Mic1k	RAIS_0x100	21	95	2,0E+05	2,1E+03	2,59E+02	1930	0	8,99E-12	0	4	5,00E-06	0
10/66						IS	1		2,0E+05			1943	0	9,05E-12	0	0	5,00E-06	0
10/68	22	40Ar12+	10,1	M1b	Mic1k	RAIS_0x80	23	104	2,0E+05	1,9E+03	2,91E+02	2098	0	9,77E-12	15	2	8,50E-05	0
10/69						IS	1		2,0E+05			2104	0	9,80E-12	15	0	7,50E-05	0
10/71	23	40Ar12+	10,1	M1b	Mic1k	RAIS_0x40	22	97	2,0E+05	2,1E+03	3,23E+02	1977	1	9,21E-12	0	0	5,00E-06	0
10/72						IS	1		2,0E+05			1978	0	9,21E-12	0	0	5,00E-06	0
10/74	24	40Ar12+	10,1	M1b	Mic1k	RAIS_0x20	27	122	2,0E+05	1,6E+03	3,56E+02	1972	0	9,18E-12	0	0	5,00E-06	0
10/75						IS	1		2,0E+05			1980	0	9,22E-12	0	0	5,00E-06	0
10/77	25	40Ar12+	10,1	M1b	Mic1k	RAIS_0x10	23	100	2,0E+05	2,0E+03	3,88E+02	2019	0	9,40E-12	0	0	5,00E-06	0
10/78						IS	1		2,0E+05			2020	0	9,41E-12	0	0	5,00E-06	0
10/80	26	40Ar12+	10,1	M1b	Mic1k	RAIS_0x8	23	101	2,0E+05	2,0E+03	4,20E+02	1977	2	9,21E-12	0	0	5,00E-06	0
10/81						IS	1		2,0E+05			1979	0	9,22E-12	0	0	5,00E-06	0
10/83	27	40Ar12+	10,1	M1b	Mic1k	RAIS_0x4	24	106	2,0E+05	1,9E+03	4,52E+02	1998	0	9,30E-12	0	0	5,00E-06	0
10/84						IS	1		2,0E+05			1999	0	9,31E-12	0	0	5,00E-06	0
10/86	28	40Ar12+	10,1	M1b	Mic1k	RAIS_0x2	28	126	2,0E+05	1,6E+03	4,85E+02	1911	0	8,90E-12	0	0	5,00E-06	0
10/87						IS	1		2,00E+05			1912	0	8,90E-12	0	0	5,00E-06	0
10/88						IS	1		2,00E+05			1912	0	8,90E-12	0	0	5,00E-06	0
10/90	29	40Ar12+	10,1	M1b	Mic1k	RAIS_0x1	26	120	2,00E+05	1,7E+03	5,17E+02	2034	1	9,47E-12	1	0	5,00E-06	0
10/91						IS	1		2,00E+05			2034	0	9,47E-12	0	0	5,00E-06	0
10/164	47	40Ar12+	10,1	M1b	Mic1k	RAIS1	24	108	2,00E+05	1,9E+03	1,10E+03	2180	0	1,02E-11	0	0	5,00E-06	0
10/165						IS	1		2,00E+05			2181	0	1,02E-11	0	0	5,00E-06	0
Σ		**40Ar12+**	**10,1**	**M1b**					**3,40E+06**	**3,2E+04**		**33745**	**27**	**9,24E-12**	**24**	**47**	**2,09E-05**	**1**

Micron MT47H256M8HG-37E DDR2-SDRAM, Mode M1b (2/2)

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initiali-sation	Loops	Time	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
09/163	151	56Fe15+	18,5	M1bR	Mic1a	RAIS1	25	115	2,0E+05	1,7E+03	2,52E+03	7789	1	3,63E-11	0	0	5,00E-06	0
09/164						RAIS1	1		2,0E+05			7808	0	3,64E-11	0	0	5,00E-06	0
09/208	163	56Fe15+	18,5	M1bR	Mic1d	RAIS1	22	97	2,0E+05	2,1E+03	4,67E+03	8714	2	4,06E-11	0	0	5,00E-06	0
09/209						RAIS1	1		2,0E+05			8714	0	4,06E-11	0	0	5,00E-06	0
Σ		**56Fe15+**	**18,5**	**M1b**					**4,0E+05**	**3,8E+03**		**16503**	**3**	**3,84E-11**	**0**	**0**	**2,50E-06**	**0**
09/232	171	82Kr22+	32,1	M1bR	Mic1d	RAIS1	23	105	4,0E+04	3,8E+02	4,97E+03	3787	1	8,82E-11	0	0	2,50E-05	0
09/233						RAIS1	1		4,0E+04			4027	0	9,38E-11	0	0	2,50E-05	0
09/251	177	82Kr22+	32,1	M1bR	Mic1a	RAIS1	21	96	4,0E+04	4,2E+02	2,84E+03	3716	2	8,65E-11	2	0	5,00E-05	0
09/252						RAIS1	1		4,0E+04			5982	0	1,39E-10	0	0	2,50E-05	0
Σ		**82Kr22+**	**32,1**	**M1b**					**8,0E+04**	**8,0E+02**		**7503**	**3**	**8,73E-11**	**2**	**0**	**2,50E-05**	**0**
09/271	235	131Xe35+	60	M1bR	Mic1a	RAIS1	21	95	1,0E+05	1,1E+03	3,27E+03	25003	10	2,33E-10	2	0	2,00E-05	0
09/272						RAIS1	1		1,0E+05			52169	0	4,86E-10	0	0	1,00E-05	0
09/298	243	131Xe35+	60	M1bR	Mic1d	RAIS1	31	141	1,0E+05	7,1E+02	5,59E+03	46189	0	4,30E-10	2	0	2,00E-05	0
09/299						RAIS1	1		1,0E+05			46189	0	4,30E-10	0	0	1,00E-05	0
09/311	247	131Xe35+	60	M1bR	Mic1d	RAIS1	31	138	1,0E+05	7,2E+02	5,97E+03	39596	0	3,69E-10	5	32	3,70E-04	0
09/312						RAIS1	1		1,0E+05			39596	0	3,69E-10	0	0	1,00E-05	0
Σ		**131Xe35+**	**60**	**M1b**					**3,0E+05**	**2,5E+03**		**110788**	**10**	**3,44E-10**	**9**	**32**	**1,37E-04**	**0**

Micron MT47H256M8HG-37E DDR2-SDRAM, Mode M2a

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initiali-sation	Loops	Time	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
09/139	142	15N4+	1,8	M2a	Mic1d	none	20	255	2,0E+07	7,8E+04	3,80E+03	0		4,66E-17	0	0	5,00E-08	0
Σ		**15N4+**	**1,8**	**M2a**					**2,0E+07**	**7,8E+04**		**0**		**4,66E-17**	**0**	**0**	**5,00E-08**	**0**
09/107	129	20Ne6+	3,6	M2a	Mic1a	none	9	115	2,0E+06	1,7E+04	9,53E+02	213		9,92E-14	24	13	1,85E-05	0
09/123	135	20Ne6+	3,6	M2a	Mic1d	none	8	95	2,0E+06	2,1E+04	8,02E+02	96		4,47E-14	8	3	5,50E-06	0
Σ		**20Ne6+**	**3,6**	**M2a**					**4,0E+06**	**3,8E+04**		**309**		**7,19E-14**	**32**	**16**	**1,20E-05**	**0**
09/18	98	40Ar12+	10,1	M2a	Mic1a	none	11	127	2,0E+05	1,6E+03	1,65E+02	4512		2,10E-11	51	14	3,25E-04	0
09/60	114	40Ar12+	10,1	M2a	Mic1d	none	8	100	2,0E+05	2,0E+03	1,94E+02	2347		1,09E-11	9	15	1,20E-04	0
09/86	122	40Ar12+	10,1	M2a	Mic1f	none	7	83	2,0E+05	2,4E+03	2,26E+02	4260		1,98E-11	36	26	3,10E-04	0
09/87						R	1		2,0E+05			514		2,39E-12	7	0	3,50E-05	0
09/88						ISR	1		2,0E+05			215		1,00E-12	3	0	1,50E-05	0
10/93	30	40Ar12+	10,1	M2a	Mic1k	none	8	105	2,0E+05	1,9E+03	5,49E+02	3094		1,44E-11	140	21	8,05E-04	0
10/94						none	1		2,0E+05			11		5,12E-14	25	2	1,35E-04	0
10/95						IS	1		2,0E+05			46		2,14E-13	44	10	2,70E-04	0
10/96						IS	1		2,0E+05			46		2,14E-13	44	10	2,70E-04	0
10/97						IS	1		2,0E+05			46		2,14E-13	44	10	2,70E-04	0
10/99	31	40Ar12+	10,1	M2a	Mic1k	none	9	110	2,0E+05	1,8E+03	5,82E+02	3032		1,41E-11	51	12	3,15E-04	0
10/100						none	1		2,0E+05			341		1,59E-12	12	1	6,50E-05	0
10/101						IS	1		2,0E+05			157		7,31E-13	16	7	1,15E-04	0
10/103	32	40Ar12+	10,1	M2a	Mic1k	none	9	105	2,0E+05	1,9E+03	6,14E+02	2465		1,15E-11	49	5	2,70E-04	0
10/104						none	1		2,0E+05			14		6,52E-14	3	2	2,50E-05	0
10/105						none	1		2,0E+05			14		6,52E-14	3	2	2,50E-05	0
10/106						IS	1		2,0E+05			108		5,03E-13	12	3	7,50E-05	0
10/272	80	40Ar12+	10,1	M2a	Mic1k	none	8	95	2,0E+05	2,1E+03	1,13E+03	2667		1,24E-11	51	21	3,60E-04	0
10/273						none	1		2,0E+05			179		8,34E-13	8	2	5,00E-05	0
10/274						IS	1		2,0E+05			373		1,74E-12	8	11	9,50E-05	0
10/276	81	40Ar12+	10,1	M2a	Mic1k	none	8	100	2,0E+05	2,0E+03	1,16E+03	2579		1,20E-11	23	24	2,35E-04	0
10/277						none	1		2,0E+05			167		7,78E-13	8	1	4,50E-05	0
10/278						IS	1		2,0E+05			188		8,75E-13	5	13	9,00E-05	0
10/280	82	40Ar12+	10,1	M2a	Mic1k	none	8	91	2,0E+05	2,2E+03	1,20E+03	1904		8,87E-12	33	15	2,40E-04	0
10/281						none			2,0E+05			5		2,33E-14	0	0	5,00E-06	0
10/282						IS			2,0E+05			110		5,12E-13	0	11	5,00E-06	0
Σ		**40Ar12+**	**10,1**	**M2a**					**1,8E+06**	**1,8E+04**		**26860**		**1,39E-11**	**443**	**153**	**3,31E-04**	**0**
09/166	152	56Fe15+	18,5	M2a	Mic1a	none	8	97	2,0E+05	2,1E+03	2,58E+03	9143		4,26E-11	107	39	7,30E-04	0
09/167						R	1		2,0E+05			470		2,19E-12	0	0	5,00E-06	0
09/168						ISR	1		2,0E+05			3558		1,66E-11	13	0	6,50E-05	0
09/211	164	56Fe15+	18,5	M2a	Mic1d	none	8	99	2,0E+05	2,0E+03	4,73E+03	9272		4,32E-11	82	28	5,50E-04	0
09/213						ISR	1		2,0E+05			3983		1,85E-11	4	0	2,00E-05	0
Σ		**56Fe15+**	**18,5**	**M2a**					**4,0E+05**	**4,1E+03**		**18415**		**4,29E-11**	**189**	**67**	**6,40E-04**	**0**
09/235	172	82Kr22+	32,1	M2a	Mic1d	none	8	101	4,0E+04	4,0E+02	4,99E+03	4809		1,12E-10	8	11	4,75E-04	0
09/236						R	1		4,0E+04			358		8,34E-12	8	0	2,00E-04	0
09/237						ISR	1		4,0E+04			589		1,37E-11	0	0	2,50E-05	0
09/254	178	82Kr22+	32,1	M2a	Mic1a	none	7	89	4,00E+04	4,5E+02	2,86E+03	4323		1,01E-10	19	7	6,50E-04	0
Σ		**82Kr22+**	**32,1**	**M2a**					**8,00E+04**	**8,5E+02**		**9132**		**1,06E-10**	**27**	**18**	**5,63E-04**	**0**
09/274	236	131Xe35+	60	M2a	Mic1a	none	9	107	1,00E+05	9,3E+02	3,36E+03	33726		3,14E-10	104	51	1,55E-03	0
09/275						R	1		1,00E+05			1933		1,80E-11	4	8	1,20E-04	0
09/276						ISR	1		1,00E+05			2078		1,94E-11	4	8	1,20E-04	0
Σ		**131Xe35+**	**60**	**M2a**					**1,00E+05**	**9,3E+02**		**33726**		**3,14E-10**	**104**	**51**	**1,55E-03**	**0**

Micron MT47H256M8HG-37E DDR2-SDRAM, Mode M2b (1/2)

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initiali-sation	Loops	Time	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
09/141	143	15N4+	1,8	M2b	Mic1d	WAIS1, RAIS1	20	255	2,0E+07	7,8E+04	4,37E+03	2		9,31E-17	0	0	5,00E-08	0
Σ		**15N4+**	**1,8**	**M2b**					**2,0E+07**	**7,8E+04**		**2**		**9,31E-17**	**0**	**0**	**5,00E-08**	**0**
09/109	130	20Ne6+	3,6	M2b	Mic1a	WAIS1, RAIS1	8	100	2,0E+06	2,0E+04	1,07E+03	29		1,35E-14	0	0	5,00E-07	0
09/112						ISR	1		2,0E+06			21		9,78E-15	0	0	5,00E-07	0
09/125	136	20Ne6+	3,6	M2b	Mic1d	WAIS1, RAIS1	8	95	2,0E+06	2,1E+04	9,17E+02	16		7,45E-15	0	0	5,00E-07	0
09/128						ISR	1		2,0E+06			4		1,86E-15	0	0	5,00E-07	0
Σ		**20Ne6+**	**3,6**	**M2b**					**4,0E+06**	**4,1E+04**		**45**		**1,05E-14**	**0**	**0**	**2,50E-07**	**0**
09/20	99	40Ar12+	10,1	M2b	Mic1a	ISWISR1ISR2	11	131	2,0E+05	1,5E+03	1,97E+02	1686		7,85E-12	9	9	9,00E-05	0
09/22	100	40Ar12+	10,1	M2b	Mic1a	WAIS1, RAIS1	10	128	2,0E+05	1,6E+03	2,30E+02	1800		8,38E-12	2	0	1,00E-05	0
09/24	101	40Ar12+	10,1	M2b	Mic1a	WAIS1k, RAIS	11	128	2,0E+05	1,6E+03	2,62E+02	1718		8,00E-12	0	7	5,00E-06	0
09/63	115	40Ar12+	10,1	M2b	Mic1d	ISWISR1ISR2	9	100	2,0E+05	2,0E+03	2,26E+02	1559		7,26E-12	13	22	1,75E-04	0
09/76	119	40Ar12+	10,1	M2b	Mic1f	ISWISR1ISR2	8	99	2,0E+05	2,0E+03	1,29E+02	2558		1,19E-11	8	16	1,20E-04	0
09/77						ISR	1		2,0E+05			7961		3,71E-11	0	2	5,00E-06	0
10/108	33	40Ar12+	10,1	M2b	Mic1k	RAIS_0x2000	10	120	2,0E+05	1,7E+03	6,46E+02	1932		9,00E-12	7	14	1,05E-04	0
10/109						none	1		2,0E+05			55		2,56E-13	0	2	5,00E-06	0
10/110						IS	1		2,0E+05			55		2,56E-13	0	2	5,00E-06	0
10/112	34	40Ar12+	10,1	M2b	Mic1k	RAIS_0x1000	9	105	2,0E+05	1,9E+03	6,79E+02	1925		8,96E-12	0	9	5,00E-06	0
10/113						none	1		2,0E+05			13		6,05E-14	0	0	5,00E-06	0
10/114						IS	1		2,0E+05			13		6,05E-14	0	0	5,00E-06	0
10/117	35	40Ar12+	10,1	M2b	Mic1k	RAIS_0x800	9	107	2,0E+05	1,9E+03	7,11E+02	2033		9,47E-12	3	7	5,00E-05	0
10/118						none	1		2,0E+05			44		2,05E-13	0	1	5,00E-06	0
10/119						IS	1		2,0E+05			44		2,05E-13	0	1	5,00E-06	0
10/121	36	40Ar12+	10,1	M2b	Mic1k	RAIS_0x400	8	93	2,0E+05	2,2E+03	7,43E+02	1814		8,45E-12	0	5	5,00E-06	0
10/122						none	1		2,0E+05			21		9,78E-14	0	1	5,00E-06	0
10/123						IS	1		2,0E+05			21		9,78E-14	0	1	5,00E-06	0
10/125	37	40Ar12+	10,1	M2b	Mic1k	RAIS_0x200	10	107	2,0E+05	1,9E+03	7,76E+02	1851		8,62E-12	0	0	5,00E-06	0
10/126						none	1		2,0E+05			1		4,66E-15	0	0	5,00E-06	0
10/127						IS	1		2,0E+05			1		4,66E-15	0	0	5,00E-06	0
10/129	38	40Ar12+	10,1	M2b	Mic1k	RAIS_0x100	9	102	2,0E+05	2,0E+03	8,08E+02	1929		8,98E-12	1	7	4,00E-05	0
10/130						none	1		2,0E+05			1		4,66E-15	0	0	5,00E-06	0
10/131						IS	1		2,0E+05			1		4,66E-15	0	0	5,00E-06	0
10/133	39	40Ar12+	10,1	M2b	Mic1k	RAIS_0x80	9	106	2,0E+05	1,9E+03	8,40E+02	1874		8,73E-12	0	0	5,00E-06	0
10/134						none	1		2,0E+05			34		1,58E-13	0	0	5,00E-06	0
10/135						IS	1		2,0E+05			34		1,58E-13	0	0	5,00E-06	0
10/137	40	40Ar12+	10,1	M2b	Mic1k	RAIS_0x40	9	107	2,0E+05	1,9E+03	8,73E+02	1856		8,64E-12	0	0	5,00E-06	0
10/138						IS	1		2,0E+05			1		4,66E-15	0	0	5,00E-06	0
10/139	41	40Ar12+	10,1	M2b	Mic1k	RAIS_0x20	8	99	2,0E+05	2,0E+03	9,05E+02	1882		8,76E-12	0	0	5,00E-06	0
10/141						none	1		2,0E+05			155		7,22E-13	0	0	5,00E-06	0
10/142						IS	1		2,0E+05			1		4,66E-15	0	0	5,00E-06	0
10/143	42	40Ar12+	10,1	M2b	Mic1k	RAIS_0x10	8	92	2,00E+05	2,2E+03	9,37E+02	1868		8,70E-12	74	0	3,70E-04	0
10/145						none	1		2,00E+05			13		6,05E-14	0	0	5,00E-06	0
10/146						IS	1		2,00E+05			1		4,66E-15	0	0	5,00E-06	0
10/147	43	40Ar12+	10,1	M2b	Mic1k	RAIS_0x8	6	74	2,00E+05	2,7E+03	9,70E+02	1868		8,70E-12	0	0	5,00E-06	0
10/149						none	1		2,00E+05			226		1,05E-12	0	0	5,00E-06	0
10/150						IS	1		2,00E+05			2		9,31E-15	0	0	5,00E-06	0
10/151	44	40Ar12+	10,1	M2b	Mic1k	RAIS_0x4	9	105	2,00E+05	1,9E+03	1,00E+03	1898		8,84E-12	0	0	5,00E-06	0
10/153						none	1		2,00E+05			20		9,31E-14	0	0	5,00E-06	0
10/154						IS	1		2,00E+05			1		4,66E-15	0	0	5,00E-06	0

Micron MT47H256M8HG-37E DDR2-SDRAM, Mode M2b (2/2)

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initiali-sation	Loops	Time	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
10/155	45	40Ar12+	10,1	M2b	Mic1k	RAIS_0x2	7	88	2,0E+05	2,3E+03	1,03E+03	1915		8,92E-12	0	0	5,00E-06	0
10/156						none	1		2,0E+05			166		7,73E-13	0	0	5,00E-06	0
10/157						IS	1		2,0E+05			166		7,73E-13	0	0	5,00E-06	0
10/159	46	40Ar12+	10,1	M2b	Mic1k	RAIS_0x1	6	76	2,0E+05	2,6E+03	1,07E+03	2004		9,33E-12	0	0	5,00E-06	0
10/160						none	1		2,0E+05			167		7,78E-13	0	0	5,00E-06	0
10/161						IS	1		2,0E+05			167		7,78E-13	0	0	5,00E-06	0
Σ		**40Ar12+**	**10,1**	**M2b**					**3,8E+06**	**3,8E+04**		**35970**		**8,82E-12**	**117**	**96**	**5,61E-05**	**0**
09/172	153	56Fe15+	18,5	M2b	Mic1a	WAIS1, RAIS1	8	103	2,0E+05	1,9E+03	2,63E+03	7711		3,59E-11	6	0	3,00E-05	0
09/173						WAIS1, RAIS1	1		2,0E+05			737		3,43E-12	0	0	5,00E-06	0
09/175	154	56Fe15+	18,5	M2b	Mic1a	WAISx2000, R.	9	110	2,0E+05	1,8E+03	2,69E+03	8594		4,00E-11	14	31	2,25E-04	0
09/176						WAISx2000, R.	1		2,0E+05			7719		3,59E-11	0	2	5,00E-06	0
09/177						IS + WAISx200	1		2,0E+05			7722		3,60E-11	0	0	5,00E-06	0
09/179	155	56Fe15+	18,5	M2b	Mic1a	WAISx2000, R.	8	99	2,0E+05	2,0E+03	2,75E+03	8653		4,03E-11	7	21	1,40E-04	0
09/180						WAISx2000, R.	1		2,0E+05			8910		4,15E-11	0	2	5,00E-06	0
09/181						IS + WAISx200	1		2,0E+05			8910		4,15E-11	0	2	5,00E-06	0
09/215	165	56Fe15+	18,5	M2b	Mic1d	WAIS1, RAIS1	8	94	2,0E+05	2,1E+03	4,79E+03	8222		3,83E-11	0	0	5,00E-06	0
09/216						WAIS1, RAIS1	1		2,0E+05			63		2,93E-13	0	0	5,00E-06	0
09/221						ISR	1		2,0E+05			21799		1,02E-10	1	0	5,00E-06	0
09/224						ISR	1		2,0E+05			3937		1,83E-11	0	0	5,00E-06	0
Σ		**56Fe15+**	**18,5**	**M2b**					**8,0E+05**	**7,9E+03**		**33180**		**3,86E-11**	**27**	**52**	**9,88E-05**	**0**
09/239	173	82Kr22+	32,1	M2b	Mic1a	WAIS1, RAIS1	7	93	4,0E+04	4,3E+02	2,78E+03	3997		9,31E-11	0	0	2,50E-05	0
09/240						WAIS1, RAIS1	1		4,0E+04			33		7,68E-13	0	0	2,50E-05	0
09/243						ISR	1		4,0E+04			3969		9,24E-11	0	0	2,50E-05	0
09/256	179	82Kr22+	32,1	M2b	Mic1a	WAIS1, RAIS1	7	91	4,0E+04	4,4E+02	2,88E+03	3861		8,99E-11	1	0	2,50E-05	0
09/257						WAIS1, RAIS1	1		4,0E+04			2419		5,63E-11	0	0	2,50E-05	0
09/261						ISR	1		4,0E+04			50443		1,17E-09	0	0	2,50E-05	0
Σ		**82Kr22+**	**32,1**	**M2b**					**8,0E+04**	**8,7E+02**		**7858**		**9,15E-11**	**1**	**0**	**1,25E-05**	**0**
09/278	237	131Xe35+	60	M2b	Mic1a	WAIS1, RAIS1	10	124	1,0E+05	8,1E+02	3,46E+03	27640		2,57E-10	0	0	1,00E-05	0
09/279						WAIS1, RAIS1	1		1,0E+05			3099		2,89E-11	0	0	1,00E-05	0
09/285						ISR	1		1,0E+05			39679		3,70E-10	0	0	1,00E-05	0
Σ		**131Xe35+**	**60**	**M2b**					**1,0E+05**	**8,1E+02**		**27640**		**2,57E-10**	**0**	**0**	**1,00E-05**	**0**

Micron MT47H256M8HG-37E DDR2-SDRAM, Mode M3a

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initiali-sation	Loops	Time	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
10/25	10	40Ar12+	10,1	M3a	Mic1k	none	1	102	2,0E+05	2,0E+03	3,23E+01	1494		6,96E-12	52	17	3,45E-04	0
10/26						none			2,0E+05			1494		6,96E-12	52	17	3,45E-04	0
10/27						IS			2,0E+05			1511		7,04E-12	0	0	5,00E-06	0
Σ		**40Ar12+**	**10,1**	**M3a**					**2,0E+05**	**2,0E+03**		**1494**		**6,96E-12**	**52**	**17**	**3,45E-04**	**0**

Micron MT47H256M8HG-37E DDR2-SDRAM, Mode M3b

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initialisation	Loops	Time	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
09/131	139	15N4+	1,8	M3b	Mic1d	IS	1	262	2,0E+07	7,6E+04	2,07E+03	5		2,33E-16	0	0	5,00E-08	0
Σ		**15N4+**	**1,8**	**M3b**					**2,0E+07**	**7,6E+04**		**5**		**2,33E-16**	**0**	**0**	**5,00E-08**	**0**
09/94	125	20Ne6+	3,6	M3b	Mic1a	IS	1	107	2,0E+06	1,9E+04	4,92E+02	36		1,68E-14	0	0	5,00E-07	0
09/114	132	20Ne6+	3,6	M3b	Mic1d	IS	1	108	2,0E+06	1,9E+04	4,57E+02	17		7,92E-15	0	0	5,00E-07	0
Σ		**20Ne6+**	**3,6**	**M3b**					**4,0E+06**	**3,7E+04**		**53**		**1,23E-14**	**0**	**0**	**2,50E-07**	**0**
09/5	93	40Ar12+	10,1	M3b	Mic1a	IS	1	127	2,0E+05	1,6E+03	6,46E+01	1612		7,51E-12	0	0	5,00E-06	0
09/51	111	40Ar12+	10,1	M3b	Mic1d	IS	1	100	2,0E+05	2,0E+03	9,70E+01	1481		6,90E-12	0	0	5,00E-06	0
10/29	11	40Ar12+	10,1	M3b	Mic1k	IS	1	116	2,0E+05	1,7E+03	6,46E+01	1759		8,19E-12	0	0	5,00E-06	0
10/30						IS	1		2,0E+05			1759		8,19E-12	0	0	5,00E-06	0
Σ		**40Ar12+**	**10,1**	**M3b**					**6,0E+05**	**5,3E+03**		**4852**		**7,53E-12**	**0**	**0**	**1,67E-06**	**0**
09/157	149	56Fe15+	18,5	M3b	Mic1a	IS	1	110	2,0E+05	1,8E+03	2,40E+03	7454		3,47E-11	0	0	5,00E-06	0
09/197	160	56Fe15+	18,5	M3b	Mic1d	IS	1	98	2,0E+05	2,0E+03	4,55E+03	8208		3,82E-11	0	0	5,00E-06	0
Σ		**56Fe15+**	**18,5**	**M3b**					**4,0E+05**	**3,9E+03**		**15662**		**3,65E-11**	**0**	**0**	**2,50E-06**	**0**
09/226	169	82Kr22+	32,1	M3b	Mic1d	IS	1	108	4,0E+04	3,7E+02	4,93E+03	3748		8,73E-11	0	0	2,50E-05	0
09/245	175	82Kr22+	32,1	M3b	Mic1a	IS	1	96	4,0E+04	4,2E+02	2,80E+03	3553		8,27E-11	0	0	2,50E-05	0
Σ		**82Kr22+**	**32,1**	**M3b**					**8,0E+04**	**7,9E+02**		**7301**		**8,50E-11**	**0**	**0**	**1,25E-05**	**0**
09/263	232	131Xe35+	60	M3b	Mic1a	IS	1	107	1,0E+05	9,3E+02	3,07E+03	27840		2,59E-10	0	0	1,00E-05	0
Σ		**131Xe35+**	**60**	**M3b**					**1,0E+05**	**9,3E+02**		**27840**		**2,59E-10**	**0**	**0**	**1,00E-05**	**0**

Elpida EDE2108ABSE-8G-E DDR2-SDRAM, Mode M1a

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initiali-sation	Loops	Time	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
10/303	332	15N4+	1,8	M1a	Elp1t	none	54	238	2,0E+05	8,4E+02	1,30E+03	6	0	2,79E-14	5	0	2,50E-05	0
10/304						none	1		2,0E+05			6	0	2,79E-14	5	0	2,50E-05	0
10/305						IS	1		2,0E+05			6	0	2,79E-14	5	0	2,50E-05	0
Σ		**15N4+**	**1,8**	**M1a**					**2,0E+05**	**8,4E+02**		**6**	**0**	**2,79E-14**	**5**	**0**	**2,50E-05**	**0**
10/414	367	20Ne6+	3,6	M1a	Elp1t	none	23	100	2,0E+06	2,0E+04	4,16E+03	5	0	2,33E-15	13	452	2,33E-04	0
10/415						none	1		2,0E+06			5	0	2,33E-15	13	452	2,33E-04	0
10/416						IS	1		2,0E+06			974	0	4,54E-13	1	0	5,00E-07	0
Σ		**20Ne6+**	**3,6**	**M1a**					**2,0E+06**	**2,0E+04**		**5**	**0**	**2,33E-15**	**13**	**452**	**2,33E-04**	**0**
10/6	4	40Ar12+	10,1	M1a	Elp1t	none	24	106	2,0E+05	1,9E+03	9,70E+01	1	0	4,66E-15	6	1	3,50E-05	0
10/7						IS	1		2,0E+05			1	0	4,66E-15	6	0	3,00E-05	0
Σ		**40Ar12+**	**10,1**	**M1a**					**2,0E+05**	**1,9E+03**		**1**	**0**	**4,66E-15**	**6**	**1**	**3,50E-05**	**0**
10/323	337	56Fe15+	18,5	M1a	Elp1t	none	12	104	2,0E+05	1,9E+03	1,49E+03			4,66E-15			5,00E-06	1
10/324						none	1		2,0E+05					4,66E-15			5,00E-06	1
10/325						IS	1		2,0E+05					4,66E-15			5,00E-06	1
Σ		**56Fe15+**	**18,5**	**M1a**					**2,0E+05**	**1,9E+03**				**4,66E-15**			**5,00E-06**	**1**
10/350	346	82Kr22+	32,1	M1a	Elp1t	none	27	118	4,0E+04	3,4E+02	1,85E+03	3	0	6,98E-14	1	0	2,50E-05	0
10/351						none	1		4,0E+04			3	0	6,98E-14	1	0	2,50E-05	0
10/352						IS	1		4,0E+04			90	0	2,10E-12	0	0	2,50E-05	0
Σ		**82Kr22+**	**32,1**	**M1a**					**4,0E+04**	**3,4E+02**		**3**	**0**	**6,98E-14**	**1**	**0**	**2,50E-05**	**0**
10/389	359	131Xe35+	60	M1a	Elp1t	none	22	96	1,0E+05	1,0E+03	3,43E+03	80	1	7,45E-13	3	0	3,00E-05	0
10/390						none	1		1,0E+05			81	0	7,54E-13	3	0	3,00E-05	0
10/395	361	131Xe35+	60	M1a	Elp1t	none	22	97	1,0E+05	1,0E+03	3,62E+03	69	0	6,43E-13	3	0	3,00E-05	0
10/396						none	1		1,0E+05			70	0	6,52E-13	4	0	4,00E-05	0
10/397						IS	1		1,0E+05			179	0	1,67E-12	0	0	1,00E-05	0
Σ		**131Xe35+**	**60**	**M1a**					**2,0E+05**	**2,1E+03**		**149**	**1**	**6,94E-13**	**6**	**0**	**3,00E-05**	**0**

Elpida EDE2108ABSE-8G-E DDR2-SDRAM, Mode M1b

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initiali-sation	Loops	Time	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
10/418	368	20Ne6+	3,6	M1b	Elp1t	RAIS1	22	99	2,0E+06	2,0E+04	4,27E+03	4	0	1,86E-15	2	0	1,00E-06	0
10/419						IS	1		2,0E+06			4	0	1,86E-15	2	0	1,00E-06	0
Σ		**20Ne6+**	**3,6**						**2,0E+06**	**2,0E+04**		**4**	**0**	**1,86E-15**	**2**	**0**	**1,00E-06**	**0**
10/9	5	40Ar12+	10,1	M1b	Elp1t	RAIS1	25	105	2,0E+05	1,9E+03	1,29E+02	3	0	1,40E-14	0	0	5,00E-06	0
10/10						IS	1		2,0E+05			3	0	1,40E-14	0	0	5,00E-06	0
10/167	48	40Ar12+	10,1	M1b	Elp1t	RAIS1	35	161	2,0E+05	1,2E+03	2,91E+02	7	0	3,26E-14	0	0	5,00E-06	0
10/168						IS	1		2,0E+05			7	0	3,26E-14	0	0	5,00E-06	0
10/170	49	40Ar12+	10,1	M1b	Elp1t	RAIS1	35	162	2,0E+05	1,2E+03	3,23E+02	3	0	1,40E-14	0	0	5,00E-06	0
10/171						IS	1		2,0E+05			3	0	1,40E-14	0	0	5,00E-06	0
10/188	54	40Ar12+	10,1	M1b	Elp1t	RAIS1	22	96	2,0E+05	2,1E+03	4,85E+02	4	0	1,86E-14	0	0	5,00E-06	0
10/189						IS	1		2,0E+05			4	0	1,86E-14	0	0	5,00E-06	0
10/191	55	40Ar12+	10,1	M1b	Elp1t	RAIS1	21	95	2,0E+05	2,1E+03	5,17E+02	3	0	1,40E-14	1	0	5,00E-06	0
10/192						IS	1		2,0E+05			3	0	1,40E-14	0	0	5,00E-06	0
10/195	56	40Ar12+	10,1	M1b	Elp1t	RAIS1	20	89	2,0E+05	2,2E+03	5,49E+02	2	0	9,31E-15	1	0	5,00E-06	0
10/196						IS	1		2,0E+05			2	0	9,31E-15	1	0	5,00E-06	0
10/198	57	40Ar12+	10,1	M1b	Elp1t	RAIS1	23	88	2,0E+05	2,3E+03	5,82E+02	1	0	4,66E-15	0	0	5,00E-06	0
10/199						IS	1		2,0E+05			0	0	4,66E-15	0	0	5,00E-06	0
10/201	58	40Ar12+	10,1	M1b	Elp1t	RAIS1	20	89	2,0E+05	2,2E+03	6,14E+02	2	0	9,31E-15	1	0	5,00E-06	0
10/202						IS	1		2,0E+05			2	0	9,31E-15	1	0	5,00E-06	0
Σ		**40Ar12+**	**10,1**						**1,6E+06**	**1,5E+04**		**25**	**0**	**1,46E-14**	**3**	**0**	**1,88E-06**	**0**
10/327	338	56Fe15+	18,5	M1b	Elp1t	RAIS1, WAIS1	23	105	2,0E+05	1,9E+03	1,55E+03	6	0	2,79E-14	1	0	5,00E-06	0
10/328						IS	1		2,0E+05			6	0	2,79E-14	1	0	5,00E-06	0
Σ		**56Fe15+**	**18,5**						**2,0E+05**	**1,9E+03**		**6**	**0**	**2,79E-14**	**1**	**0**	**5,00E-06**	**0**
10/354	347	82Kr22+	32,1	M1b	Elp1t	RAIS1	28	128	4,0E+04	3,1E+02	1,87E+03	5	0	1,16E-13	1	0	2,50E-05	0
10/355						IS	1		4,0E+04			5	0	1,16E-13	1	0	2,50E-05	0
10/367	351	82Kr22+	32,1	M1b	Elp1t	RAIS1, WAIS1	21	92	4,0E+05	4,3E+03	2,32E+03	51	0	1,19E-13	2	0	5,00E-06	0
10/368						IS	1		4,0E+05			51	0	1,19E-13	1	0	2,50E-06	0
10/376	354	82Kr22+	32,1	M1b	Elp1t	RAIS1, WAIS1	20	90	4,0E+05	4,4E+03	2,93E+03	82	0	1,91E-13	1	0	2,50E-06	0
10/377						IS	1		4,0E+05			82	0	1,91E-13	1	0	2,50E-06	0
Σ		**82Kr22+**	**32,1**						**8,4E+05**	**9,1E+03**		**138**	**0**	**1,53E-13**	**4**	**0**	**4,76E-06**	**0**
10/392	360	131Xe35+	60	M1b	Elp1t	RAIS1	21	93	1,0E+05	1,1E+03	3,52E+03	84	0	7,82E-13	2	0	2,00E-05	0
10/393						IS	1		1,0E+05			84	0	7,82E-13	2	0	2,00E-05	0
Σ		**131Xe35+**	**60**						**1,0E+05**	**1,1E+03**		**84**	**0**	**7,82E-13**	**2**	**0**	**2,00E-05**	**0**

IDA

Elpida EDE2108ABSE-8G-E DDR2-SDRAM, Mode M2a

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initiali-sation	Loops	Time	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
10/307	333	15N4+	1,8	M2a	Elp1t	none	13	219	2,0E+05	9,1E+02	1,31E+03	2		9,31E-15	0	0	5,00E-06	0
10/308						none	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/309						IS	1		2,0E+05			0		4,66E-15	1	0	5,00E-06	0
Σ		**15N4+**	**1,8**						**2,0E+05**	**9,1E+02**		**2**		**9,31E-15**	**0**	**0**	**5,00E-06**	**0**
10/421	369	20Ne6+	3,6	M2a	Elp1t	none	8	106	2,0E+06	1,9E+04	4,39E+03			4,66E-16			5,00E-07	1
10/422						none	1		2,0E+06					4,66E-16			5,00E-07	1
10/423						IS	1		2,0E+06					4,66E-16			5,00E-07	1
Σ		**20Ne6+**	**3,6**						**2,0E+06**	**1,9E+04**				**4,66E-16**			**5,00E-07**	**1**
10/12	6	40Ar12+	10,1	M2a	Elp1t	none	4	94	2,0E+05	2,1E+03	1,62E+02	1		4,66E-15	2	0	1,00E-05	0
10/13						IS	1		2,0E+05			0		4,66E-15	2	0	1,00E-05	0
10/173	50	40Ar12+	10,1	M2a	Elp1t	none	8	108	2,0E+05	1,9E+03	3,56E+02			4,66E-15			5,00E-06	1
10/174						none	1		2,0E+05					4,66E-15			5,00E-06	1
10/175						IS	1		2,0E+05					4,66E-15			5,00E-06	1
10/176						IL	1		2,0E+05					4,66E-15			5,00E-06	1
10/178	51	40Ar12+	10,1	M2a	Elp1t	none	8	95	2,0E+05	2,1E+03	3,88E+02			4,66E-15			5,00E-06	1
10/179						none	1		2,0E+05					4,66E-15			5,00E-06	1
10/180						IS	1		2,0E+05					4,66E-15			5,00E-06	1
10/182	52	40Ar12+	10,1	M2a	Elp1t	none	5	94	2,0E+05	2,1E+03	4,20E+02			4,66E-15			5,00E-06	1
10/183						none	1		2,0E+05					4,66E-15			5,00E-06	1
10/184						IS	1		2,0E+05					4,66E-15			5,00E-06	1
10/204	59	40Ar12+	10,1	M2a	Elp1t	none	8	95	2,0E+05	2,1E+03	6,46E+02	0		4,66E-15	4	1	2,50E-05	0
10/205						none	1		2,0E+05			0		4,66E-15	0	1	5,00E-06	0
10/206						IS	1		2,0E+05			0		4,66E-15	3	0	1,50E-05	0
10/208	60	40Ar12+	10,1	M2a	Elp1t	none	5	104	2,0E+05	1,9E+03	6,79E+02			4,66E-15			5,00E-06	1
10/209						none	1		2,0E+05					4,66E-15			5,00E-06	1
10/210						IS	1		2,0E+05			1		4,66E-15	0	0	5,00E-06	0
10/221	64	40Ar12+	10,1	M2a	Elp1t	none	9	110	2,0E+05	1,8E+03	8,08E+02	0		4,66E-15	3	0	1,50E-05	0
10/222						none	1		2,0E+05			0		4,66E-15	1	0	5,00E-06	0
10/223						IS	1		2,0E+05			0		4,66E-15	3	0	1,50E-05	0
10/264	78	40Ar12+	10,1	M2a	Elp1t	none	8	98	2,0E+05	2,0E+03	1,26E+03	1		4,66E-15	6	0	3,00E-05	0
10/265						none	1		2,0E+05			0		4,66E-15	2	0	1,00E-05	0
10/266						IS	1		2,0E+05			0		4,66E-15	3	0	1,50E-05	0
Σ		**40Ar12+**	**10,1**						**8,0E+05**	**8,1E+03**		**2**		**2,33E-15**	**15**	**1**	**2,00E-05**	**4**
10/357	348	82Kr22+	32,1	M2a	Elp1t	none	10	124	4,0E+04	3,2E+02	1,89E+03	3		6,98E-14	3	0	7,50E-05	0
10/358						none	1		4,0E+04			0		2,33E-14	0	0	2,50E-05	0
10/359						IS	1		4,0E+04			1		2,33E-14	0	0	2,50E-05	0
Σ		**82Kr22+**	**32,1**						**4,0E+04**	**3,2E+02**		**3**		**6,98E-14**	**3**	**0**	**7,50E-05**	**0**
10/399	362	131Xe35+	60	M2a	Elp1t	none	8	107	1,0E+05	9,3E+02	3,72E+03	55		5,12E-13	0	0	1,00E-05	0
10/400						none			1,0E+05			0		9,31E-15	0	0	1,00E-05	0
10/401						IS	1		1,0E+05			14		1,30E-13	0	0	1,00E-05	0
Σ		**131Xe35+**	**60**						**1,0E+05**	**9,3E+02**		**55**		**5,12E-13**	**0**	**0**	**1,00E-05**	**0**

Elpida EDE2108ABSE-8G-E DDR2-SDRAM, Mode M2b

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initiali-sation	Loops	Time	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
10/425	370	20Ne6+	3,6	M2b	Elp1t	RAIS1, WAIS1	9	108	2,0E+06	1,9E+04	4,50E+03	12		5,59E-15	0	0	5,00E-07	0
10/426						IS	1		2,0E+06			1		4,66E-16	0	0	5,00E-07	0
Σ		**20Ne6+**	**3,6**						**2,0E+06**	**1,9E+04**		**12**		**5,59E-15**	**0**	**0**	**5,00E-07**	**0**
10/15	7	40Ar12+	10,1	M2b	Elp1t	RAIS1, WAIS1	8	96	2,0E+05	2,1E+03	1,94E+02	3		1,40E-14	0	0	5,00E-06	0
10/16						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/212	61	40Ar12+	10,1	M2b	Elp1t	RAIS1	9	109	2,0E+05	1,8E+03	7,11E+02	3		1,40E-14	0	0	5,00E-06	0
10/213						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/215	62	40Ar12+	10,1	M2b	Elp1t	RAIS1	9	108	2,0E+05	1,9E+03	7,43E+02	4		1,86E-14	2	0	1,00E-05	0
10/216						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/218	63	40Ar12+	10,1	M2b	Elp1t	RAIS_0x2000	9	107	2,0E+05	1,9E+03	7,76E+02	1		4,66E-15	1	0	5,00E-06	0
10/219						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/225	65	40Ar12+	10,1	M2b	Elp1t	RAIS_0x1000	9	111	2,0E+05	1,8E+03	8,40E+02	2		9,31E-15	0	0	5,00E-06	0
10/226						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/228	66	40Ar12+	10,1	M2b	Elp1t	RAIS_0x800	9	111	2,0E+05	1,8E+03	8,73E+02	0		4,66E-15	0	0	5,00E-06	1
10/229						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	1
10/231	67	40Ar12+	10,1	M2b	Elp1t	RAIS_0x400	9	110	2,0E+05	1,8E+03	9,05E+02	0		4,66E-15	0	0	5,00E-06	1
10/232						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	1
10/234	68	40Ar12+	10,1	M2b	Elp1t	RAIS_0x200	9	109	2,0E+05	1,8E+03	9,37E+02	1		4,66E-15	0	0	5,00E-06	0
10/235						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/237	69	40Ar12+	10,1	M2b	Elp1t	RAIS_0x100	9	110	2,0E+05	1,8E+03	9,70E+02	2		9,31E-15	0	0	5,00E-06	0
10/238						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/240	70	40Ar12+	10,1	M2b	Elp1t	RAIS_0x80	9	103	2,0E+05	1,9E+03	1,00E+03	3		1,40E-14	0	0	5,00E-06	0
10/241						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/243	71	40Ar12+	10,1	M2b	Elp1t	RAIS_0x40	9	108	2,0E+05	1,9E+03	1,03E+03	2		9,31E-15	0	0	5,00E-06	0
10/244						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/246	72	40Ar12+	10,1	M2b	Elp1t	RAIS_0x20	9	109	2,0E+05	1,8E+03	1,07E+03	0		4,66E-15	0	0	5,00E-06	0
10/247						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/249	73	40Ar12+	10,1	M2b	Elp1t	RAIS_0x10	8	101	2,0E+05	2,0E+03	1,10E+03	3		1,40E-14	0	0	5,00E-06	0
10/250						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/252	74	40Ar12+	10,1	M2b	Elp1t	RAIS_0x8	9	102	2,0E+05	2,0E+03	1,13E+03	4		1,86E-14	2	0	1,00E-05	0
10/253						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/255	75	40Ar12+	10,1	M2b	Elp1t	RAIS_0x4	9	104	2,0E+05	1,9E+03	1,16E+03	3		1,40E-14	9	0	4,50E-05	0
10/256						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/258	76	40Ar12+	10,1	M2b	Elp1t	RAIS_0x2	8	101	2,0E+05	2,0E+03	1,20E+03	2		9,31E-15	0	0	5,00E-06	0
10/259						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
10/261	77	40Ar12+	10,1	M2b	Elp1t	RAIS_0x1	8	96	2,0E+05	2,1E+03	1,23E+03	5		2,33E-14	0	0	5,00E-06	0
10/262						IS	1		2,0E+05			0		4,66E-15	0	0	5,00E-06	0
Σ		**40Ar12+**	**10,1**						**3,0E+06**	**2,9E+04**		**38**		**1,18E-14**	**14**	**0**	**4,67E-06**	**2**
10/334	340	56Fe15+	18,5	M2b	Elp1t	RAIS1, WAIS1	9	107	2,0E+05	1,9E+03	1,67E+03	11		5,12E-14	1	0	5,00E-06	0
10/335						IS	1		2,00E+05			0		4,66E-15	0	0	5,00E-06	0
10/340	342	56Fe15+	18,5	M2b	Elp1t	RAIS1, WAIS1	9	105	2,00E+05	1,9E+03	1,78E+03	11		5,12E-14	4	0	2,00E-05	0
10/341						IS	1		2,00E+05			0		4,66E-15	0	0	5,00E-06	0
Σ		**56Fe15+**	**18,5**						**4,00E+05**	**3,8E+03**		**22**		**5,12E-14**	**5**	**0**	**1,25E-05**	**0**
10/361	349	82Kr22+	32,1	M2b	Elp1t	RAIS1, WAIS1	5	114	4,00E+04	3,5E+02	1,91E+03	5		1,16E-13	0	0	2,50E-05	0
10/362						IS	1		4,00E+04			0		2,33E-14	0	0	2,50E-05	0
10/370	352	82Kr22+	32,1	M2b	Elp1t	RAIS1, WAIS1	8	96	4,00E+05	4,2E+03	2,52E+03	3		6,98E-15	5	0	1,25E-05	0
10/371						IS	1		4,00E+05			2		4,66E-15	0	0	2,50E-06	0
10/379	355	82Kr22+	32,1	M2b	Elp1t	RAIS1, WAIS1	8	93	4,00E+05	4,3E+03	3,14E+03	46		1,07E-13	13	0	3,25E-05	0
10/380						IS	1		4,00E+05			0		2,33E-15	0	0	2,50E-06	0
Σ		**82Kr22+**	**32,1**						**8,40E+05**	**8,8E+03**		**54**		**5,99E-14**	**18**	**0**	**2,14E-05**	**0**
10/403	363	131Xe35+	60	M2b	Elp1t	RAIS1, WAIS1	7	90	1,00E+05	1,1E+03	3,81E+03	69		6,43E-13	2	0	2,00E-05	0
10/404						IS	1		1,00E+05			15		1,40E-13	0	0	1,00E-05	0
Σ		**131Xe35+**	**60**						**1,00E+05**	**1,1E+03**		**69**		**6,43E-13**	**2**	**0**	**2,00E-05**	**0**

Elpida EDE2108ABSE-8G-E DDR2-SDRAM, Mode M3a

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initiali-sation	Loops	Time	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
10/299	331	15N4+	1,8	M3a	Elp1t	none	1	235	2,0E+05	8,5E+02	1,30E+03	5		2,33E-14	3	0	1,50E-05	0
10/300						none	1		2,0E+05			5		2,33E-14	3	0	1,50E-05	0
10/301						IS	1		2,0E+05			192		8,94E-13	2	0	1,00E-05	0
Σ		**15N4+**	**1,8**						**2,0E+05**	**8,5E+02**		**5**		**2,33E-14**	**3**	**0**	**1,50E-05**	**0**
10/406	365	20Ne6+	3,6	M3a	Elp1t	none	1	110	2,0E+06	1,8E+04	3,93E+03	16		7,45E-15	13	0	6,50E-06	0
10/407						none	1		2,0E+06			2		9,31E-16	12	0	6,00E-06	0
10/408						IS	1		2,0E+06			288		1,34E-13	0	0	5,00E-07	0
10/409						IS	1		2,0E+06			288		1,34E-13	0	0	5,00E-07	0
10/428	371	20Ne6+	3,6	M3a	Elp1t	none	1	106	2,0E+06	1,9E+04	4,62E+03			4,66E-16			5,00E-07	1
10/429						none	1		2,0E+06					4,66E-16			5,00E-07	1
10/430						IS	1		2,0E+06			8		3,73E-15	0	0	5,00E-07	0
10/438	374	20Ne6+	3,6	M3a	Elp1t	none	1	179	2,0E+07	1,1E+05	6,00E+03			4,66E-17			5,00E-08	1
10/439						none	1		2,0E+07					4,66E-17			5,00E-08	1
10/440						IS	1		2,0E+07			199		9,27E-15	0	0	5,00E-08	0
10/441						IS	1		2,0E+07			199		9,27E-15	0	0	5,00E-08	0
Σ		**20Ne6+**	**3,6**						**2,0E+06**	**1,8E+04**		**16**		**7,45E-15**	**13**	**0**	**6,50E-06**	**2**
10/2	2	40Ar12+	10,1	M3a	Elp1t	none	1	120	2,0E+05	1,7E+03	3,23E+01	0		4,66E-15	6	0	3,00E-05	0
10/18	8	40Ar12+	10,1	M3a	Elp1t	none	1	85	2,0E+05	2,4E+03	2,26E+02	1		4,66E-15	6	0	3,00E-05	0
10/19						IS	1		2,0E+05			331		1,54E-12	0	0	5,00E-06	0
10/20						IS	1		2,0E+05			331		1,54E-12	0	0	5,00E-06	0
10/21						IL	1		2,0E+05			331		1,54E-12	0	0	5,00E-06	0
Σ		**40Ar12+**	**10,1**						**4,0E+05**	**4,0E+03**		**1**		**2,33E-15**	**12**	**0**	**3,00E-05**	**0**
10/316	335	56Fe15+	18,5	M3a	Elp1t	none	1	89	2,0E+05	2,2E+03	1,37E+03	36		1,68E-13	5	0	2,50E-05	0
10/317						none	1		2,0E+05			36		1,68E-13	5	0	2,50E-05	0
10/318						IS	1		2,0E+05			386		1,80E-12	0	0	5,00E-06	0
Σ		**56Fe15+**	**18,5**						**2,0E+05**	**2,2E+03**		**36**		**1,68E-13**	**5**	**0**	**2,50E-05**	**0**
10/343	344	82Kr22+	32,1	M3a	Elp1t	none	1	160	4,0E+04	2,5E+02	1,80E+03	5		1,16E-13	3	0	7,50E-05	0
10/344						none	1		4,0E+04			5		1,16E-13	3	0	7,50E-05	0
10/345						IS	1		4,0E+04			197		4,59E-12	0	0	2,50E-05	0
Σ		**82Kr22+**	**32,1**						**4,0E+04**	**2,5E+02**		**5**		**1,16E-13**	**3**	**0**	**7,50E-05**	**0**
10/382	357	131Xe35+	60	M3a	Elp1t	none	1	103	1,0E+05	9,7E+02	3,24E+03			9,31E-15			1,00E-05	1
10/383						none	1		1,0E+05					9,31E-15			1,00E-05	1
10/384						IS	1		1,0E+05					9,31E-15			1,00E-05	1
Σ		**131Xe35+**	**60**						**1,0E+05**	**9,7E+02**				**9,31E-15**			**1,00E-05**	**1**

Elpida EDE2108ABSE-8G-E DDR2-SDRAM, Mode M3b

Run IDA	Run RADEF	Ion	LET	Mode	DUT	Initiali-sation	Loops	Time	Fluence	Flux	Dose	SEU sta.	SEU dyn.	σSEU, bit static	Class B Row Err.	Class B Col Err.	ClassB σSEFI, dev	Class C SEFI
10/411	366	20Ne6+	3,6	M3b	Elp1t	1000	1	112	2,0E+06	1,8E+04	4,04E+03	1		4,66E-16	0	0	5,00E-07	0
10/412						IS	1		2,0E+06			1		4,66E-16	0	0	5,00E-07	0
10/432	372	20Ne6+	3,6	M3b	Elp1t	1000	1	125	2,0E+06	1,6E+04	4,73E+03	7		3,26E-15	0	0	5,00E-07	0
10/433						IS	1		2,0E+06			7		3,26E-15	0	0	5,00E-07	0
10/435	373	20Ne6+	3,6	M3b	Elp1t	1000	1	107	2,0E+06	1,9E+04	4,85E+03	1		4,66E-16	0	0	5,00E-07	0
10/436						IS	1		2,0E+06			1		4,66E-16	0	0	5,00E-07	0
10/443	375	20Ne6+	3,6	M3b	Elp1t	1000	1	186	2,0E+07	1,1E+05	7,15E+03	39		1,82E-15	3	0	1,50E-07	0
10/444						IS	1		2,0E+07			39		1,82E-15	3	0	1,50E-07	0
10/446	376	20Ne6+	3,6	M3b	Elp1t	30000	1	204	2,0E+07	9,8E+04	8,30E+03			4,66E-17			5,00E-08	1
10/447						IS	1		2,0E+07					4,66E-17			5,00E-08	1
10/449	377	20Ne6+	3,6	M3b	Elp1t	20000	1	191	2,0E+07	1,0E+05	9,46E+03			4,66E-17			5,00E-08	1
10/450						IS	1		2,0E+07					4,66E-17			5,00E-08	1
10/452	378	20Ne6+	3,6	M3b	Elp1t	12000	1	198	2,0E+07	1,0E+05	1,06E+03	33		1,54E-15	13	0	6,50E-07	0
10/453						IS	1		2,0E+07			58		2,70E-15	6	0	3,00E-07	0
Σ		**20Ne6+**	**3,6**						**4,6E+07**	**2,6E+05**		**81**		**1,64E-15**	**16**	**0**	**3,48E-07**	**2**
10/4	3	40Ar12+	10,1	M3b	Elp1t	1000	1	99	2,0E+05	2,0E+03	6,46E+01	1		4,66E-15	0	0	5,00E-06	0
10/23	9	40Ar12+	10,1	M3b	Elp1t	1000	1	93	2,0E+05	2,2E+03	2,59E+02	1		4,66E-15	0	0	5,00E-06	0
10/186	53	40Ar12+	10,1	M3b	Elp1t	1000	1	91	2,0E+05	2,2E+03	4,52E+02	0		4,66E-15	0	0	5,00E-06	0
Σ		**40Ar12+**	**10,1**						**6,0E+05**	**6,4E+03**		**2**		**3,10E-15**	**0**	**0**	**1,67E-06**	**0**
10/320	336	56Fe15+	18,5	M3b	Elp1t	1000	1	105	2,0E+05	1,9E+03	1,43E+03	5		2,33E-14	0	0	5,00E-06	0
10/321						IS	1		2,0E+05			5		2,33E-14	0	0	5,00E-06	0
Σ		**56Fe15+**	**18,5**						**2,0E+05**	**1,9E+03**		**5**		**2,33E-14**	**0**	**0**	**5,00E-06**	**0**
10/347	345	82Kr22+	32,1	M3b	Elp1t	1000	1	114	4,0E+04	3,5E+02	1,82E+03	1		2,33E-14	0	0	2,50E-05	0
10/348						IS	1		4,0E+04			1		2,33E-14	0	0	2,50E-05	0
10/364	350	82Kr22+	32,1	M3b	Elp1t	1000	1	92	4,0E+05	4,3E+03	2,11E+03	41		9,55E-14	0	0	2,50E-06	0
10/365						IS	1		4,0E+05			41		9,55E-14	0	0	2,50E-06	0
10/373	353	82Kr22+	32,1	M3b	Elp1t	1000	1	89	4,0E+05	4,5E+03	2,73E+03	87		2,03E-13	0	0	2,50E-06	0
10/374						IS	1		4,0E+05			87		2,03E-13	0	0	2,50E-06	0
Σ		**82Kr22+**	**32,1**						**8,4E+05**	**9,2E+03**		**129**		**1,43E-13**	**0**	**0**	**1,19E-06**	**0**
10/386	358	131Xe35+	60	M3b	Elp1t	1000	1	100	1,0E+05	1,0E+03	3,97E+02	64		5,96E-13	0	0	1,00E-05	0
10/387						IS	1		1,0E+05			64		5,96E-13	0	0	1,00E-05	0
Σ		**131Xe35+**	**60**						**1,0E+05**	**1,0E+03**		**64**		**5,96E-13**	**0**	**0**	**1,00E-05**	**0**

9. Reference

[1] A Virtanen et al., “Upgrades for the RADEF Facility”, 2007 IEEE Radiation Effects Data Workshop Record, pp. 38-41
[2] R. Koga et al., “Proton and Heavy Ion Induced Semi-Permanent Upsets in Double Data rate SDRAMs”, IEEE Radiation Effects Data Workshop 2007, pp. 199-203
[3] R. Harboe Sorensen et al., “Heavy-Ion SEE Test Concept and Results for DDR-II Memo ries”, IEE Trans. Nucl. Sci., vol.54, no 6, pp 2125-2130, Dec. 2007
[4] H. Schmidt et al., “SEE and TID Acceptance Test of the Radiation Test-Bed for High Ca pacity Memory Components”, QCA Final Presentation Day, ESTEC, ESA, May 2005, https://escies.org./GetFile?rscid=1

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