



Customer-Oriented Product Engineering of Micro and Nano Devices

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# Efficient Virtual Manufacturing for MNT

**Gerold Schröpfer, Coventor**

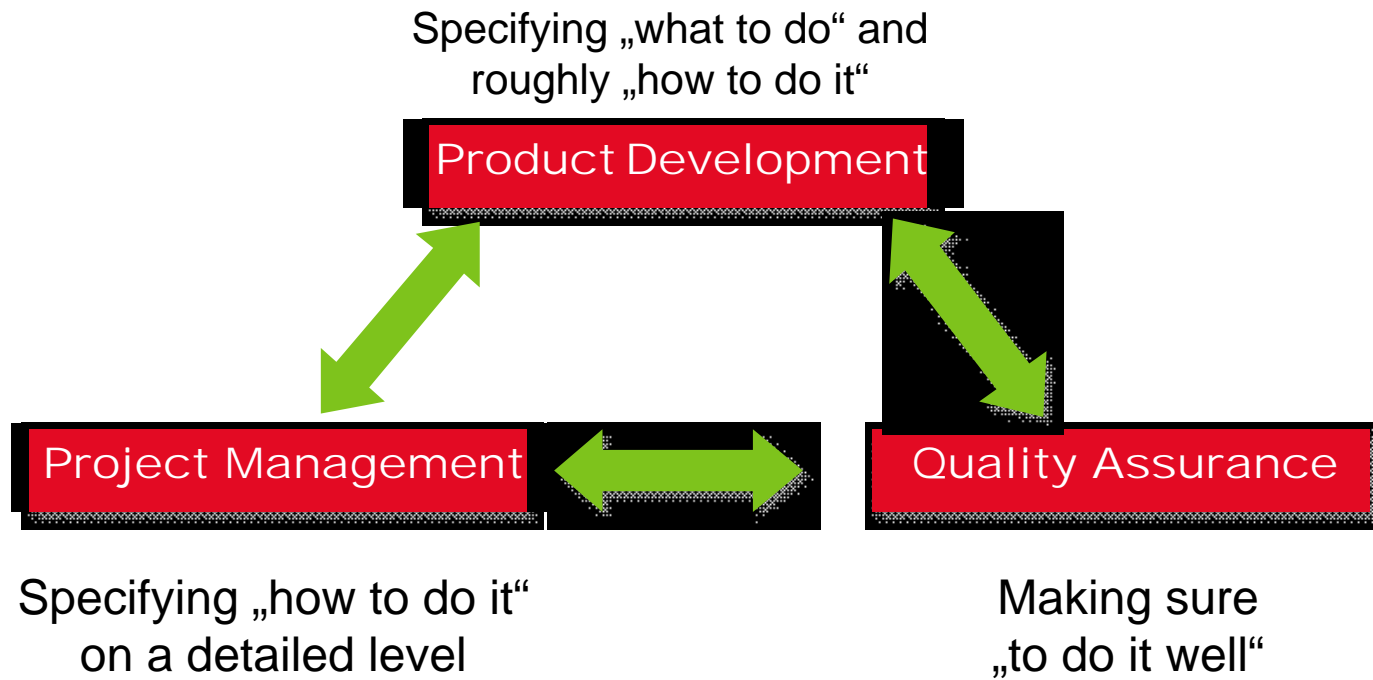
September 2010, 7th ESA Round-Table on MNT for Space Applications





- **CORONA project**
  - Vision and aims
- **CORONA software tools**
  - Process IP and know-how management
  - 3D MNT design
  - Virtual Manufacturing
  - Process design kits

- ... is the process of gradually turning the idea of a technical device into a physical realisation.
- ... includes both the design and the fabrication stages.

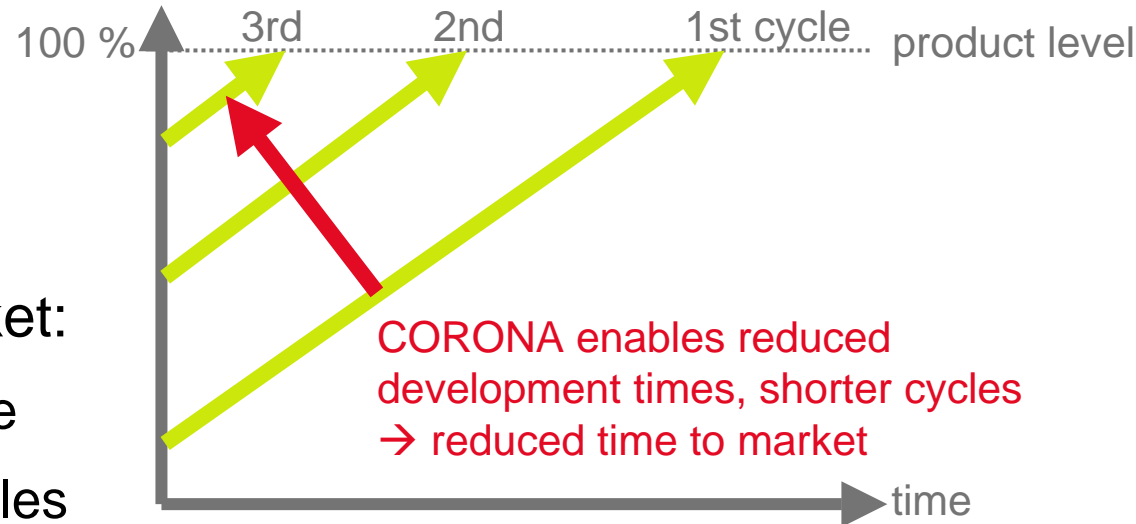




- **A large variety of business models**
    - From large IDMs to specialised companies
  - **Distributed development and manufacturing**
    - Different companies (or departments) at different locations
  - **SME focus**
    - Frequently SMEs involved with small development budget
  - **Customer orientation**
    - Only the customer knows product and constraints
- **But...**
    - There is currently no appropriate product engineering methodology and tools available to support these aspects.

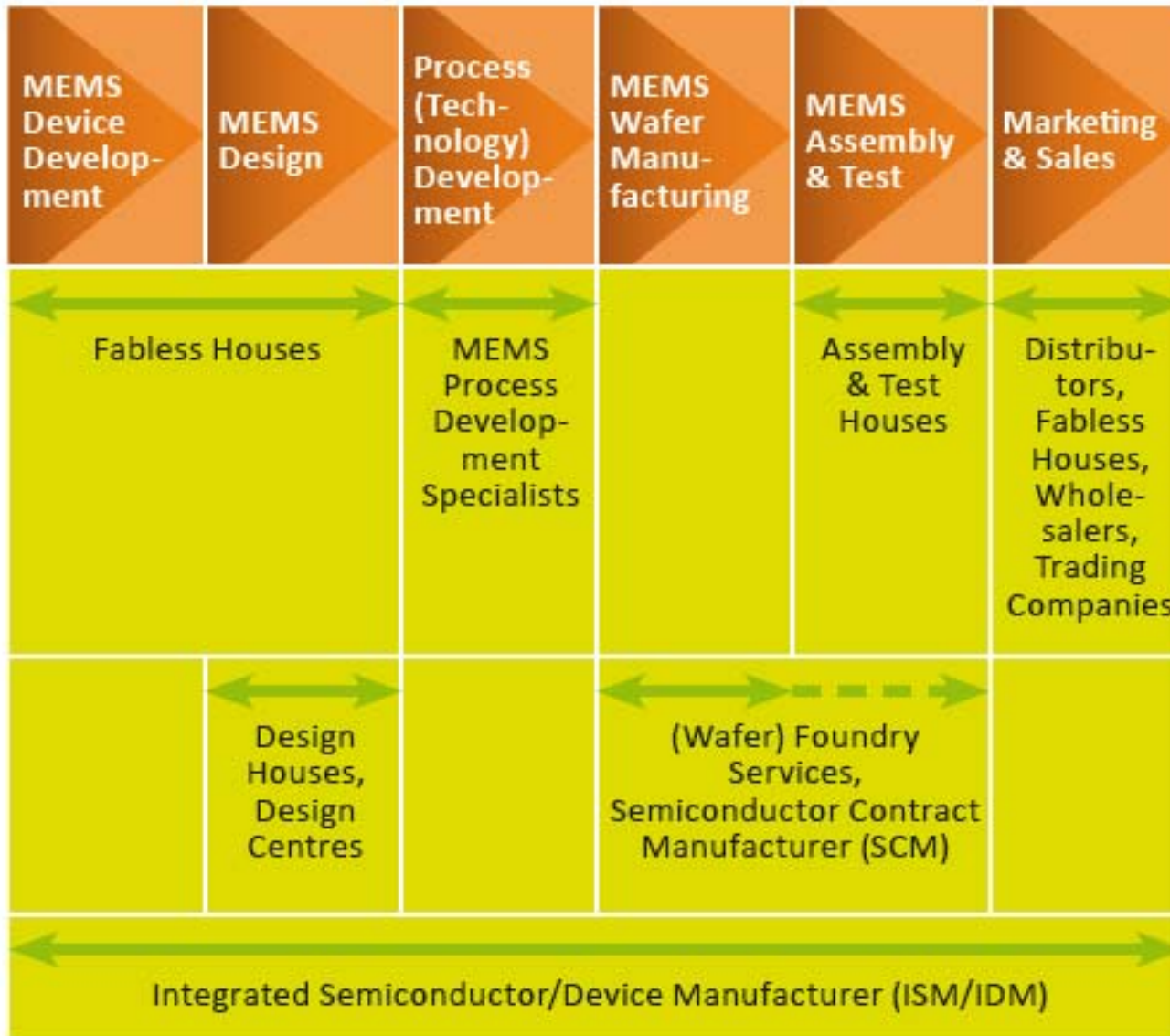
## ■ What can be expected from MNT product engineering?

- Shorter time-to-market:
  - Reduced cycle time
  - Fewer learning cycles



- Access to knowledge-bases on design and fabrication
  - ICT based structure and tools
  - Improved transfer of knowledge from design to production
- Customer-lead multi-site product development

# Value chain in MNT



# Partners



## CORONA:

- NMP Project CP-FP 213969-2
- 11 Partners all along the MNT Value Chain
- Project Duration: 01/07/2008 – 30/06/2011
- Budget: 4.36 Million €

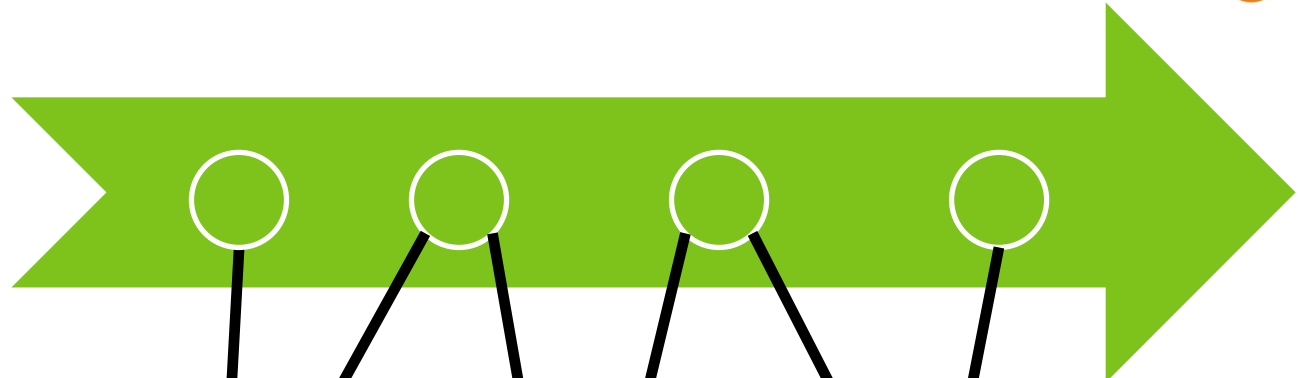


# Workflow in CORONA

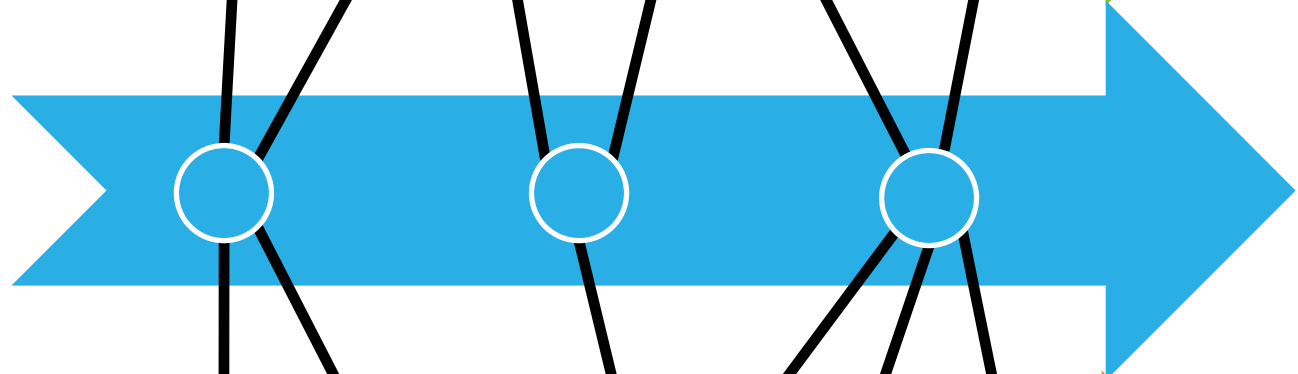
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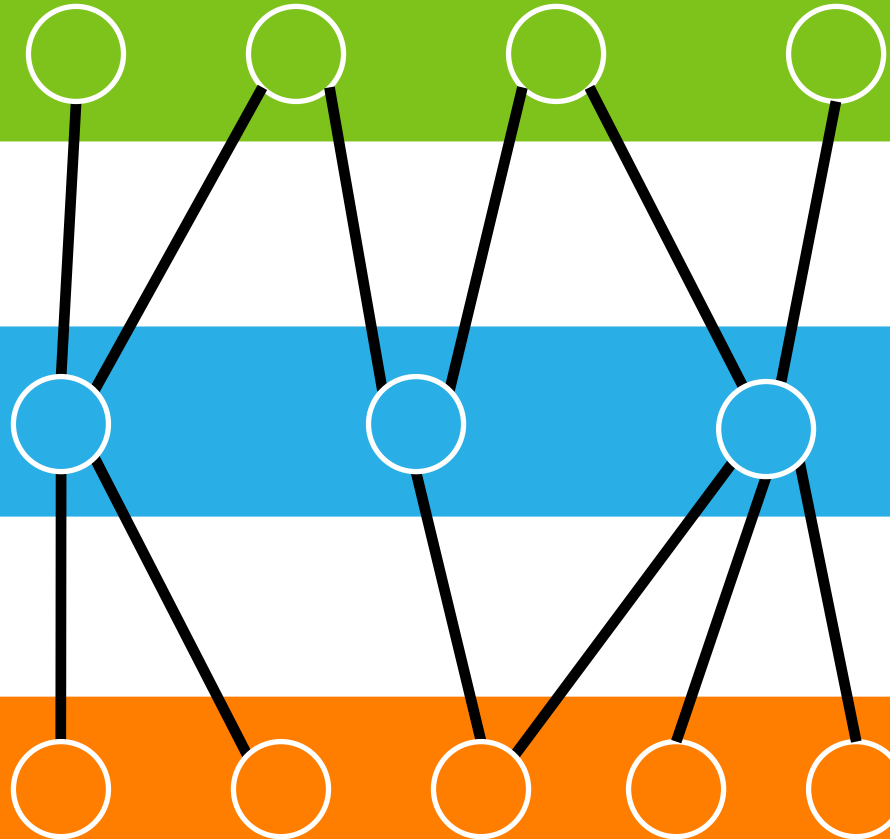
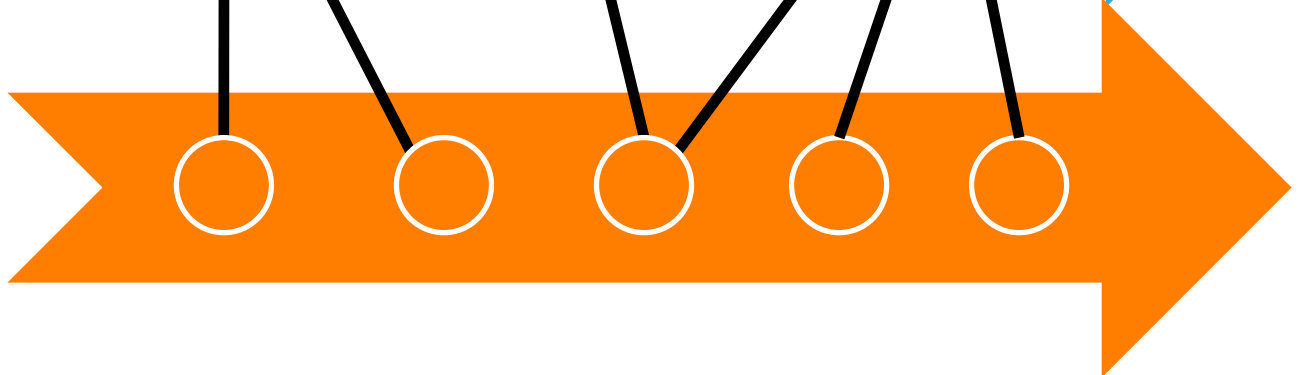
**Methodology**  
Workflow Definition



**Middle Ware & Tools**  
Workflow/Designflow Integration



**Validation**  
by real-life business cases



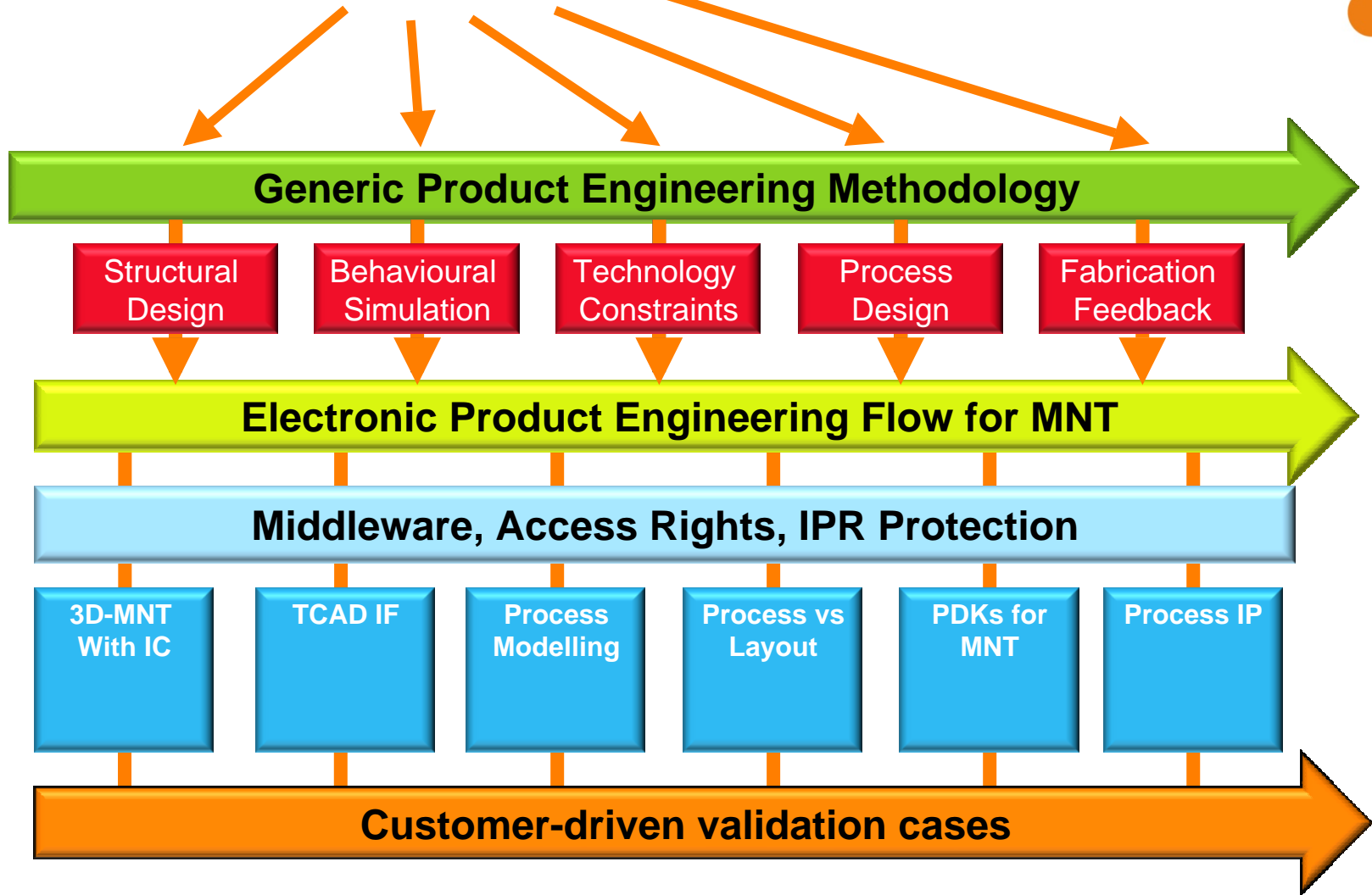


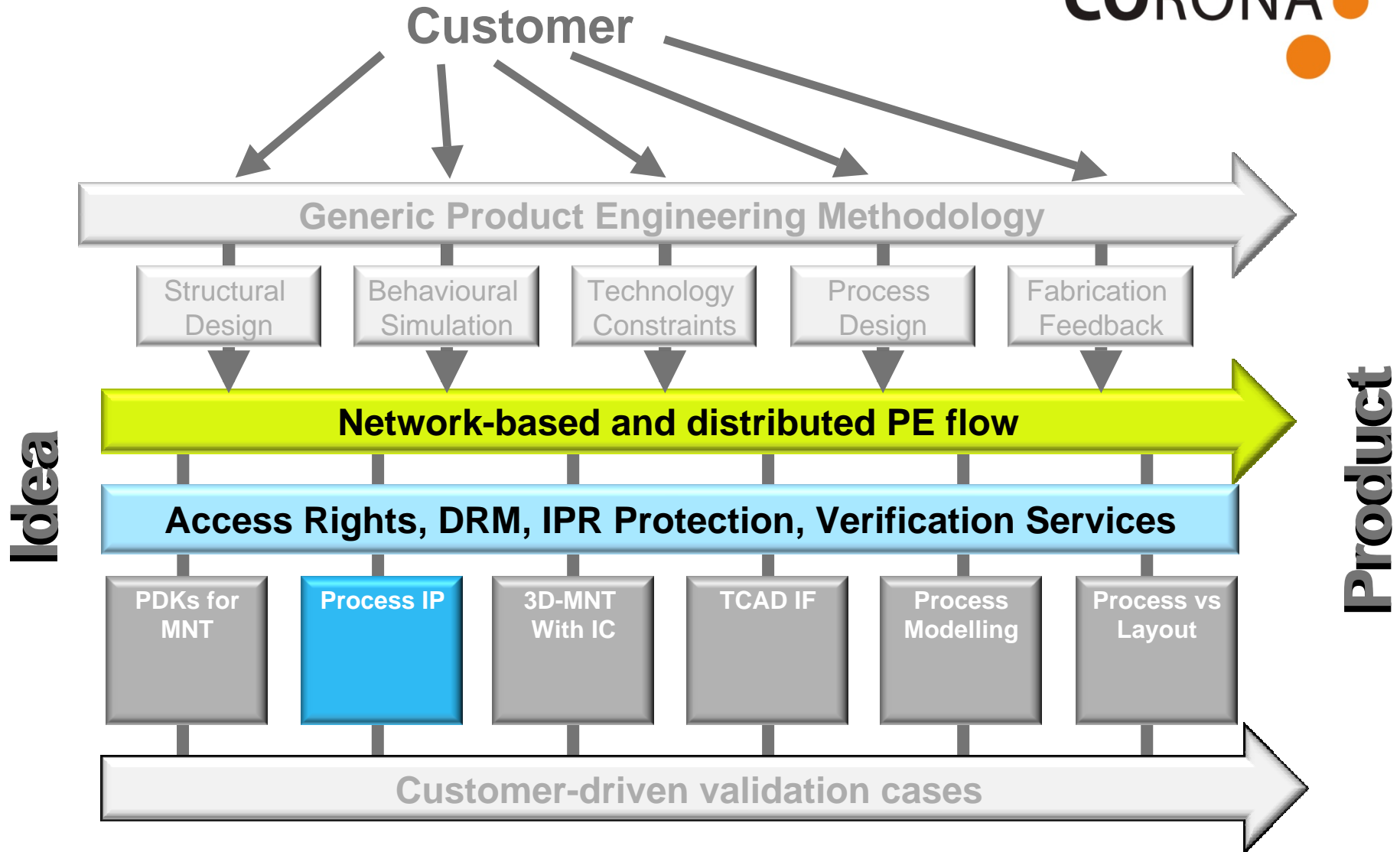


**Customer**

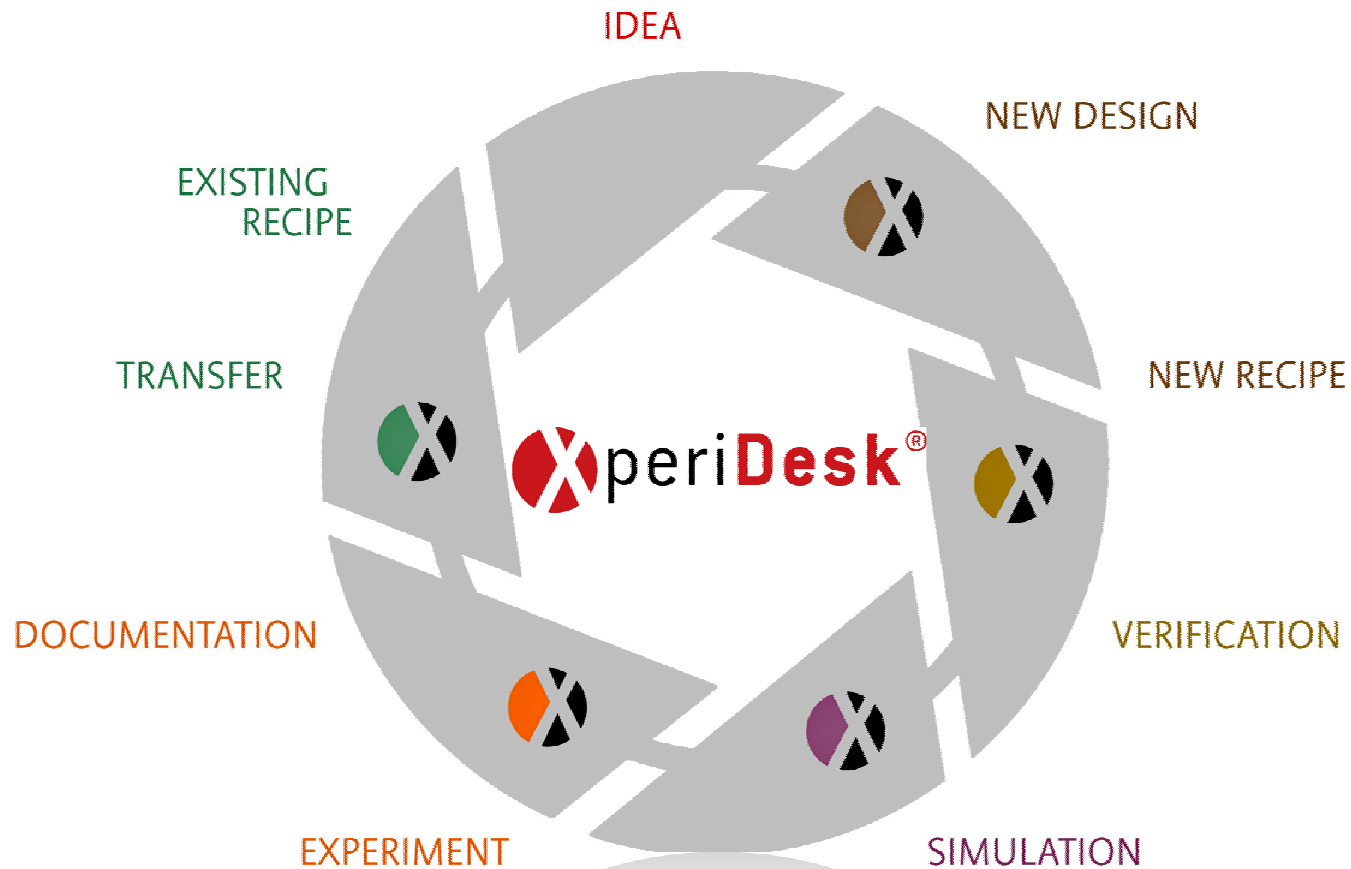
**Idea**

**Product**

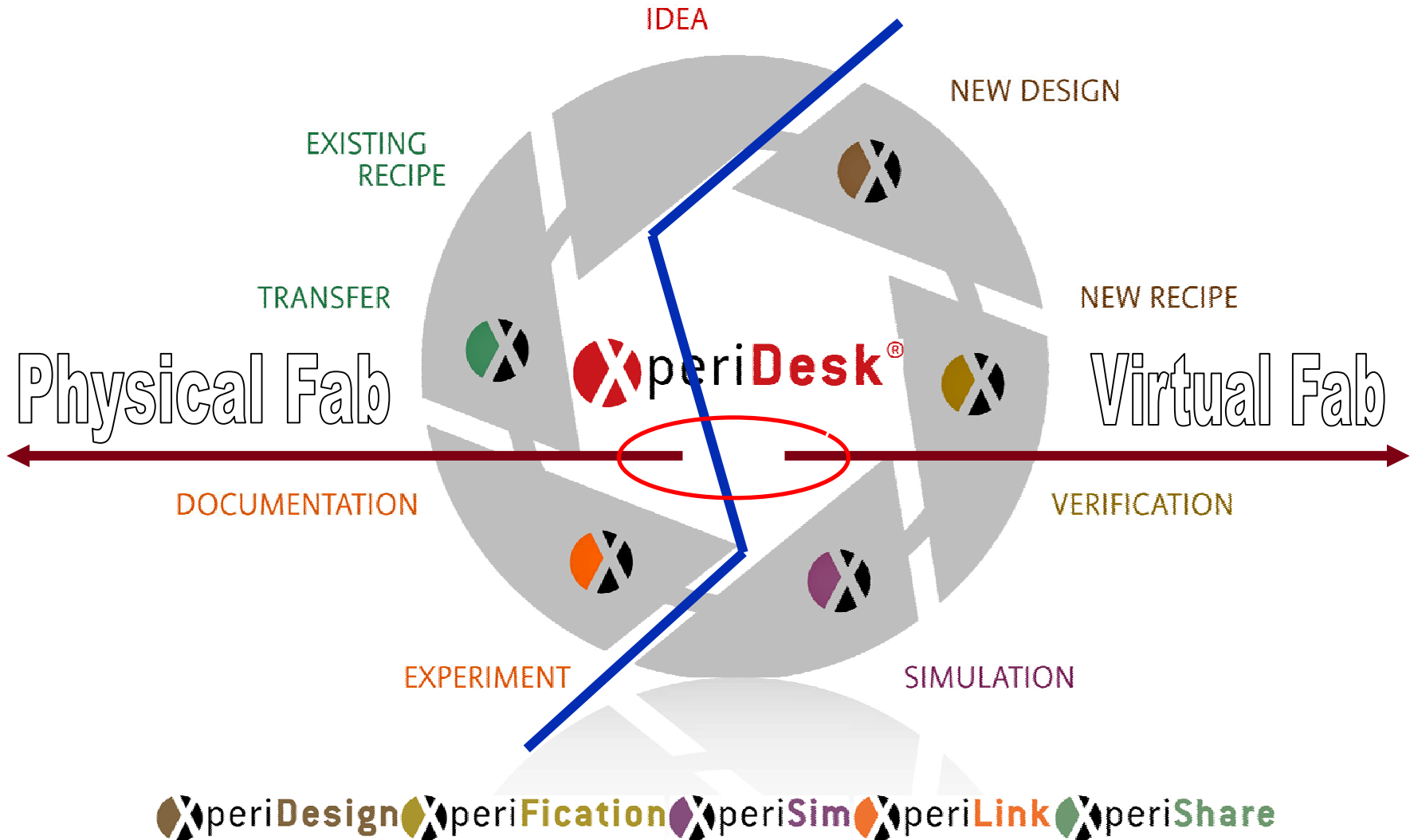




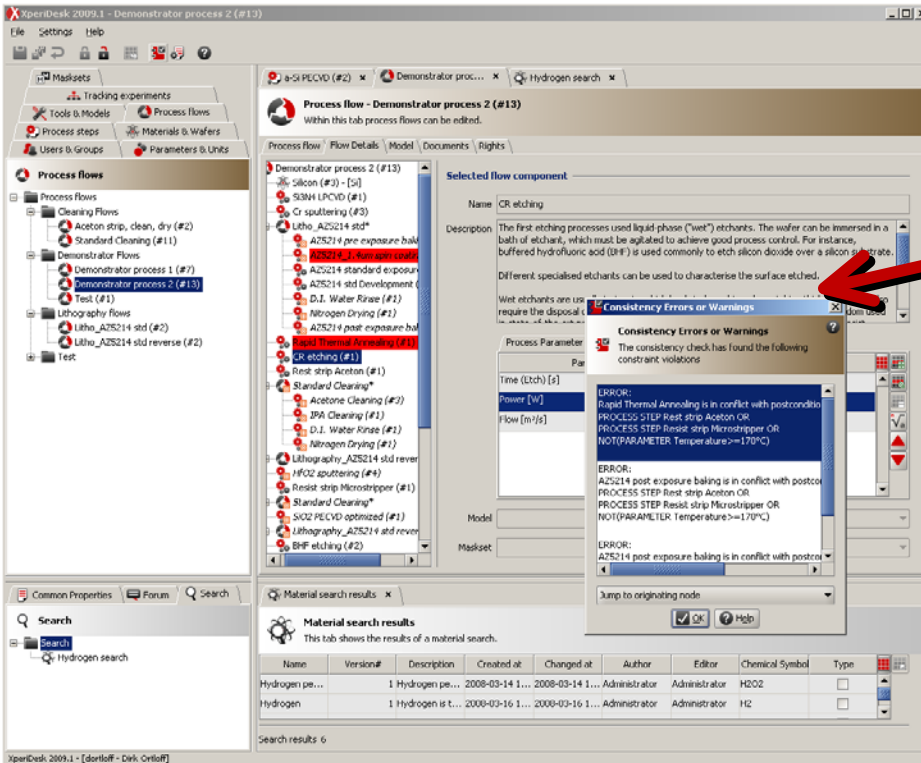
# Process development cycle



# Physical and Virtual Fab

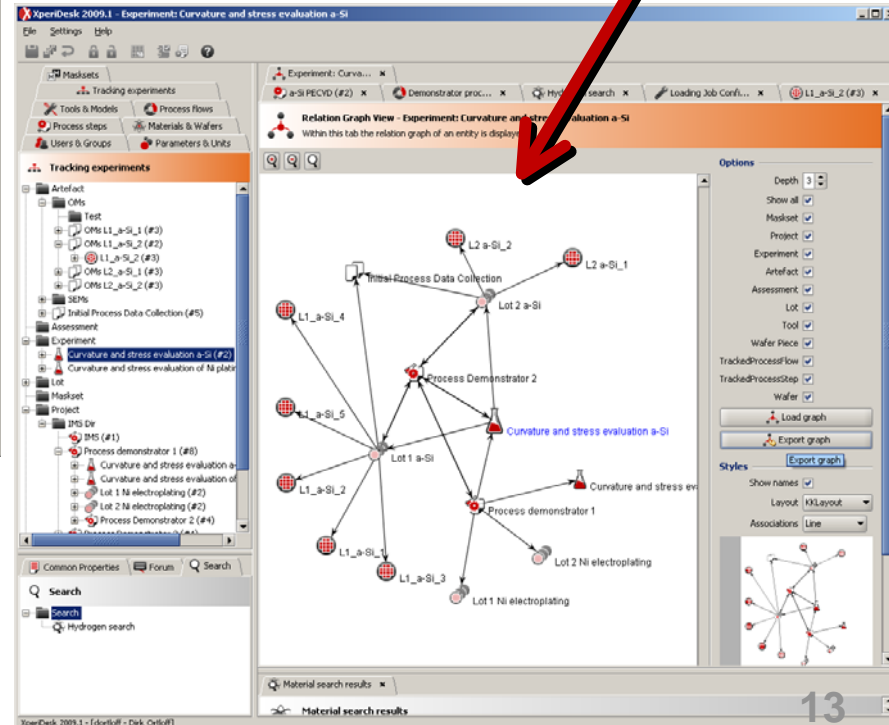


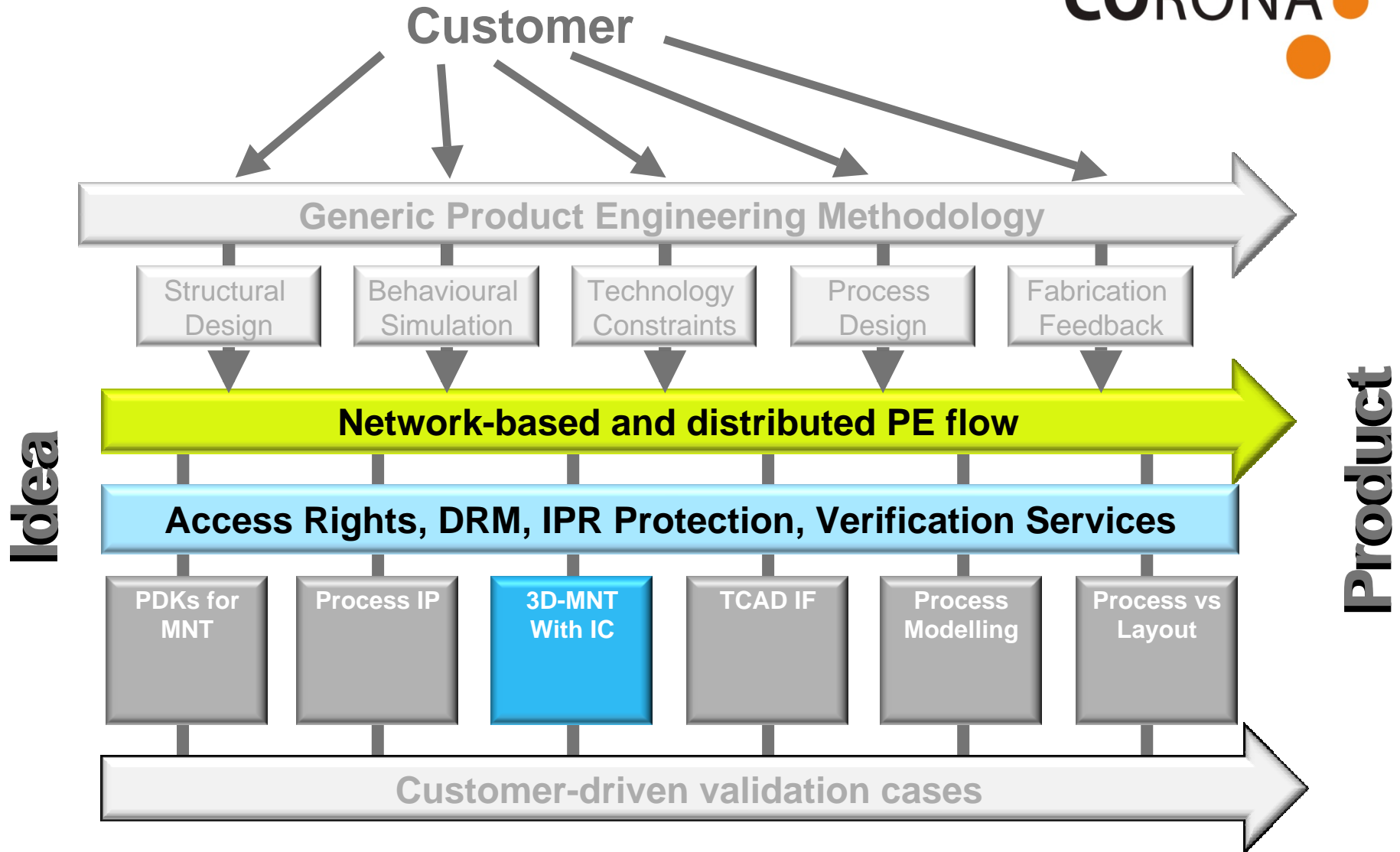
- A framework for process design verification and tracking



Process Flow Editor

Process Tracking



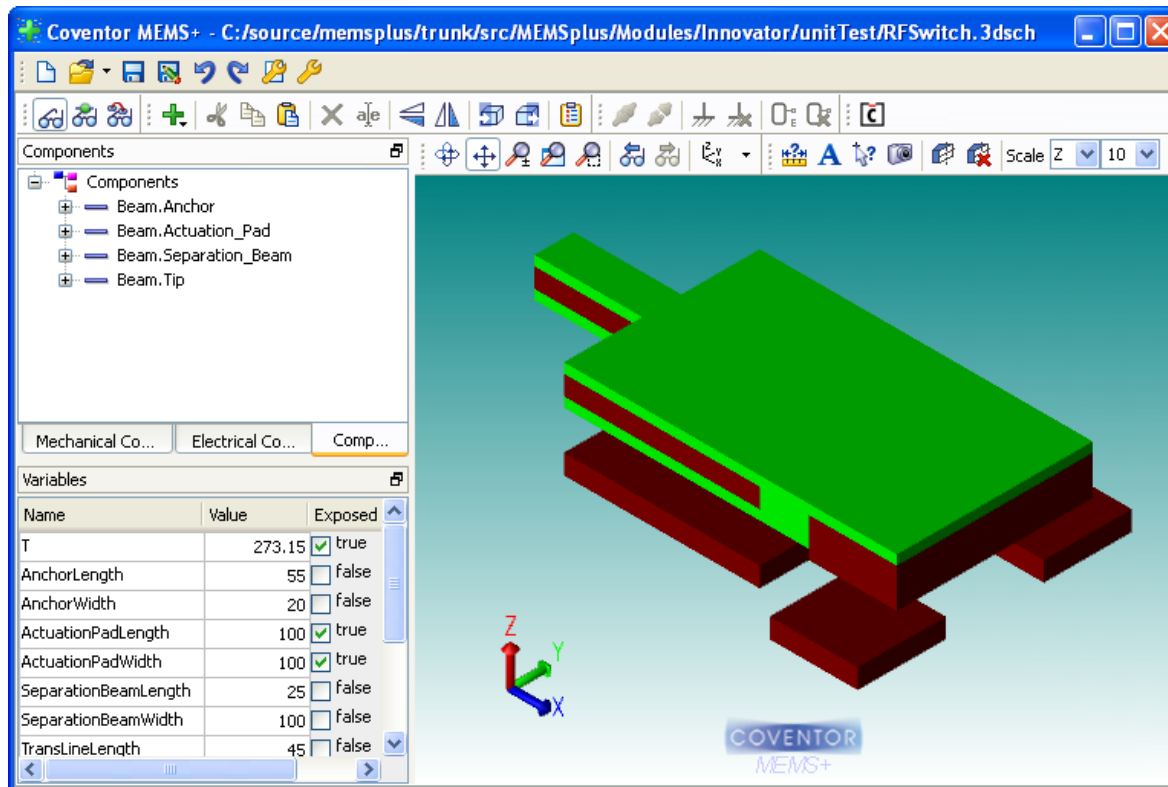


# 3D Schematic Editor for MEMS

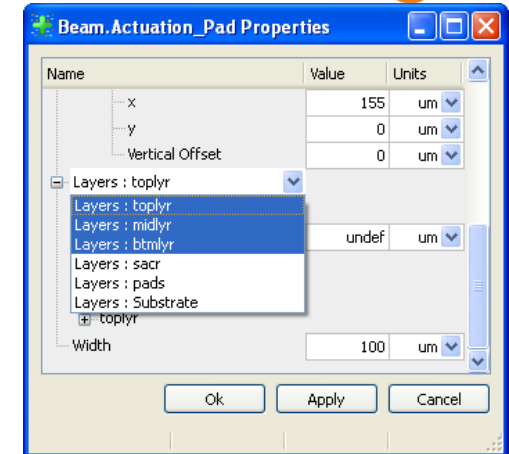


## MEMS Design in 3D

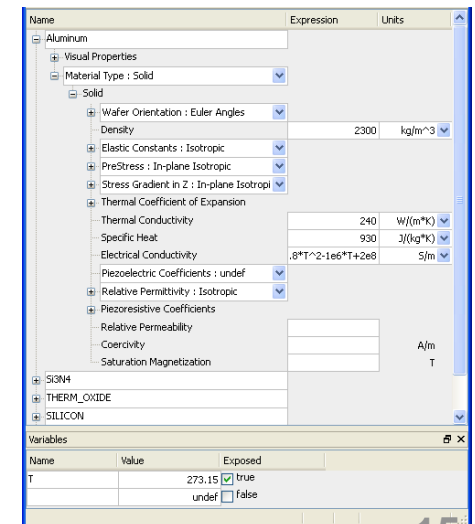
- Intuitive 3D environment for device creation
- Based on validated MEMS component library
- Parameterization of material, process and design



3-D view of RF switch in new 3D schematic Editor GUI (Graphical User Interface)



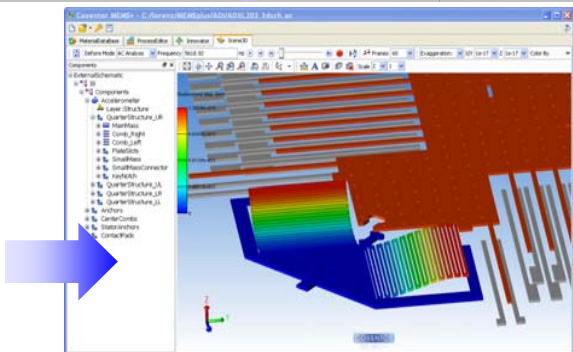
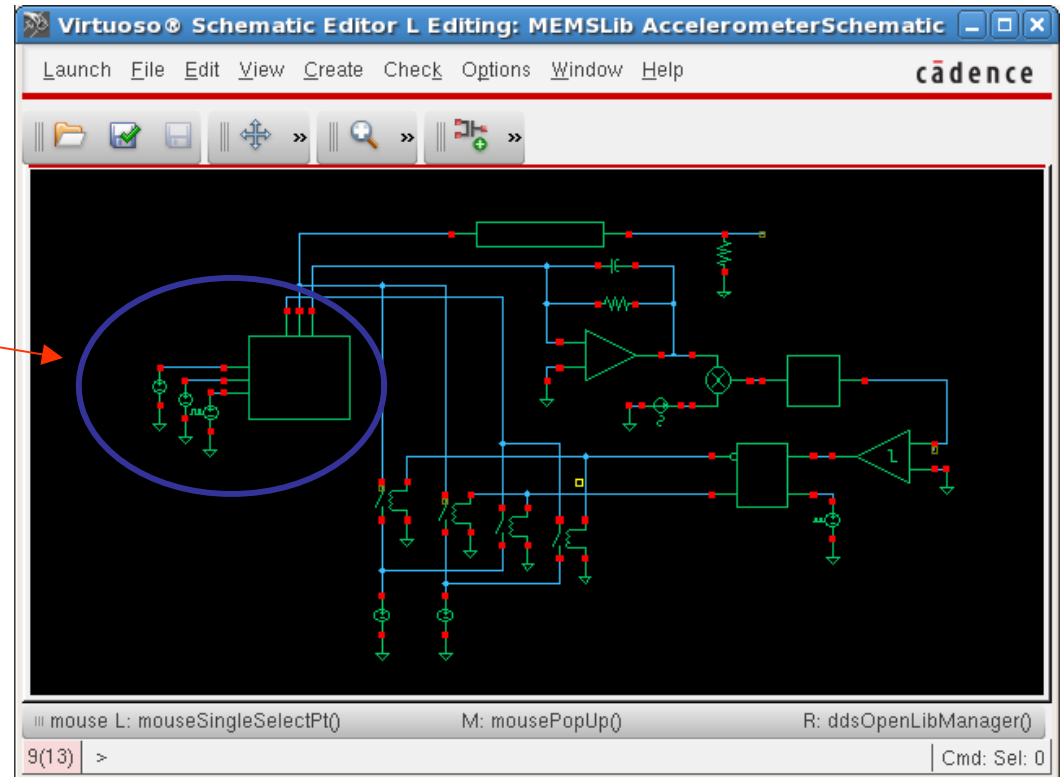
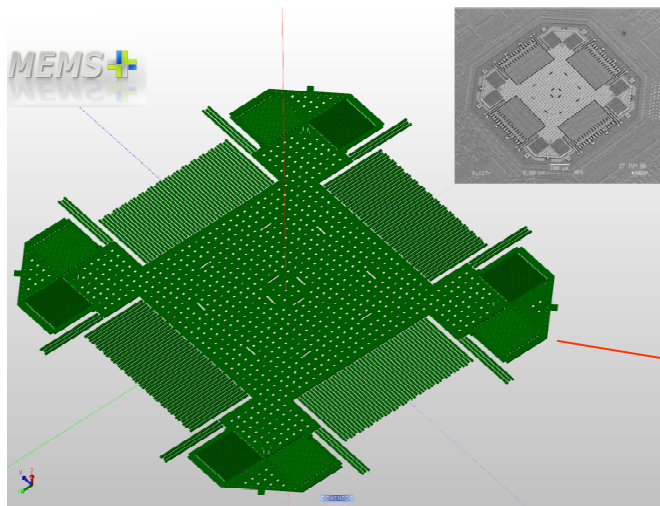
Layer Browser in a Property Window of a Straight Beam Component



Material Property Editor

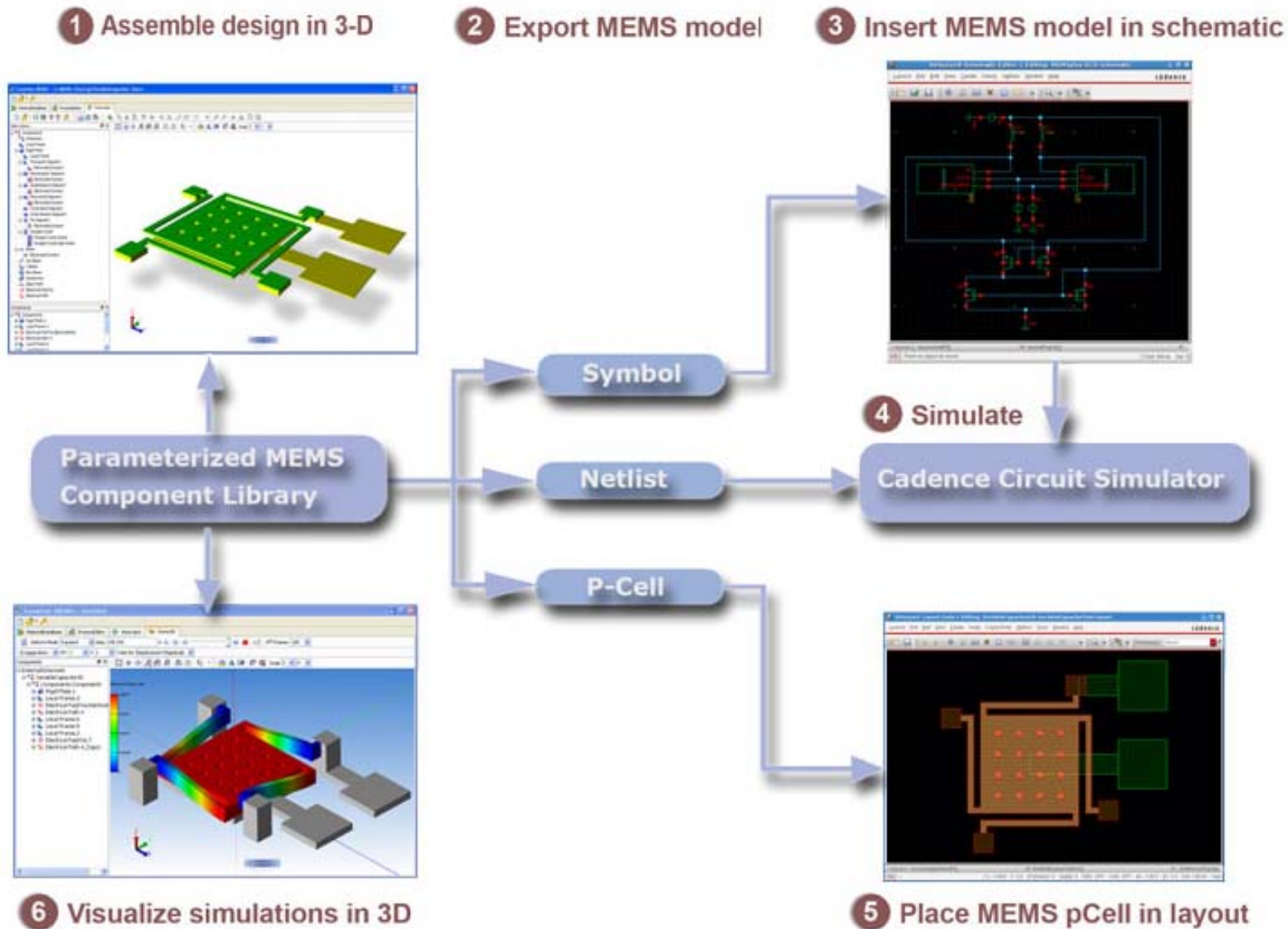
- **Seamless Connection to IC Design**

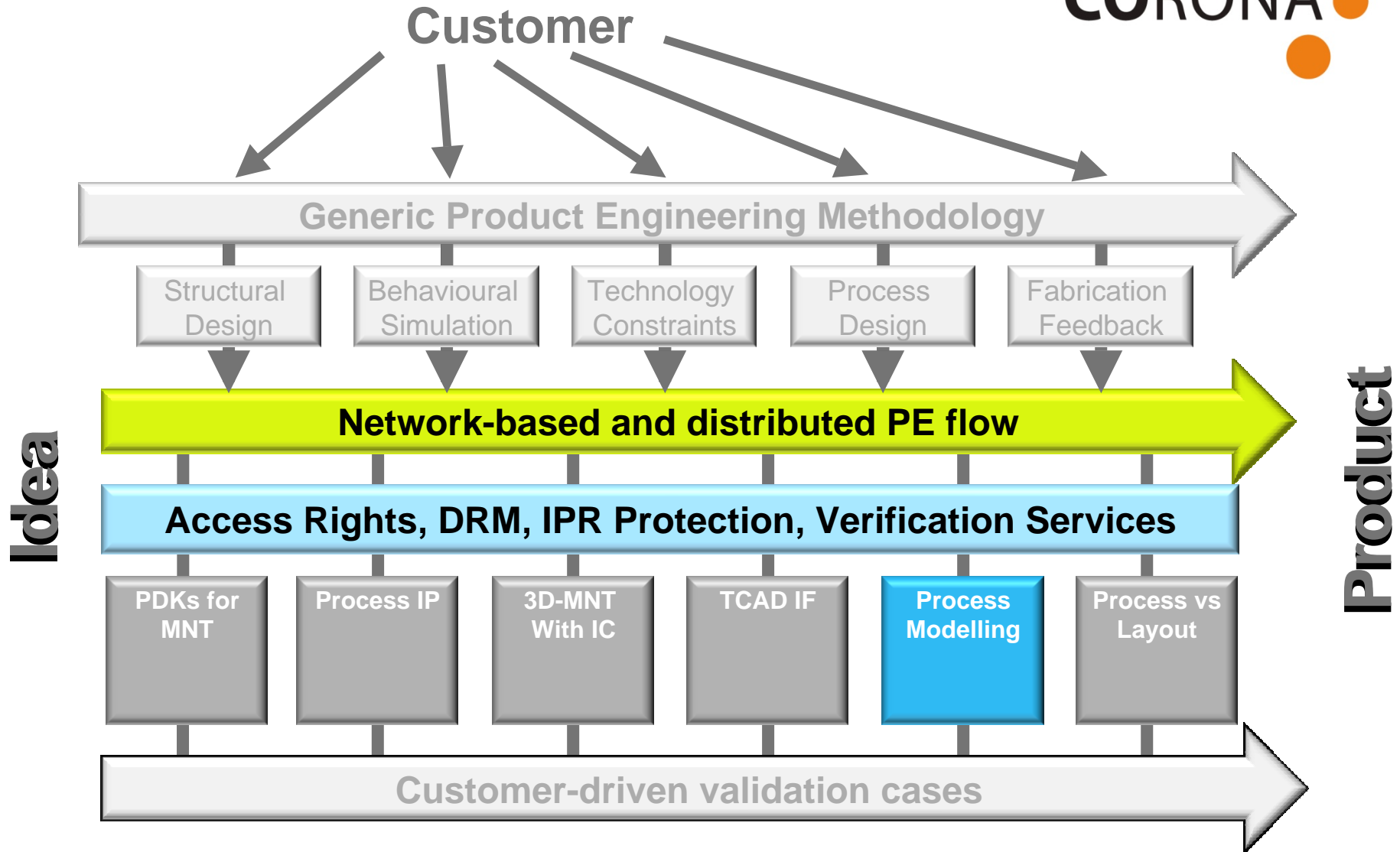
- The MEMS designer transfers the model to the IC-designer
- The IC designer does electronic system design





# Design of 3D MEMS with IC





# Virtual Fabrication



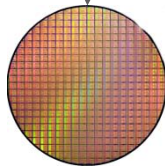
*Actual Fab*

*Blank wafer*



Move wafer thru line,  
following recipe  
*(partial or full sequence)*

*Processed wafer*



*Sample,  
image,  
measure*

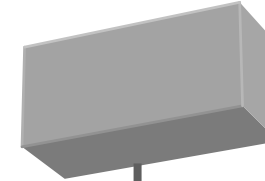


2-D layout

*Virtual Fab  
software*

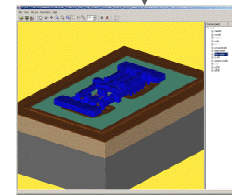


*Rectangular  
area of interest*



Mimic equipment  
to build 3-D model  
*(partial or full sequence)*

3-D model

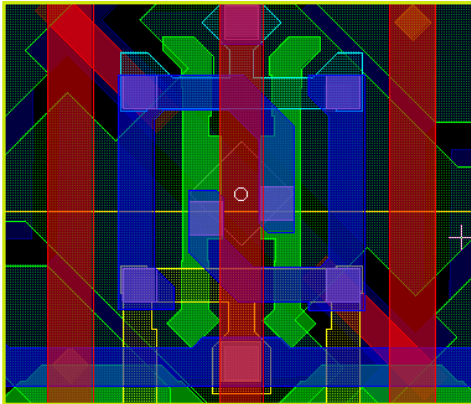


*Visualize,  
image,  
measure*

# How it works

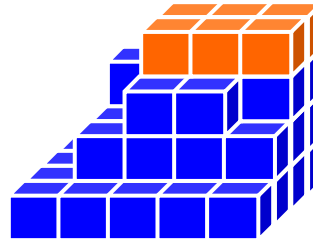


## GDSII Layout



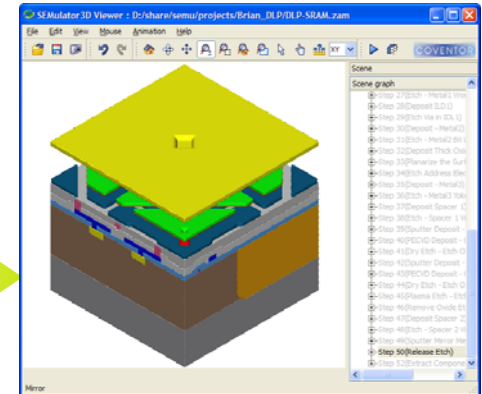
## 3D Modeling Engine

builds voxel models by applying a sequence of primitive operations

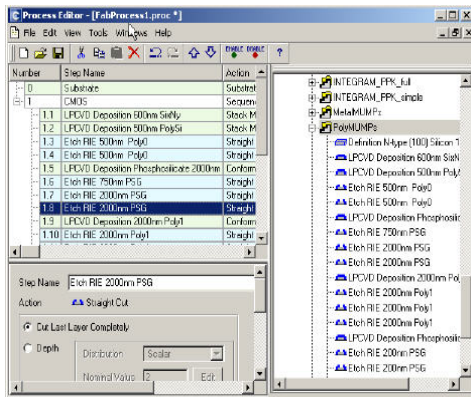


Voxels are 3D pixels

## Visualization

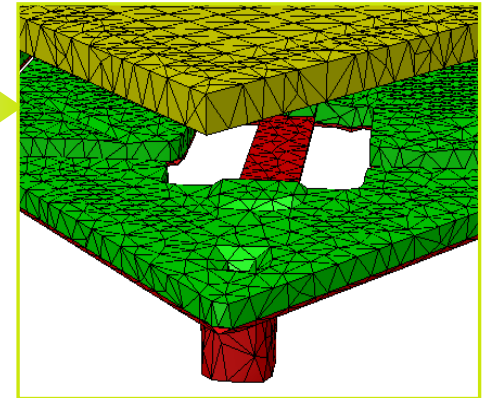


## Process Description

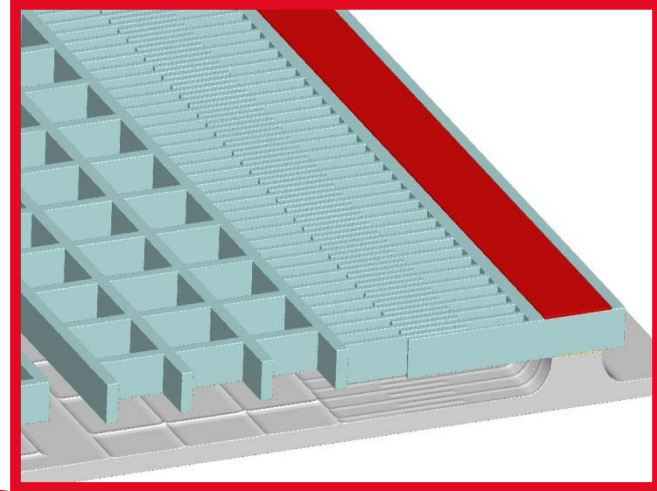
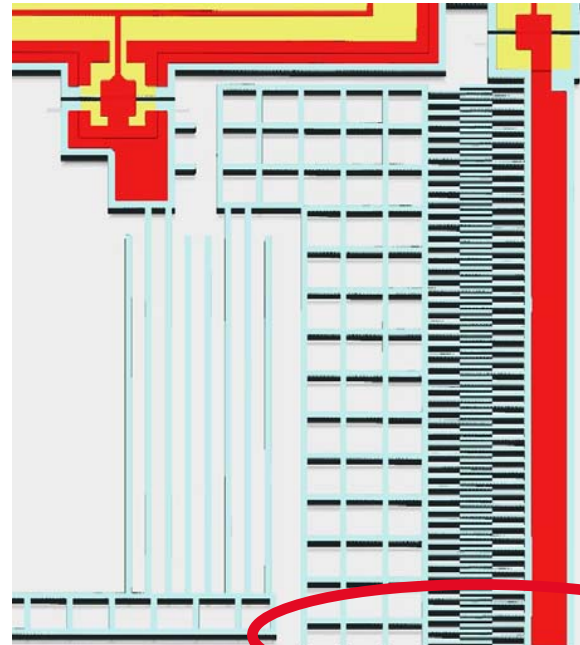
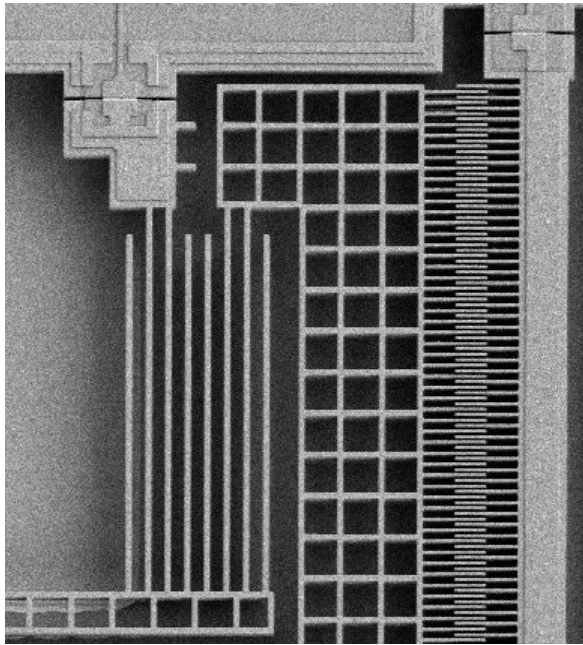


Customizable to any process technology

## Simulation Mesh



# Use case example: X-FAB SOI



SEM image

images created with SEMulator3D

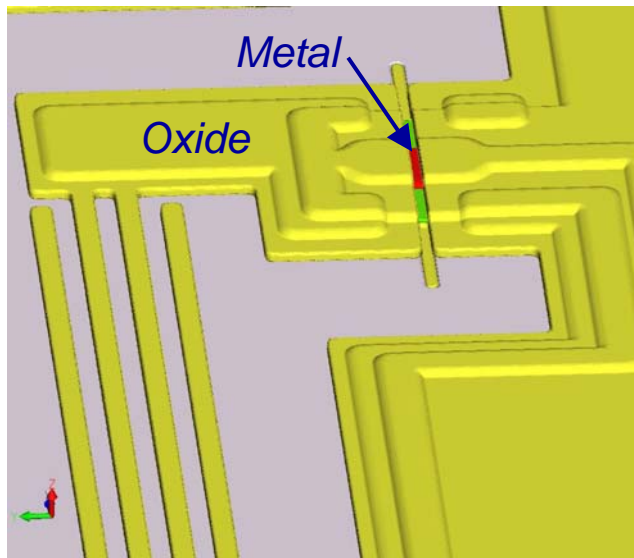
## X-FAB uses virtual fab runs for...

- Customer support, marketing of MEMS foundry technologies
- Checking new designs prior to actual fabrication
- Process development
- Failure analysis

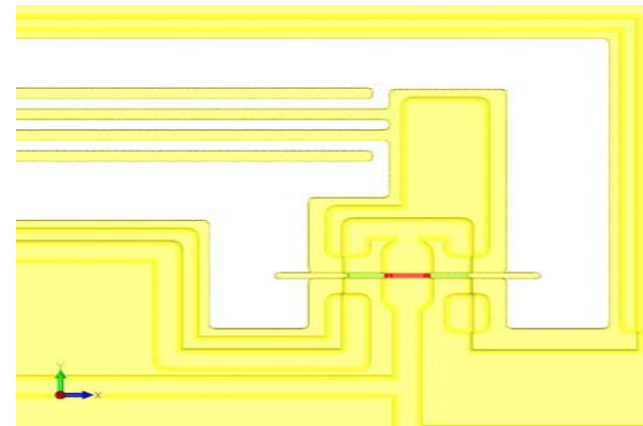
# Example: Design Check



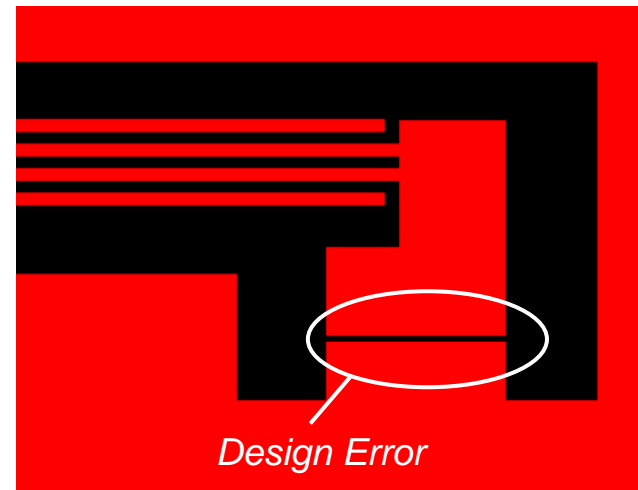
**Example: A design error that was caught before mask tape-out**



*Visual inspection of SEMulator3D model showed isolation trench structure would have been improperly exposed to subsequent DRIE*



*Top view of SEMulator3D model*

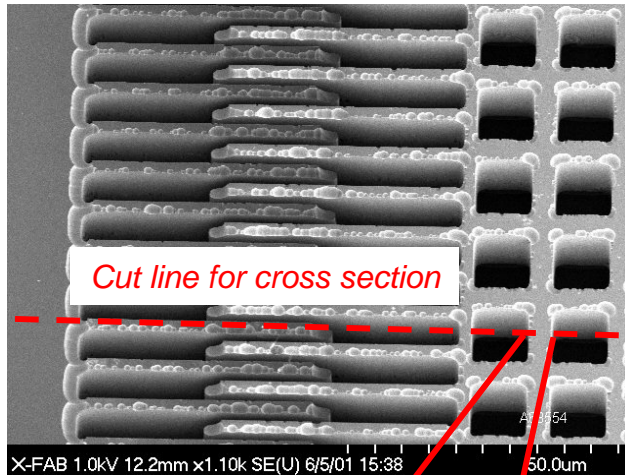


*DRIE Oxide Mask*

# Example: Failure Analysis

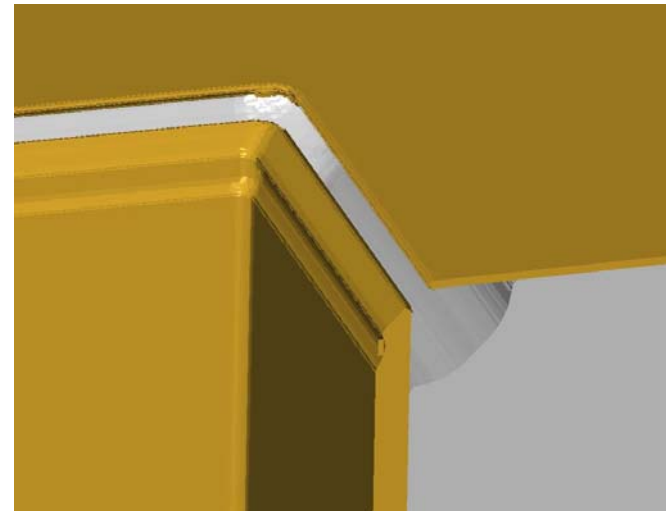
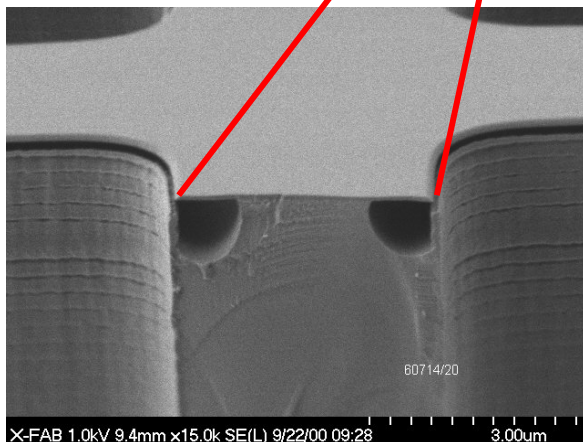


During development of X-FAB's technology, undesired pockets formed in mechanical layer during release etch

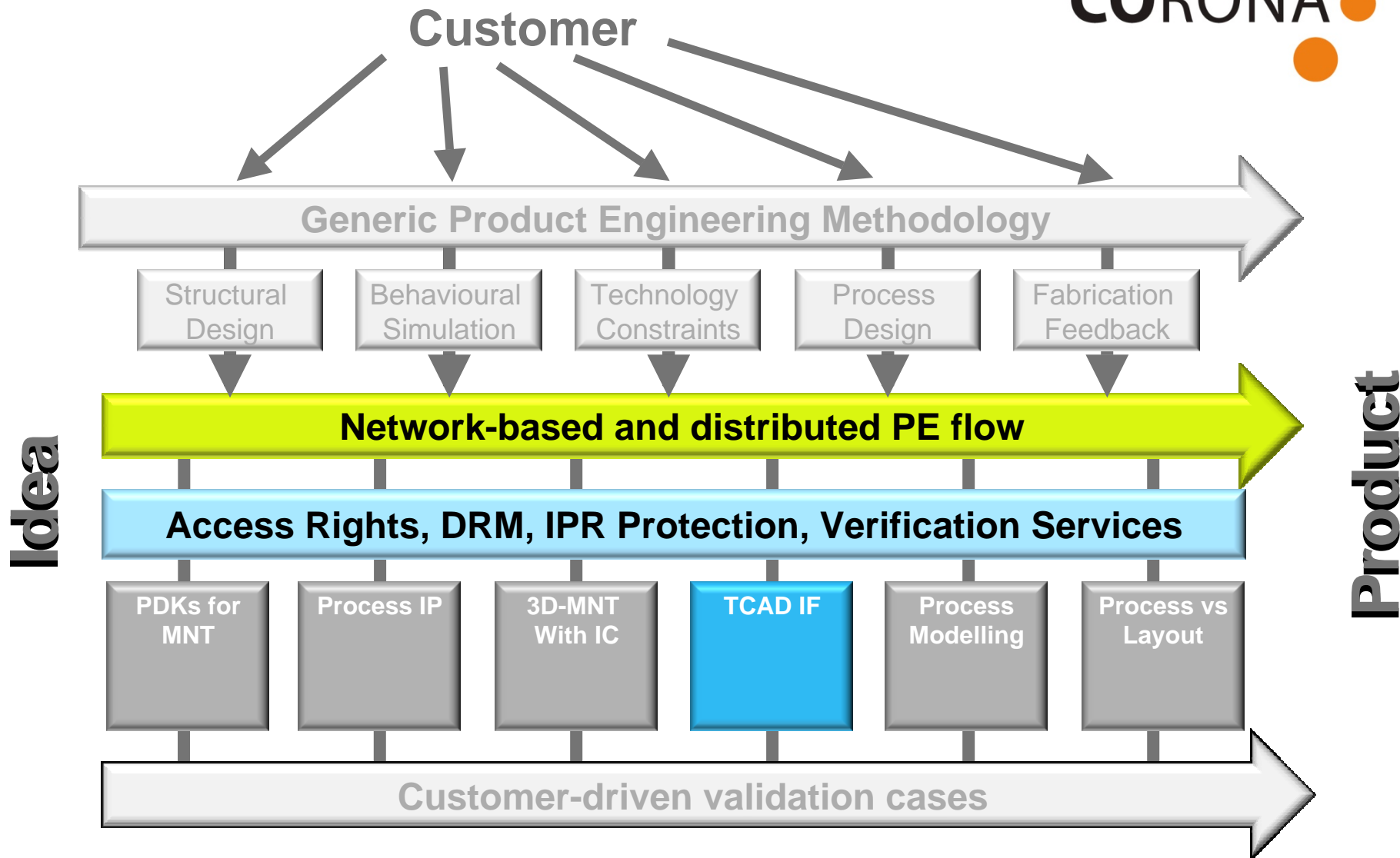


Detailed 3-D process model of the protective oxide layer confirmed the hypothesis about the process failure:

*The release etch for the movable parts was etching through thin spots in the protective oxide layer*

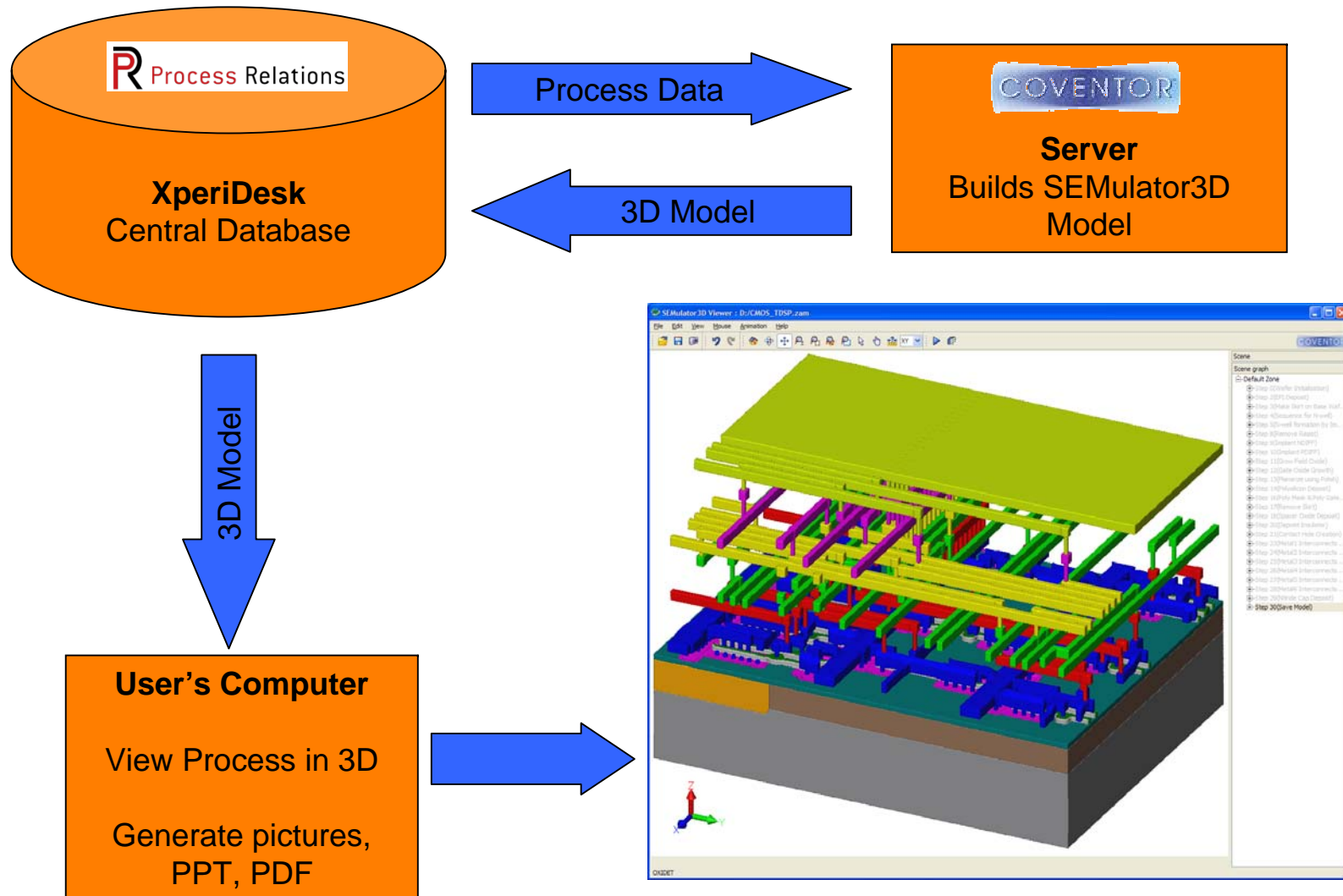


*3-D Model*

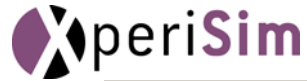




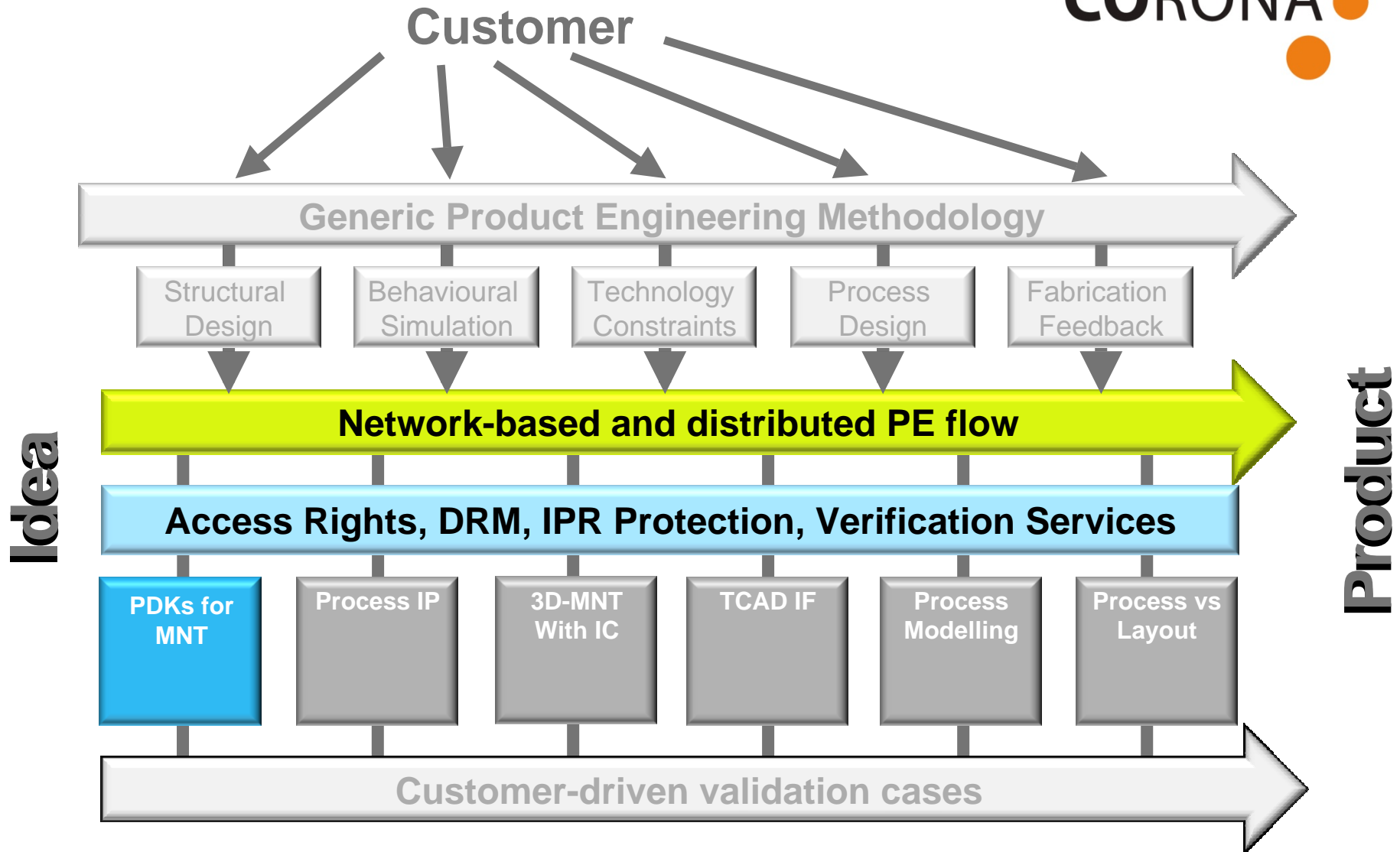
# SEMulator3D and XperiDesk Bi-Directional Integration



# Virtual manufacturing via simulation



The screenshot shows the XperiDesk 2009.1 software interface. The title bar reads 'XperiDesk 2009.1 - Demonstrator process 2 (#13)'. The interface includes a menu bar (File, Settings, Help), a toolbar, and a sidebar with navigation options like 'Masksets', 'Tracking experiments', 'Tools &amp; Models', 'Process flows', 'Process steps', 'Materials &amp; Wafers', 'Users &amp; Groups', and 'Parameters &amp; Units'. The main workspace is divided into several panes. On the left, a tree view shows the 'Process flows' hierarchy, with 'Demonstrator process 2 (#13)' selected. The central pane displays the 'Process flow - Demonstrator process 2 (#13)' with a list of steps: Silicon (#3) - [Si], Si3N4 LPCVD (#1), Cr sputtering (#3), Litho\_AZ5214 std\*, Rapid Thermal Annealing (#1), CR etching (#1), Rest strip Aceton (#1), Standard Cleaning\*, and Lithography\_AZ5214 std rev. The 'Selected flow component' pane on the right shows details for 'CR etching', including its name and a description: 'The first etching processes used liquid-phase ("wet") etchants. The wafer can be immersed in a bath of etchant, which must be agitated to achieve good process control. For instance, buffered hydrofluoric acid (BHF) is used commonly to etch silicon dioxide over a silicon substrate. Different specialised etchants can be used to characterise the surface etched.' The bottom pane shows a 3D simulation of a wafer with a grid of red lines representing the etching process. The bottom status bar indicates 'XperiDesk 2009.1 - [dortloff - Marc Randa]'.



# Design Kit Motivation

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CORONA



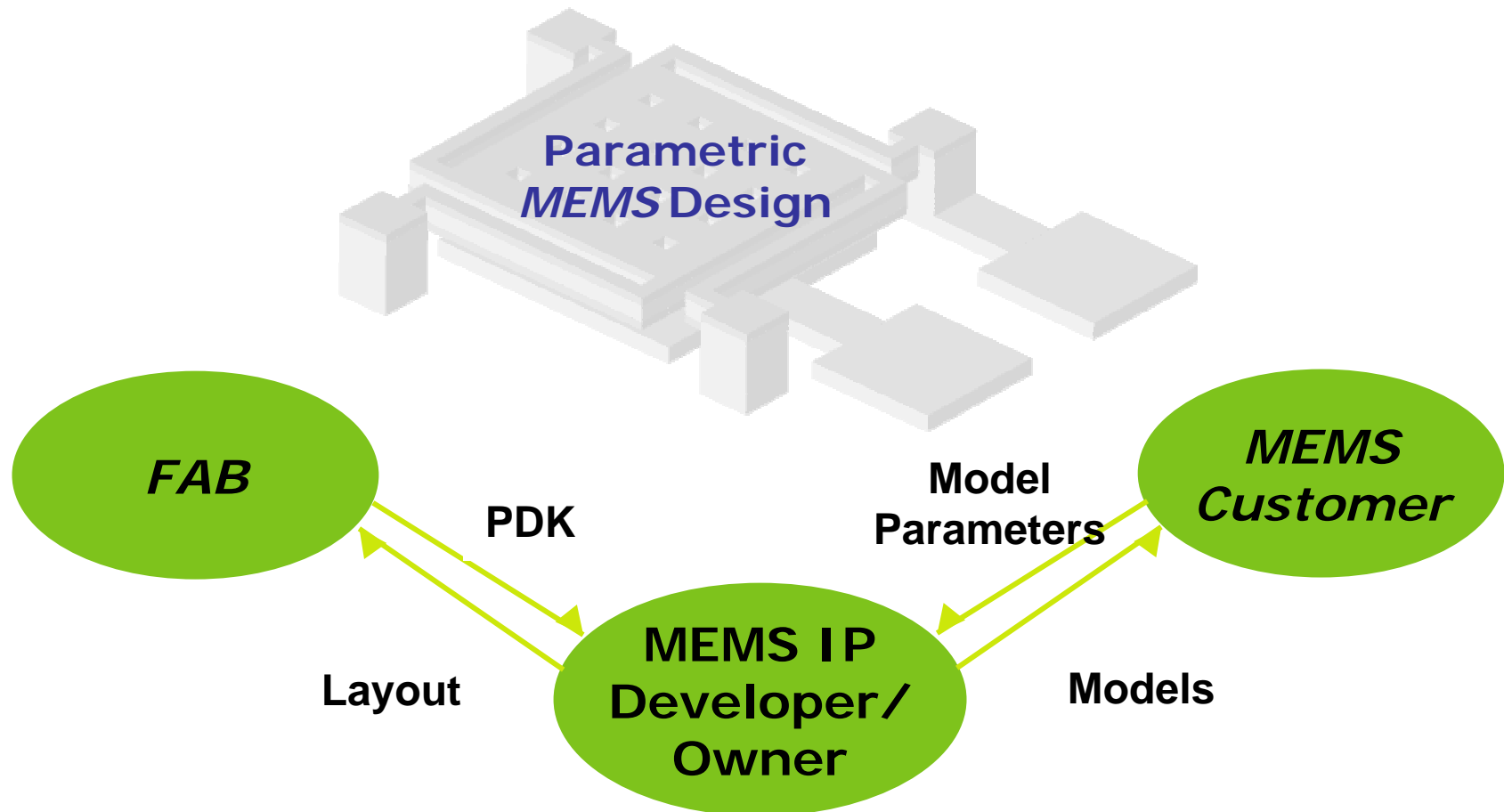
**Designer**

**... use tools to build a bridge**

# Enable MEMS Eco-System



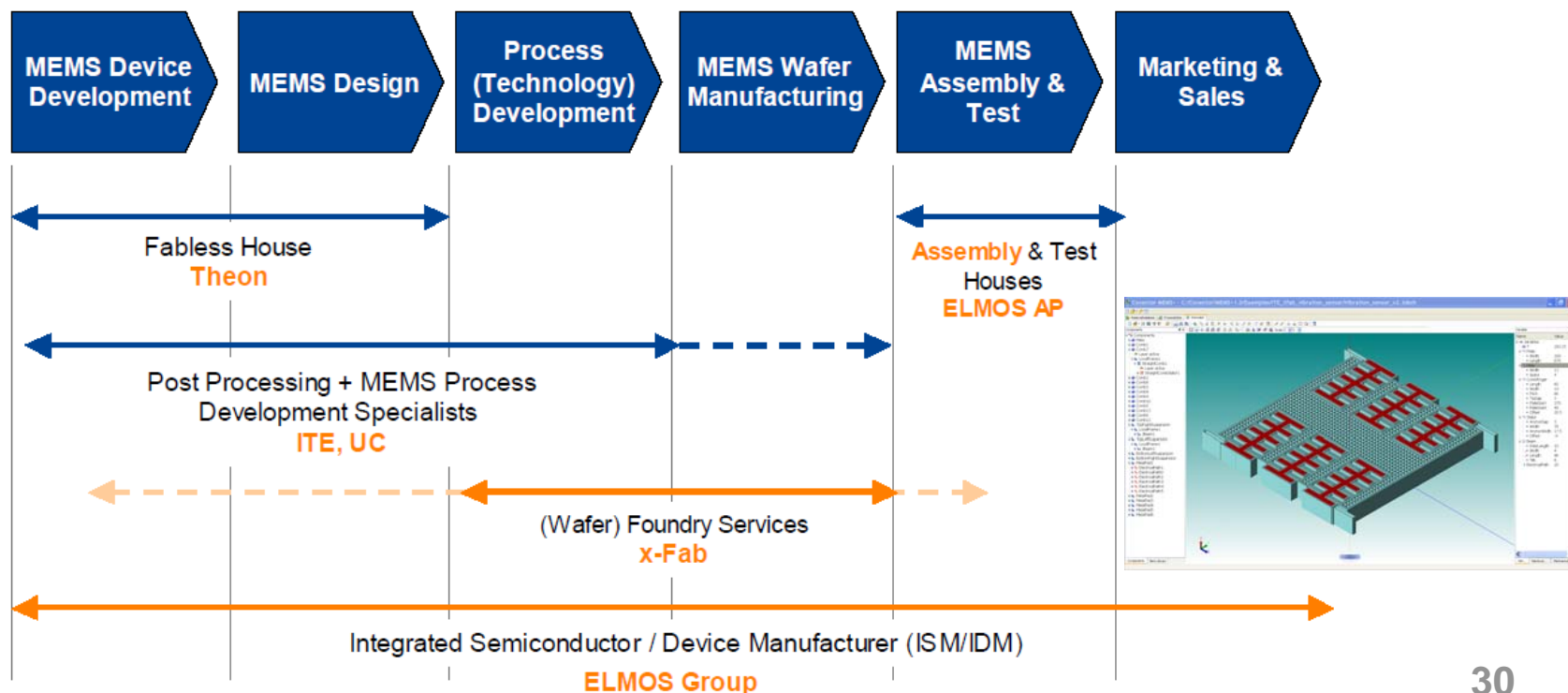
- Facilitate communication between the distributed partners of the MEMS eco-system



# Validation via Business Cases



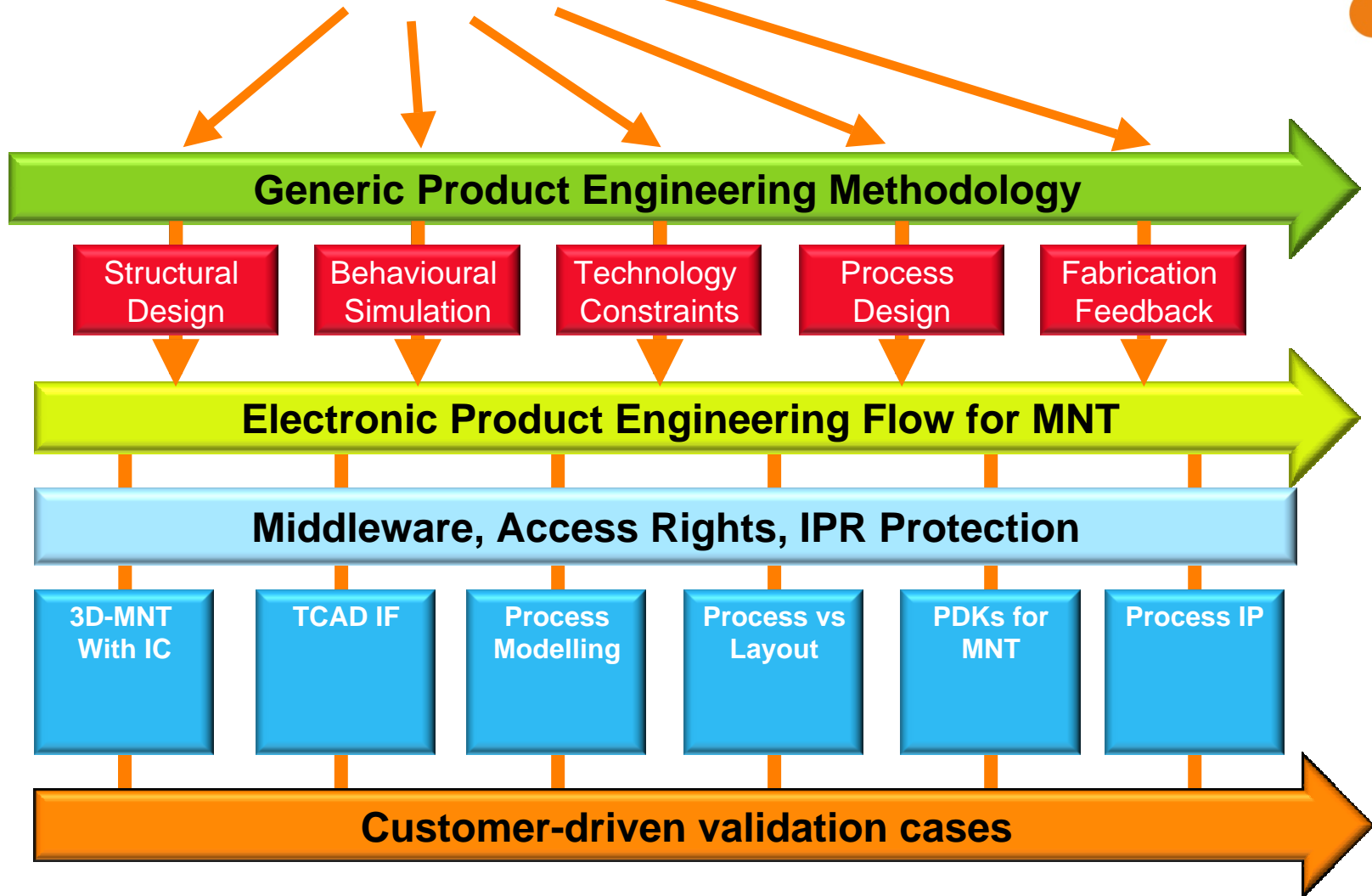
- **Fab Less -> Theon -> Capacitive Accelerometer**
- **Combination XFAB / ITE -> Technology design / Post Processing -> Smart vibration detector**
- **University Cambridge -> post processing -> Life Science**
- **Integrated Manufacturer -> ELMOS -> Pressure Sensor System**



**Customer**

**Idea**

**Product**



# Contact

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Benefit from shorter time to market by:

- Faster product engineering
- Customer-lead multi-site product development
- Access to knowledge-base on design and processes
- Information and communication technology (ICT) structure and tools

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A NMP project in FP7 funded by the European Commission  
NMP2-SL-2008-213969



**R** Process Relations  
Streamlining Process Development

