Fraunhofer ISIT

Hermetic and Reliable Wafer-Level Packaging for MEMS

T. Lisec and W. Reinert
Fraunhofer ISIT, Itzehoe, Germany

7th ESA Round Table on Micro & Nano Technologies for Space Applications
September 13th-17th 2010, ESA/ESTEC Noordwijk, The Netherlands

Outline

- Introduction
- Bonding techniques
- Cap wafer processing at ISiT
- Inertial sensor packaging
- RF MEMS packaging
- Micro mirror packaging
- Summary

Introduction

MEMS Packaging

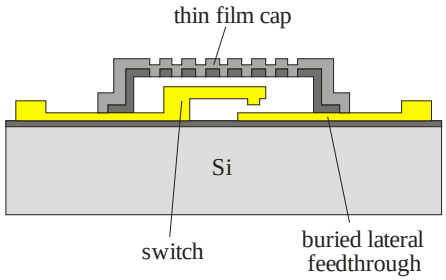
- Majority of MEMS requires hermetic packaging.
- Typically packaging is needed before a singulation into dies to avoid contamination and damaging of the MEMS structures during the dicing and the subsequent single chip handling.
- Package must be well adapted to the MEMS in size.
- Packaging must be cheap.

Packaging on wafer level required!

- Most common is wafer-to-wafer bonding.
- For large devices chip-to-wafer bonding is a possible alternative.
- For small devices thin-film capping can offer advantages in chip size and price.

Introduction

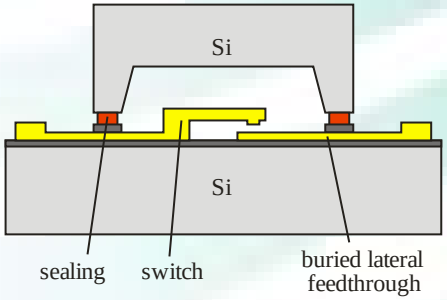
Thin-Film Capping



- fully integrated, IC compatible,
- rather no influence on the device,
- minimum space requirements,
- package height neglectible,
- flip-chip bonding possible,

- rather not suitable for large devices as well as large topologies,
- cap is mechanically sensitive,
- in very small cavities outgassing can be problematic,

Wafer-to-Wafer Bonding



- process complexity lower,
- device area can vary in a wide range,
- mechanically robust,
- controlled atmosphere and pressure inside the cavity,

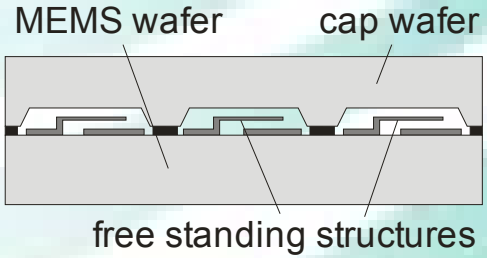
- additional wafer needed,
- thinning of the bonded stack required to reduce chip height,
- to allow flip-chip bonding vertical vias must be created,
- sealing can impact device performance,

Bonding Techniques

Hermetic Wafer-to-Wafer Bonding Techniques

- Low-T and anodic bonding are less suited for wafer-level packaging in this particular case:

→ Low-T: large, very smooth and flat bond area required. activation procedure can impact the MEMS structures.



→ Anodic: large voltages must be applied, which can impact the MEMS as well as integrated electronic components.

	Low-T direct	Anodic	Au-Si	Au-Sn	Glass Frit
Process temperature	< 400°C	< 450°C	≈ 400°C	≈ 300°C	< 450°C
Outgassing	none	O_2	Ar possibly	Ar possibly	CO, H_2O, C_xH_y
Interaction with MEMS structures	possible	possible	none	none	none
Vacuum without getter	0.1 mbar	> 10 mbar	1 mbar	1 mbar	1-5 mbar

Bonding Techniques

Glass Frit, Au-Si and Au-Sn Bonding

- Bonding is performed at ISiT on 6 and 8 inch using equipment from Süss Microtec.

	Glass Frit	Au-Si	Au-Sn
Bonding temperature	< 450°C	~ 400°C	~ 300°C
Specific requirements on the MEMS side	diffusion barrier beneath the bond frame	clean, smooth Si, at least 2 µm tick	Au bond frame
Storage time limitations	no	MEMS, few hours (Si oxidation)	cap, few days (Sn oxidation)
Bond frame width	> 150 µm	< 100 µm	< 80 µm
Topology tolerance	2 µm	few tenth of nm	2 µm
Outgassing	yes	possible	possible
Getter integration possible?	yes	yes	yes
Remelts if bonding temperature is reached again?	yes	yes	no
Grinding and polishing of bonded stack possible?	yes	yes	yes

Cap Wafer Process

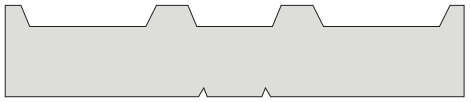
Basic Cap Wafer Process

- Only 3 lithography steps required, Si as well as glass wafers can be used.

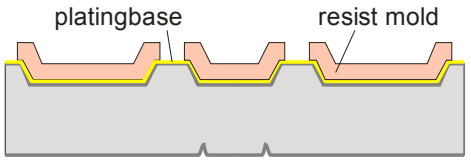
- Single-side or double-side polished Si substrate, with a thermal oxide.

- 1st lithography (MEMS cavities and bond pad recesses), dry etching of the oxide and resist removal.

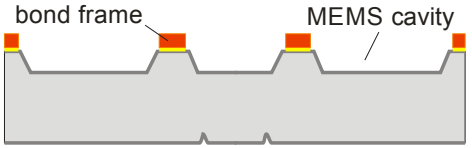
- 2nd lithography (backside alignment and dicing marks), dry etching of the oxide and resist removal.



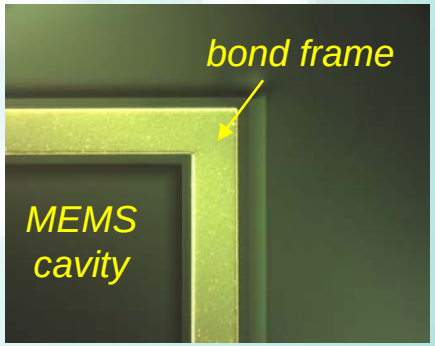
- Anisotropic etching in KOH to create the MEMS cavities on the frontside and the marks on the backside, then oxide removal and oxidation again.



- Platingbase deposition and 3rd lithography (bond frame) using spray coating.



- Electroplating of the bond frame and removal of the platingbase if required.

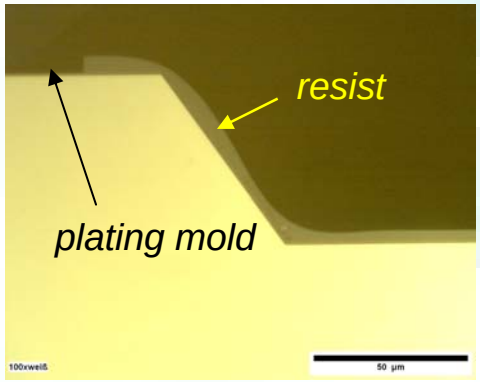


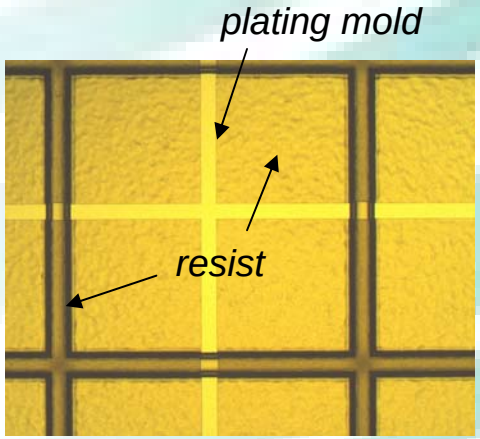
Cap Wafer Process

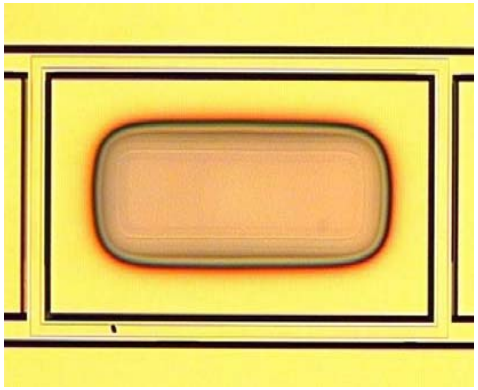
Special Cap Wafer Features

Use of spray resist coating allows:

- Cavity depth of several 100 µm,
- Structures at the cavity bottom,
- Processing of dry etched cavities with vertical side walls (but this is more expensive).







- Getter layer can be deposited within the cavity (one additional lithography step is required):
  → Minimum pressure inside the cavity in the range of 1 µbar with getter in contrast to 1 mbar without.

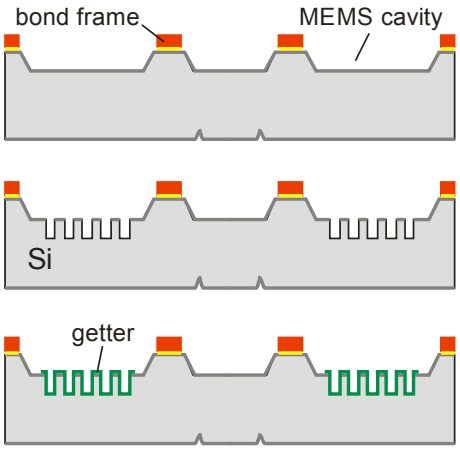
Cap wafer with Zr based getter from SAES at the bottom of the cavity.

- Dimensions of the cavity and the surrounding Si frame can be varied within a wide range depending on the MEMS as well as the particular bonding technique.

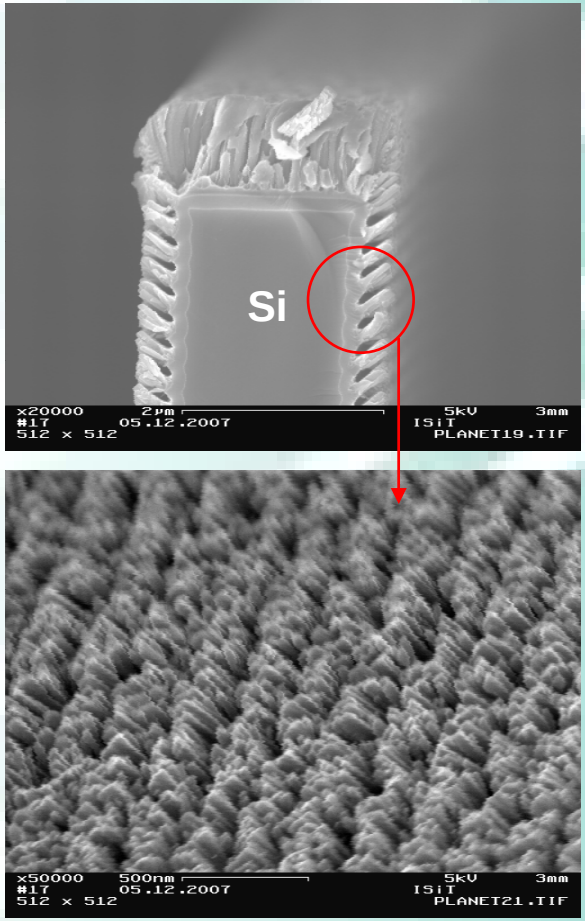
Cap Wafer Process

Special Cap Wafer Features

- Getter enhancement by structuring of the cavity bottom (two additional lithography steps required), → increased getter capacity / reduced area,
- Characteristic scalloping at the sidewalls of the DRIE structures induce needle-type growth of the getter material,



- Basic cap wafer with sealing frame.
- 4th lithography and dry etching of the Si at the bottom of the MEMS cavity by DRIE.
- Getter deposition by evaporation, 5th lithography and getter structuring by wet etching.

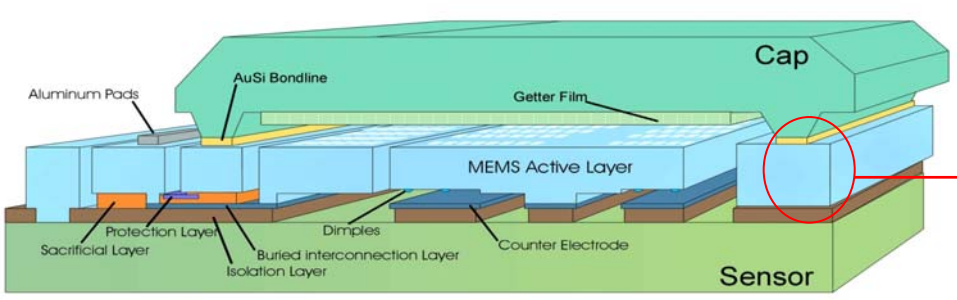


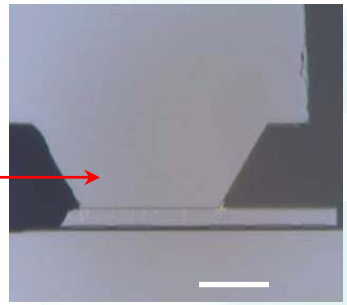
View on TIGER3D getter from ISiT.

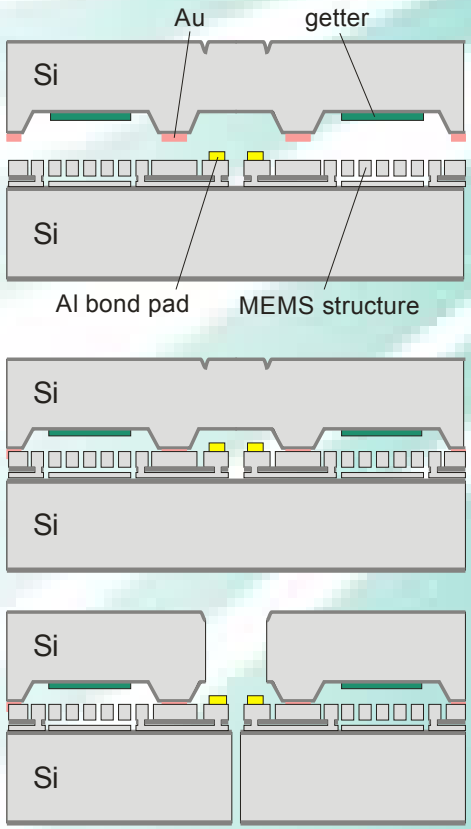
Applications

Inertial Sensor Packaging

- Bonding directly on bare silicon of MEMS wafer after the release procedure.
- No bond frame preparation on MEMS wafer necessary.
- Buried lateral feedthroughs below the epi-poly layer.
- Getter integrated on the cap wafer.
- By smart backfilling the gas pressure inside the cavity can be adjusted to any value between 1 µbar and 1 bar.
- Overmolding at up to 90 bar possible.
- Bond strength high enough to allow subsequent thinning.







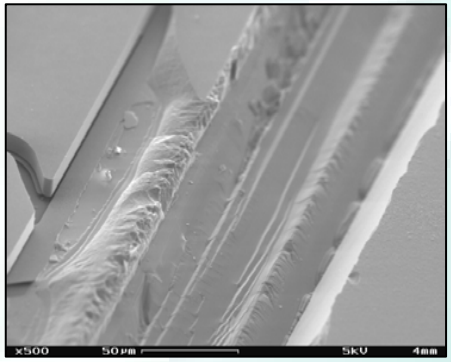
Schematic cross-section of a packaged sensor and foto of the seal frame area.

Applications

Inertial Sensor Packaging

Stress Test	ABV	#	Sample size	Sample type	Method / Conditions	Readout Points
TEST GROUP A						
Temperature-Humidity-Bias	THB	A2	60	Sensor	JESD22-A101 / +85°C, 85% RH, biased (shirp)	@ 500 hrs, end of test (1000 hrs)
Autoclave	AC	A3	77	Sensor	JESD22-A102 / +121°C, 2bar, 100% RH, unbiased	end of test (96 hrs)
Temperature Cycling	TC	A4	77	Sensor	JESD22-A104 & App. 3, Grade 1 / -50°C to +150°C, unbiased	@ 500 cycles, end of test (1000 cycles)
High Temperature Storage Life	HTSL	A6	1	Wafer	JESD22-A103, Grade 1 / +150°C, unbiased	@ 500 hrs, end of test (1000 hrs)
TEST GROUP B						
Neon Bombing Test after stress of THB	NBT2		45	Sensor	Ne, 3bar	end of test (96 hrs)
Cap Shear Test after Stress	CAPS2	DS	45	Sensor		none
TEST GROUP C						
Neon Bombing Test	NBT		2	Wafer	Ne, 3bar	end of test (96 hrs)
Cap Shear Test	CAPS1	DS	50	Sensor		none
Ball Shear Test	BALLS	C5	10	Sensor	AEC Q100-010	none
Physical Dimensions	PD	C4	10		JESD22-B100 / B108	none
TEST GROUP E						
Pre- and Post-Stress Function/Parameter Test on Sensor Level	TEST1	E1	Acc. test		to supplier data sheet or user specification	@ all stress test readout points
Pre- and Post-Stress Function/Parameter Test on Wafer Level	TEST2	E8	Acc. test		to supplier data sheet or user specification	@ all stress test readout points
Electrical Distributions	ED	E5	all		AEC Q100-009	None
Characterization	CHAR	E7	all		Acc. Limits	None
TEST GROUP F						
Process Average Testing	PAT	F1	all		Reject units outside limits with +/- 6 sigma	None
Statistical Bin/Yield Analysis	SBA	F2	all		Reject units outside criteria	None
TEST GROUP G						
Constant Acceleration	CA	G3	10	Sensor	30.000g / 1min / -Z direction	end of test
Die Strength Test	DST		20	Sensor	90 bar oil pressure / RT / 1h	None

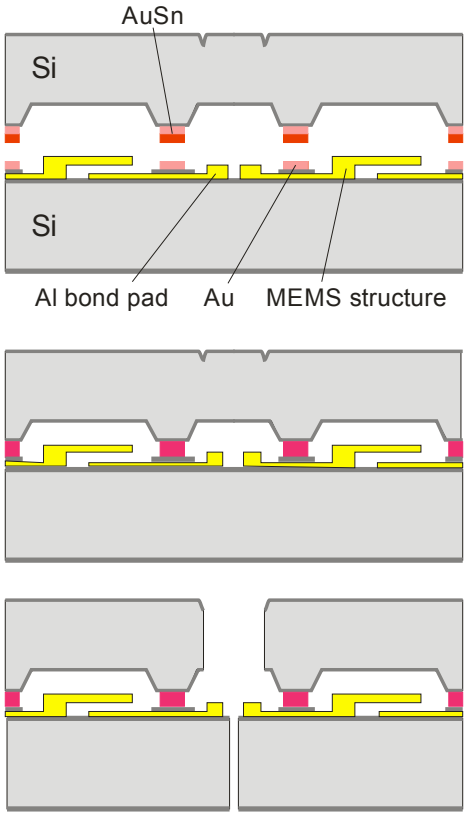
- Packaging process has passed AEC Q100 Qualification (tests described in the table).
- Is used in production on 6-inch wafers since 2008 and on 8-inch since 2010.
- Process yield >94% verified by Q-factor measurement (on 6-inch wafers 2008, 2009).
- Leak rate $<1\times10^{-15}$ mbar·l/s calculated.



Decapsulated device showing chunking of Si in the bond frame area of the MEMS wafer.

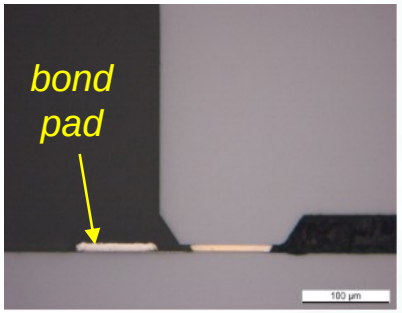
Applications

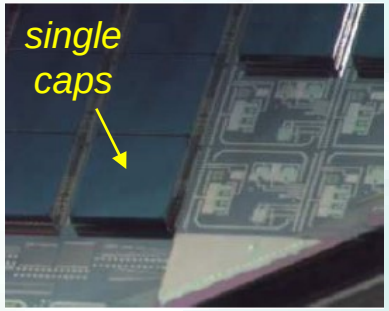
RF MEMS Packaging

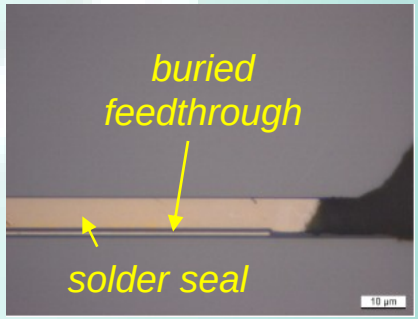


Cross-sections through the seal frame area and wafer after cap dicing.

- Bonding temperature below 300°C to avoid a damaging of the MEMS structures consisting of an Al alloy.
- Reliable sealing of lateral feedthroughs of various height as well as density and dimensions.
- Sealing width ≤ 80 µm.
- Minor solder outflow from the sealing frame area.
- Pure N_2 at a near atmosphere pressure within the cavity.
- Overmolding at up to 90 bar possible.
- Bond strength high enough to allow subsequent thinning.







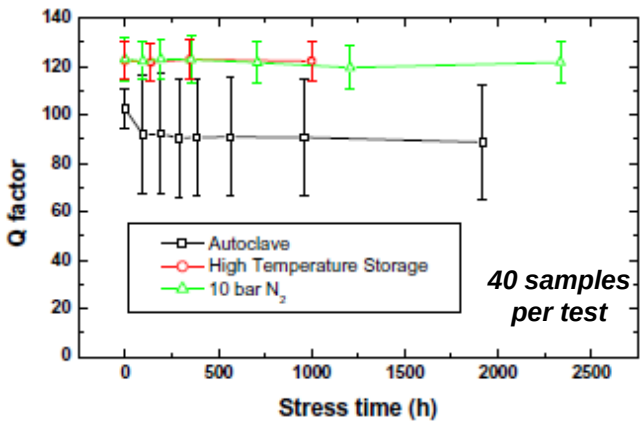
Applications

RF MEMS Packaging

- Packaging process available at ISiT on a pre-production level, 8 inch process is currently established.
- Hermeticity evaluation applying pressure cooker testing (PCT: 121°C, 2 bar,100% RH), high temperature storage (HTS: 121°C), thermal cycling (TC: -50°C/ 150°C), N_2 or Ne bombing (10 bar).
- Results obtained at ISiT for a particular RF-MEMS design on 6 inch:

→ average packaging yield >85% (after 96 h standard PCT),

→ HTS and TC have no impact on hermeticity or cap shear strength.



Special test:

Average Q factor of MEMS switches packaged at ≈ 2 mbar as function of the duration of different reliability tests:

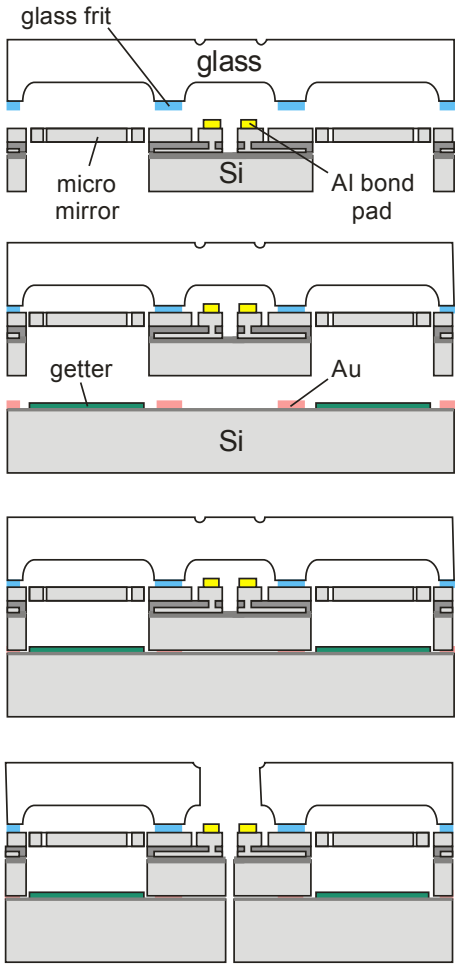
→ 1 device failed after 96 h PCT,

→ other samples do not show any degradation after 1920 h PCT, 1000 h N_2 bombing or 2400 h HTS.

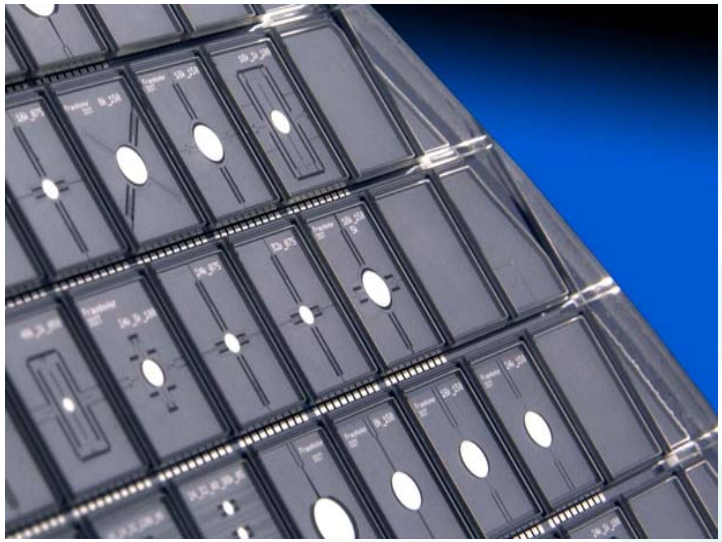
P.J. van der Wel et al., Proc. IRPS, Phoenix AZ, 2008

Applications

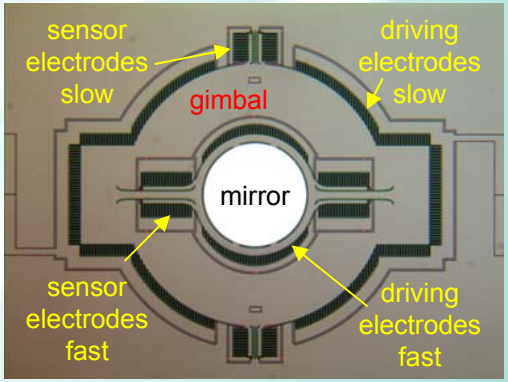
2-Axis Micro Mirror Packaging



- Bonding of 3 wafers in total, glass frit at the cap side and Au-Si eutectic at the bottom side.
- No bond frame preparation on MEMS wafer necessary,
- Buried lateral feedthroughs below the epi-poly layer.
- Getter integrated on the bottom wafer.
- Bond strength high enough to allow subsequent thinning.



Unpackaged mirror structure and a finished wafer after cap dicing.

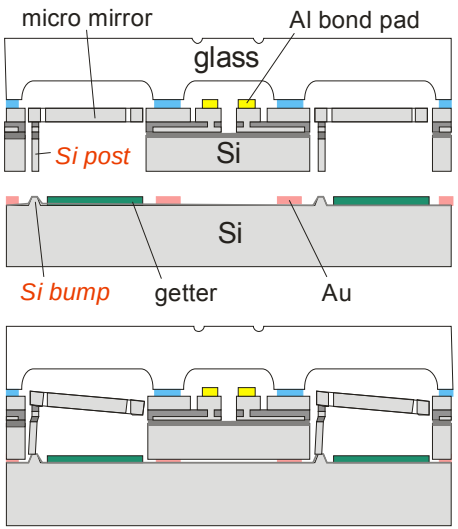


Applications

2-Axis Micro Mirror Packaging

- MEMS process still in development at ISiT.
- Operation in vacuum enables:
  → large mirrors with apertures up to 10 mm,
  → scan angles up to 120°, scan speed up to 200000 lines/s,
  → very low power consumption as well as low driving voltages.

decive parameter	typical value
mirror aperture size	0,5 ... 7 mm
scan frequency fast axis	16 ... 108 kHz
scan frequency low axis	150 ... 2000 Hz
total optical scan angle	20° ... 120°
Q factor	> 60000
power consumption	0,1 µW ... 0,1 mW
driving voltage	5 ... 70 V



- If mirror plate and glass cover are in parallel a parasitic spot (bright dot) occur within the image.
  → Can be avoided by tilting the mirror with respect to the cover, for example using posts below the mirror frame and bumps on the bottom wafer.

M. Oldsen et al., Proc. SPIE, Vol. 6882, 2008

Summary

- Mature technology for MEMS packaging on wafer level using different bonding techniques has been presented.
- Large variety of devices can be sealed in a wide pressure range from 1 µbar to atmosphere using different gases.
- Additional functionality, for example various getters, can be integrated at the cap side within the MEMS cavity.
- Subsequent bonding of several wafers possible using one and the same bonding technique as well as a combination of different techniques.

Fraunhofer ISIT

Thank you!