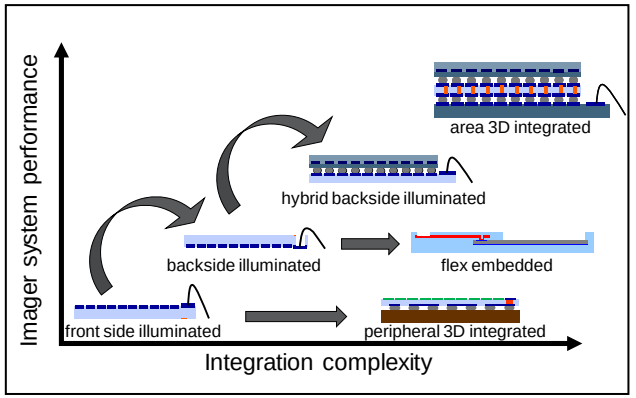
3D INTEGRATED IMAGE SENSORS FOR SMART IMAGING SYSTEMS

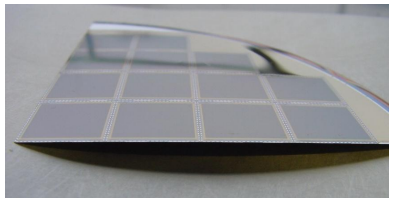
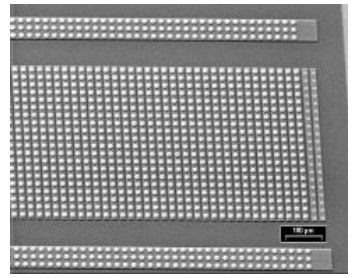
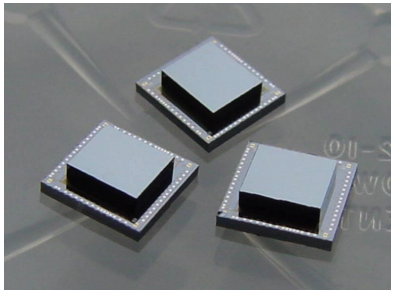
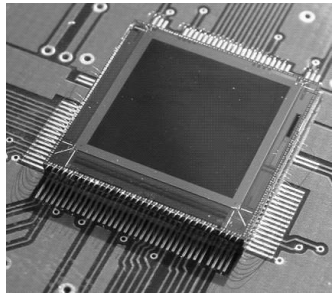
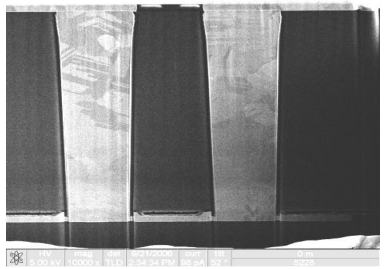
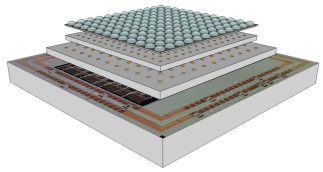
PIET DE MOOR

imec

OUTLINE

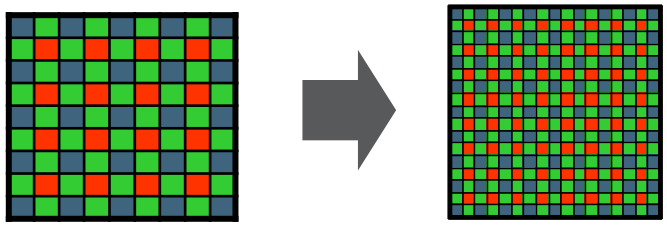


- Introduction: imec vision & roadmap
- Technology components and results:
  - Frontside illuminated imagers
  - Backside illuminated imagers
  - Hybrid backside illuminated imagers
  - 3D integrated imagers
  - Flex embedded imagers
- Conclusion

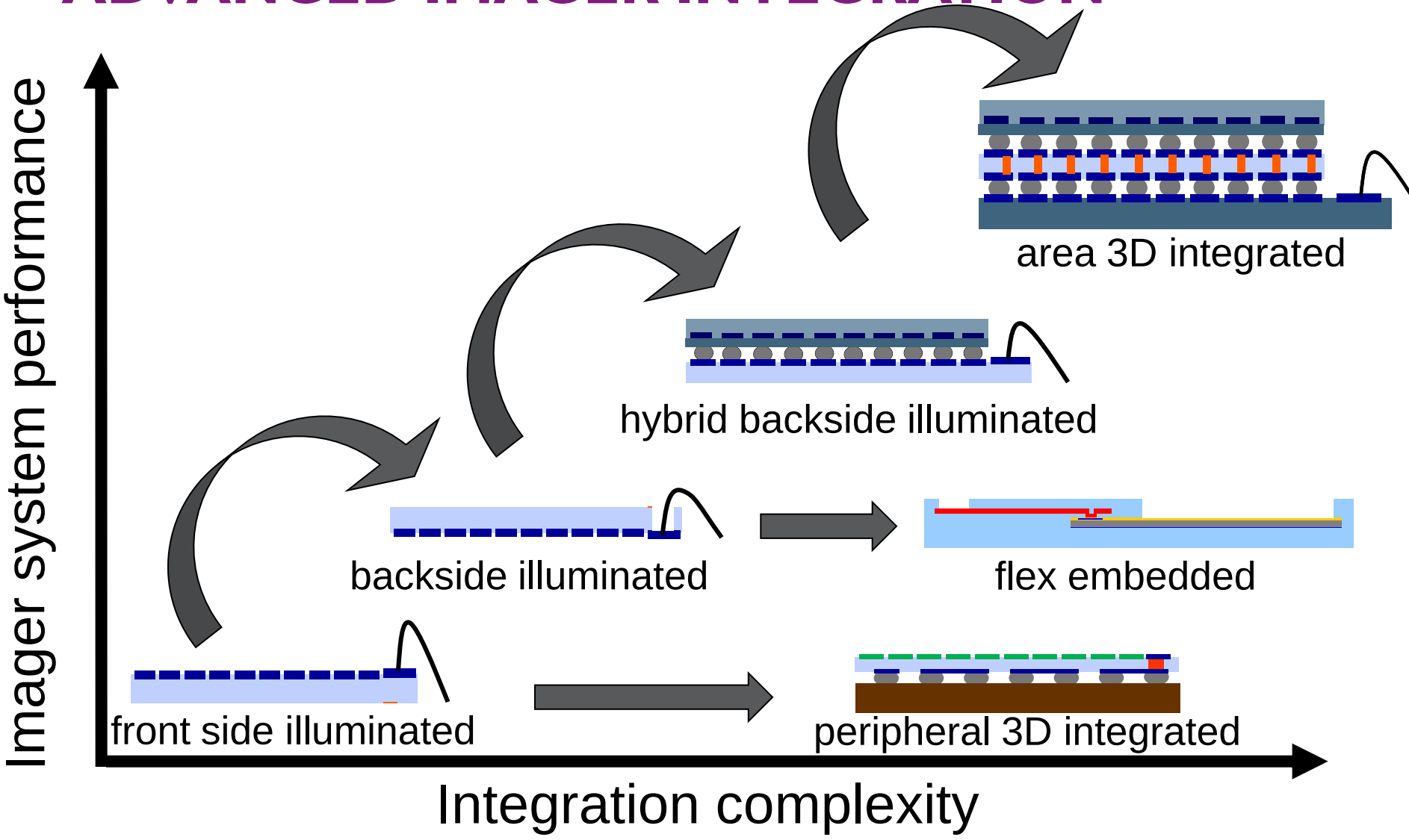
INTRODUCTION

- 2 imager roadmaps with a different approach:
  - Traditional roadmap: scaling to smaller pixels:
    - Equal chip size (or slightly smaller)
    - Higher resolution



    - Lower sensitivity/pixel → backside illumination
  - IMEC Integration/packaging roadmap:
    - Backside illuminated → Hybrid → 3D integrated
    - Enables advanced imaging systems

IMEC VISION: ADVANCED IMAGER INTEGRATION



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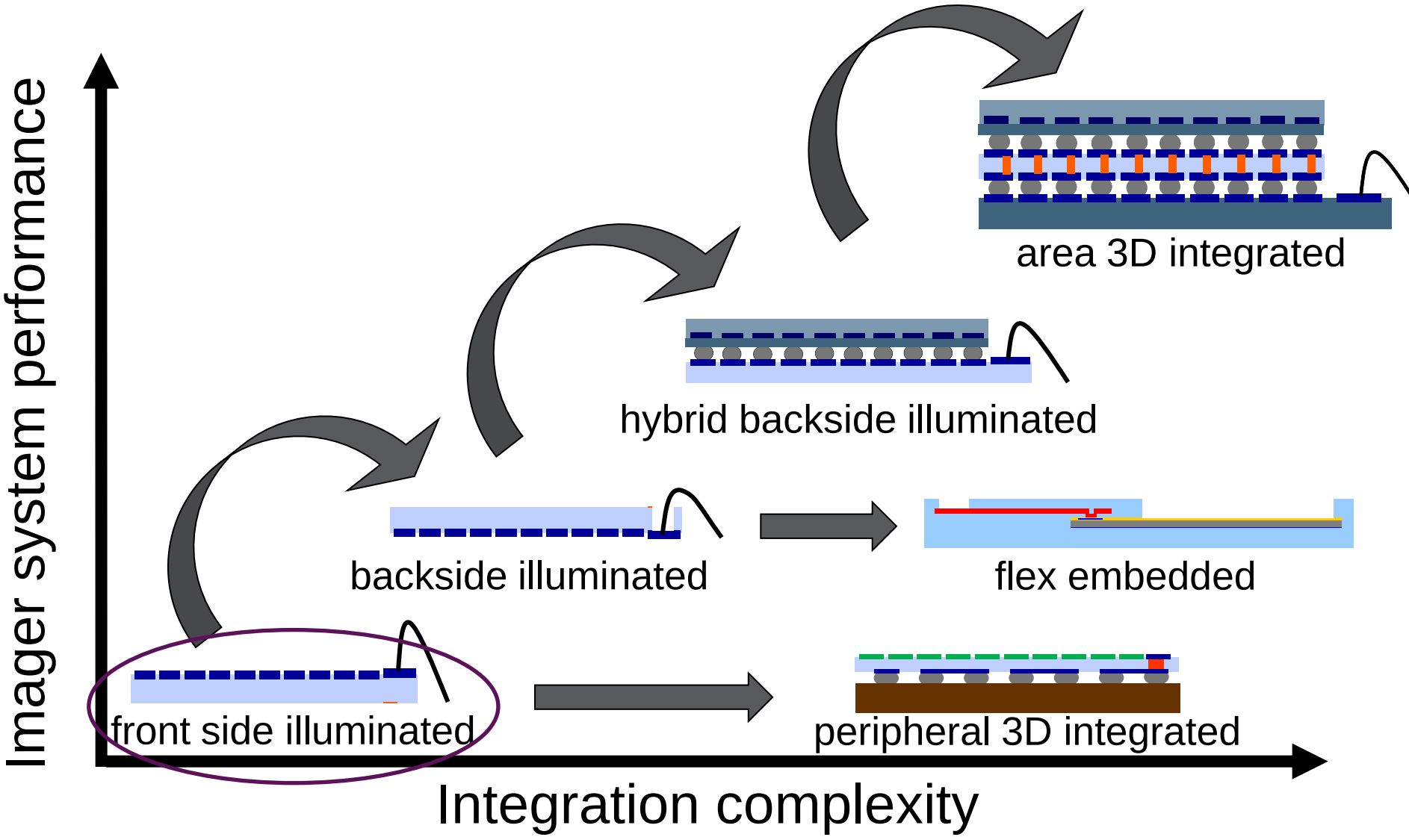
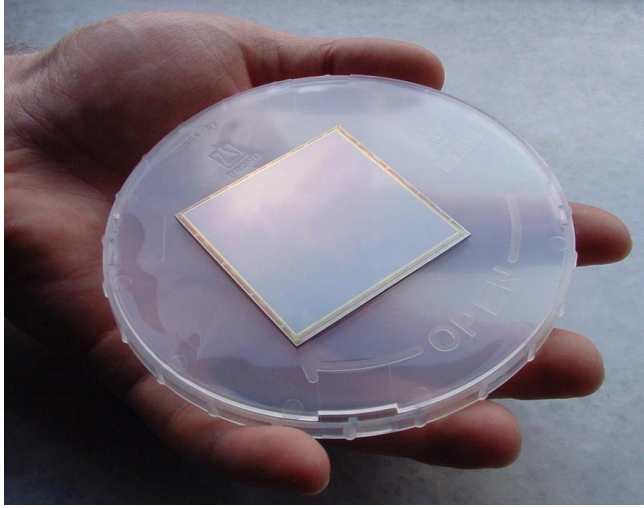
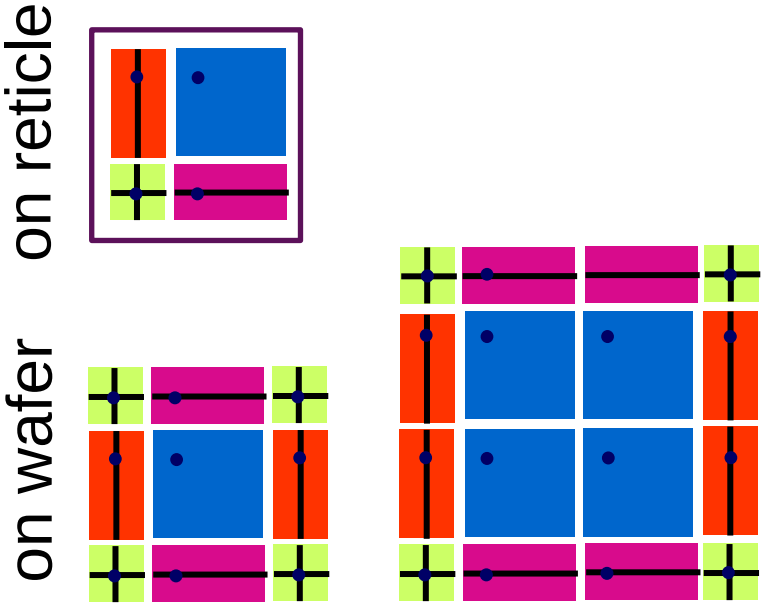
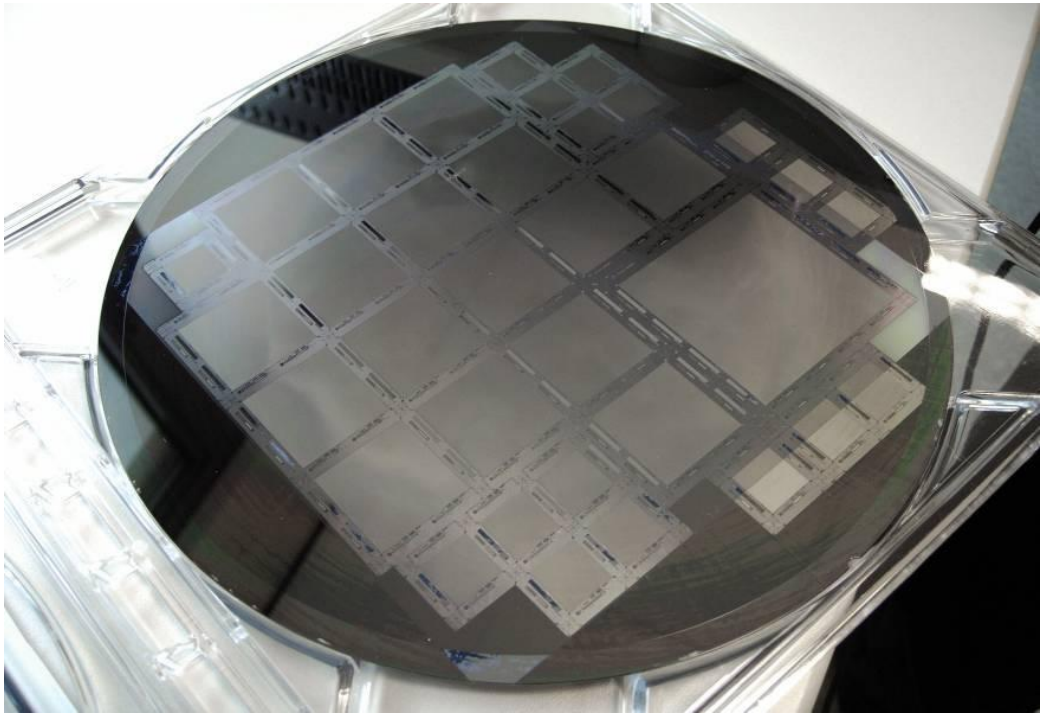

Imager system performance
area 3D integrated
hybrid backside illuminated
backside illuminated
flex embedded
front side illuminated
peripheral 3D integrated
Integration complexity

LARGE AREA IMAGERS: STITCHING



- Stitching allows large area imagers:
  - Up to 1 imager per wafer
- Different imager sizes on one wafer demonstrated:
  - 12x12 mm^2, 25x25 mm^2 and 50x50 mm^2
- Application: e.g. X-ray





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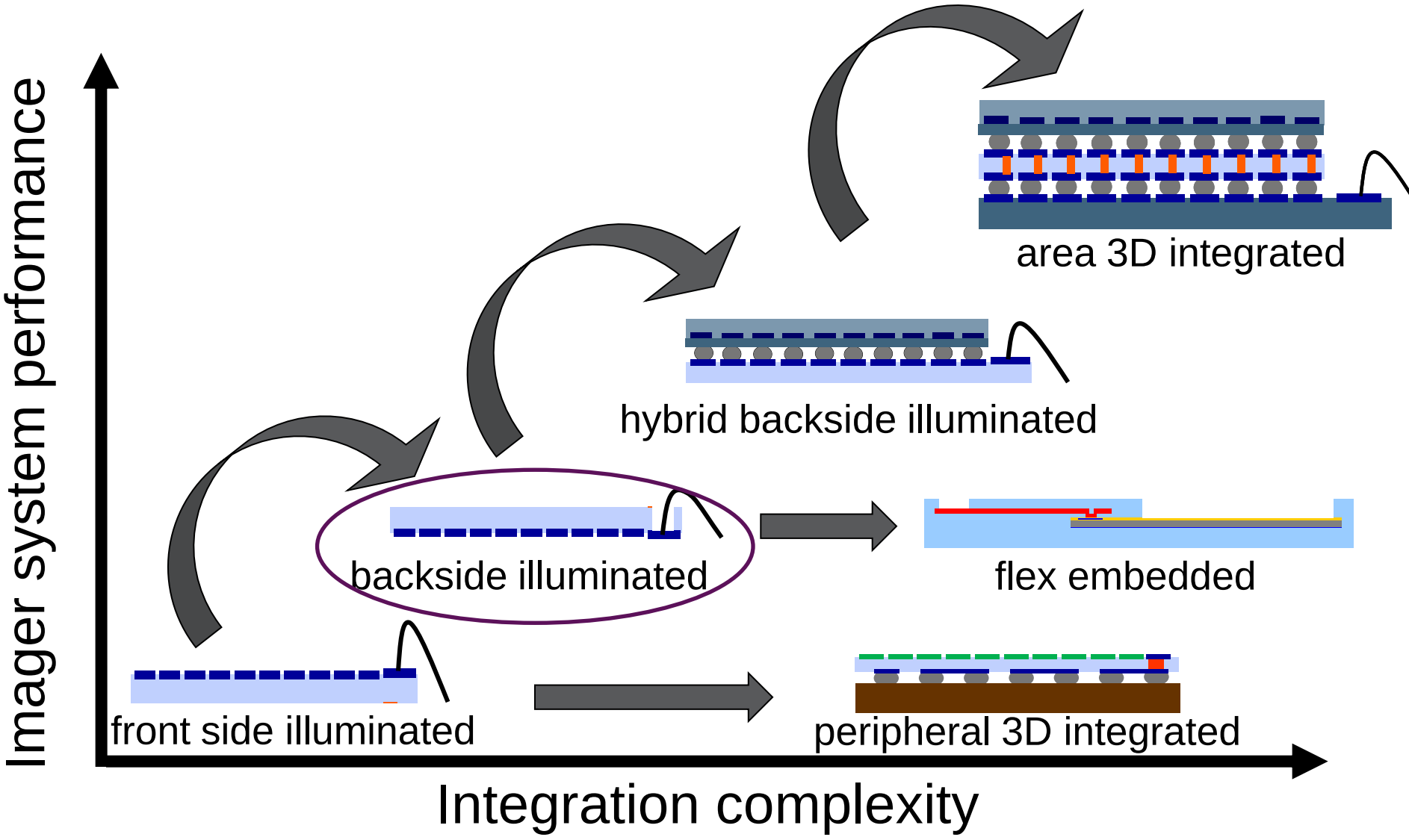
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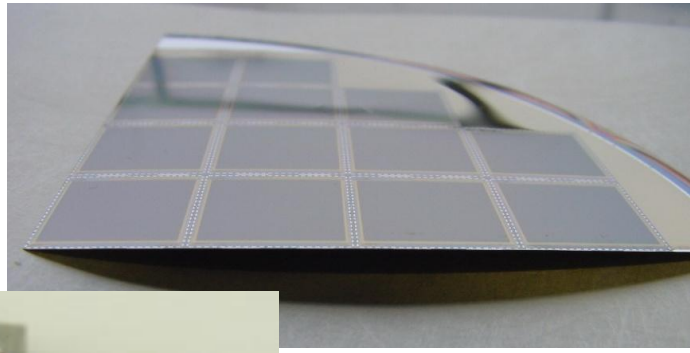
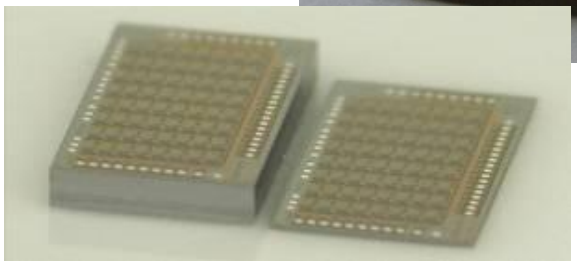
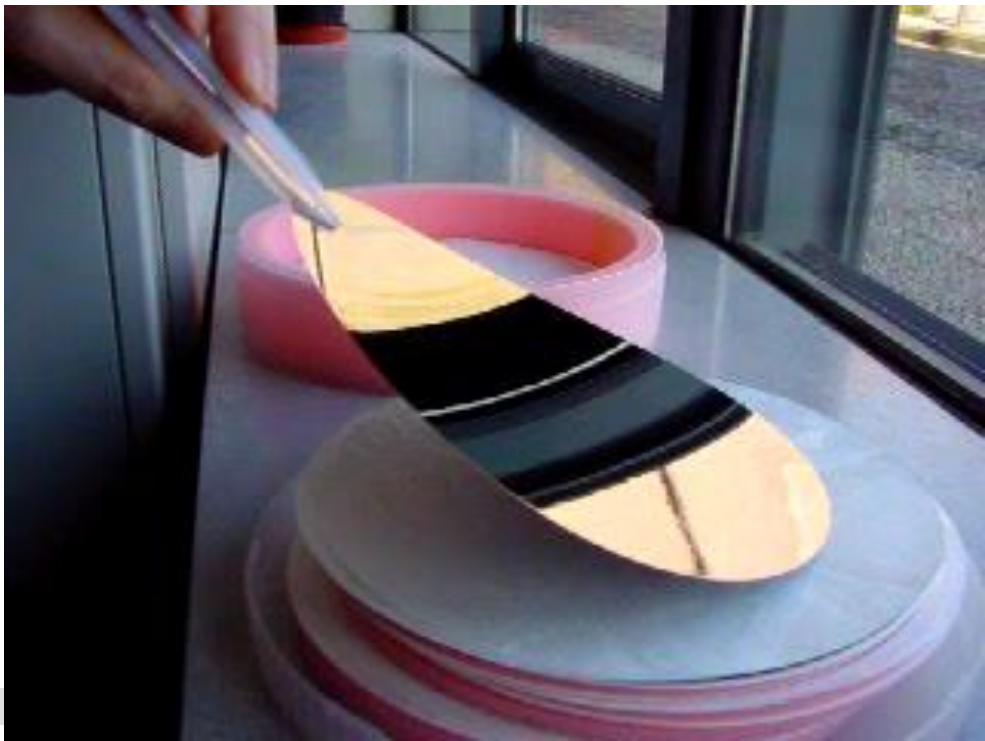
Integration complexity
front side illuminated
backside illuminated
hybrid backside illuminated
area 3D integrated
flex embedded
peripheral 3D integrated

BACKSIDE ILLUMINATED IMAGERS: THINNING

- Technology:
  - Course + fine grinding
  - Critical: thinning damage, impact on devices
- Wafer handling:
  - Very thin wafers (< 100 um): use of carrier wafers and temporary wafer (de-)bonding technology
- IMEC results:
  - Thinning down to 15 um
  - Total thickness variation ~ 2 um on 200 mm wafer

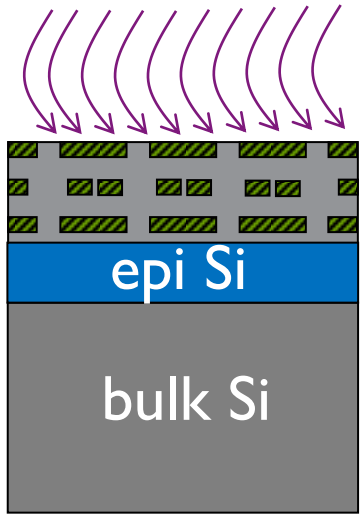




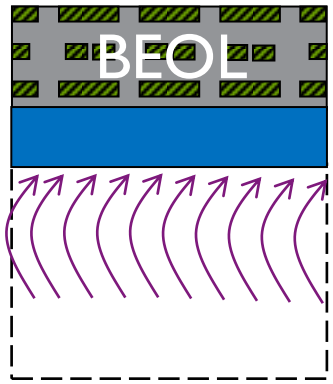


BACKSIDE ILLUMINATED IMAGERS:

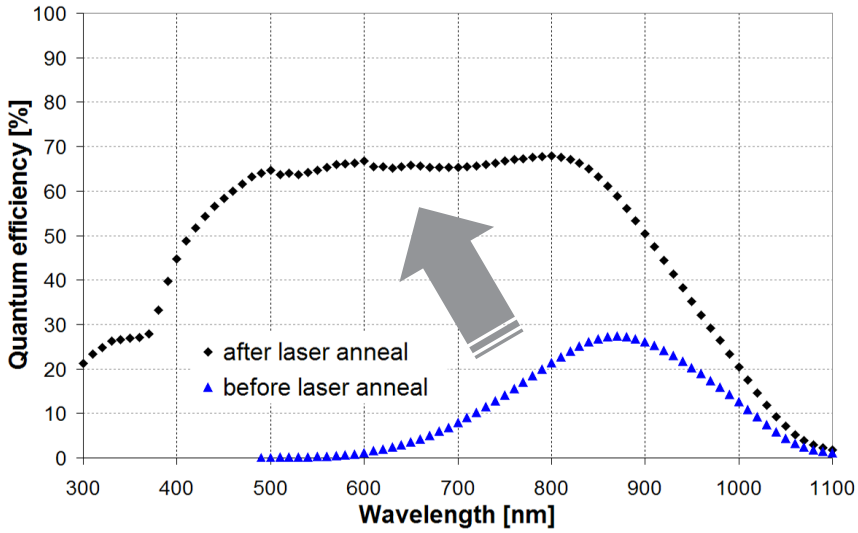
- Advantage: no dielectric/metal in light path:
  - 100% fill factor,
  - No QE loss
  - Broader wavelength range (i.e. in UV)
- Technology:
  - Backside thinning + damage removal:
    - Combination of grinding and Si etch
  - Backside passivation of trapping centers:
    - High dose implant
    - Laser annealing (for low T budget)



frontside illuminated

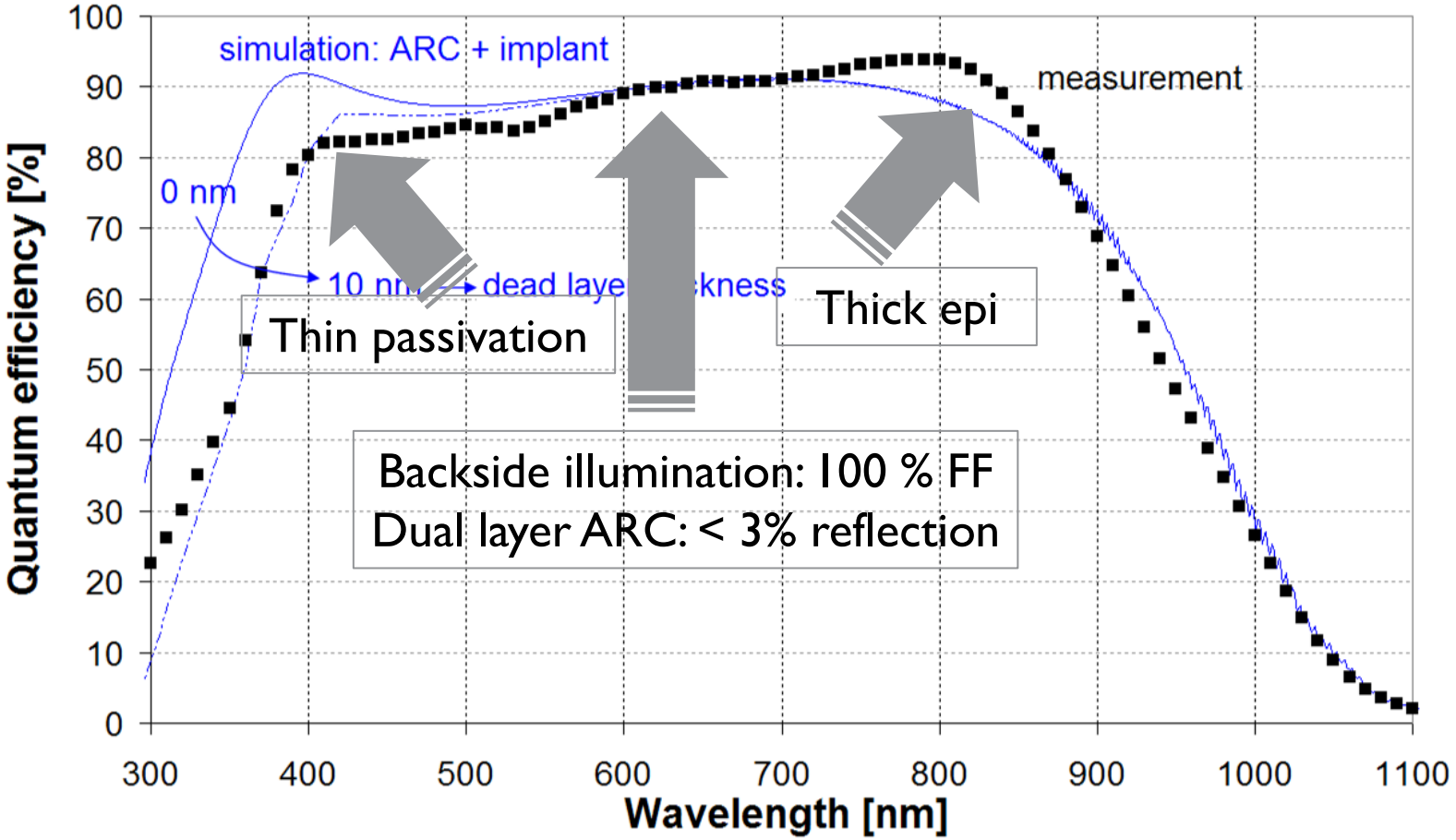


backside illuminated



BACKSIDE ILLUMINATED IMAGERS:
HIGH SENSITIVITY = HIGH QUANTUM EFFICIENCY

- World record broadband QE thanks to:



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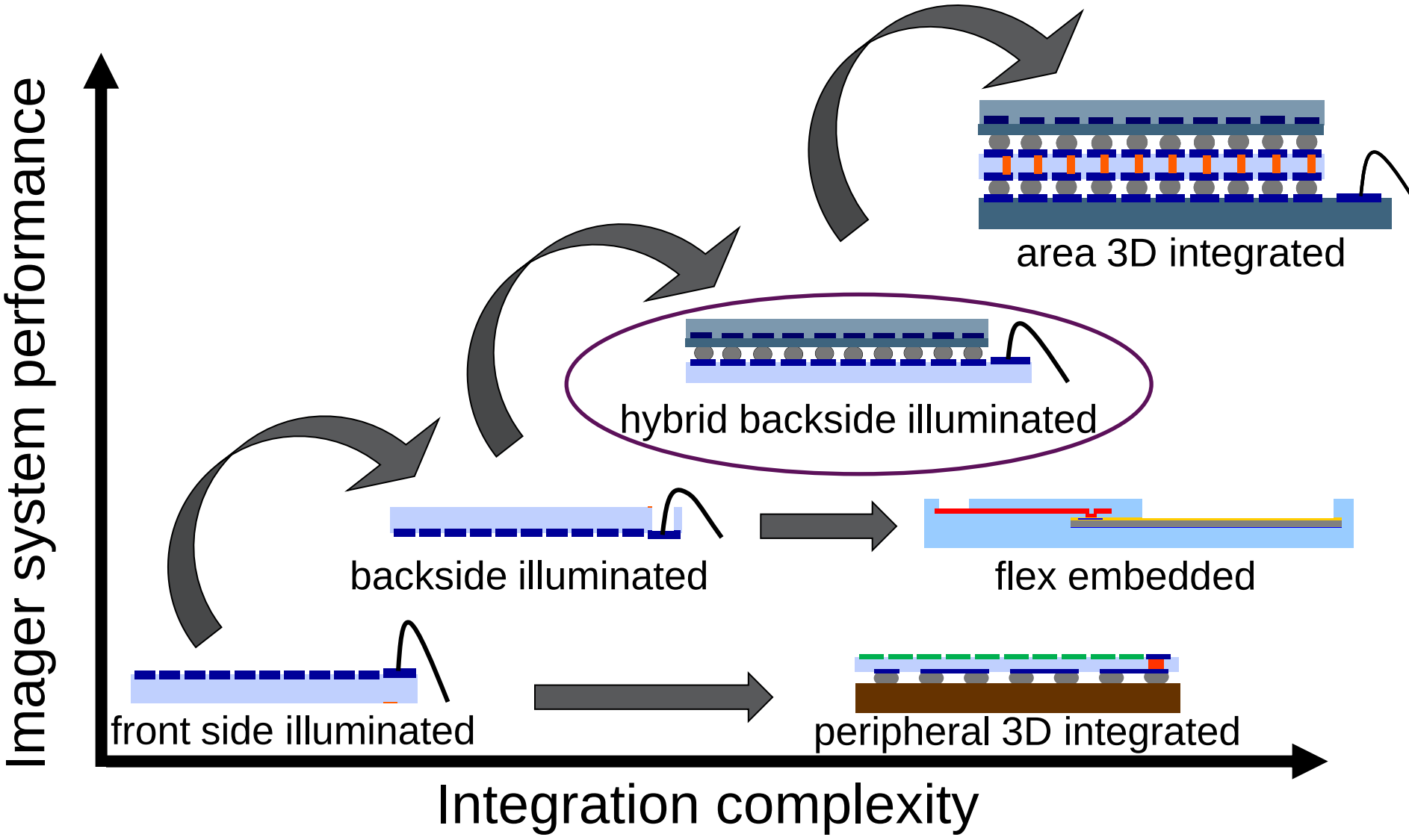
Imager system performance
Integration complexity
front side illuminated
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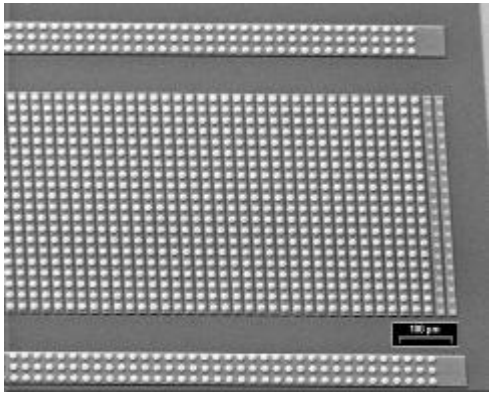
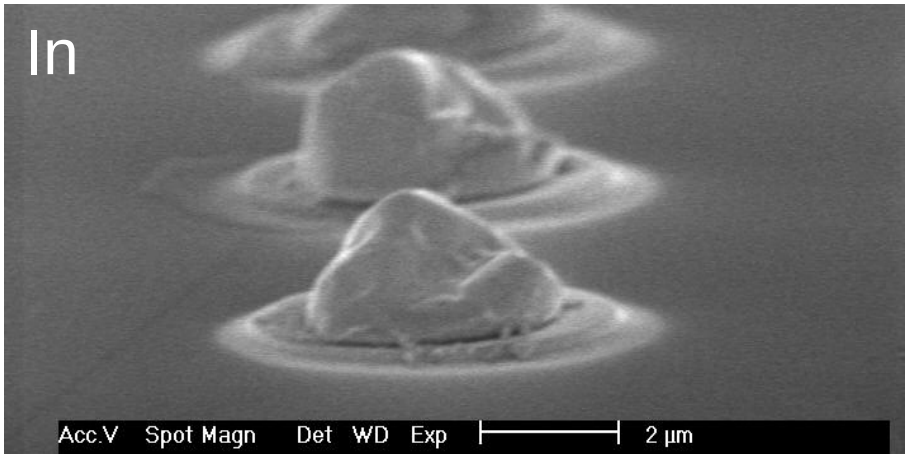
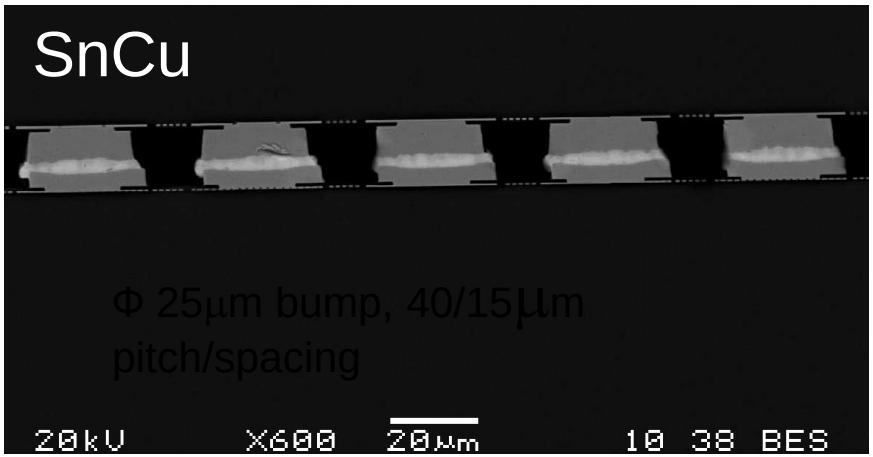
hybrid backside illuminated
area 3D integrated
flex embedded
peripheral 3D integrated

HYBRID BACKSIDE ILLUMINATED IMAGERS: HIGH DENSITY BUMPING

- In and CuSn microbumps:
  - Post-process at wafer level for both sides:
    - Under-bump metallization (UBM) & patterning
    - Solder deposition & patterning
  - Smallest pitch:
    - 20 um
    - 10 um under development

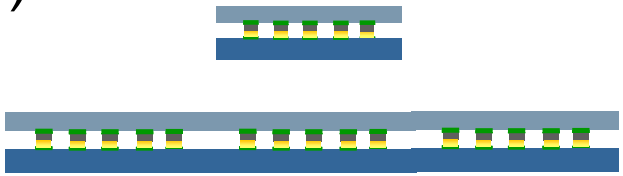


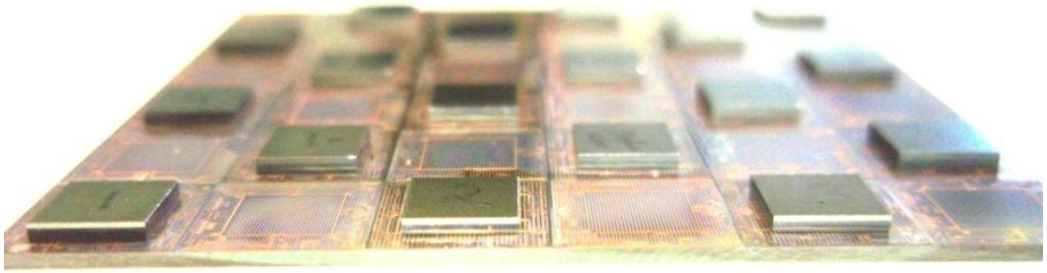


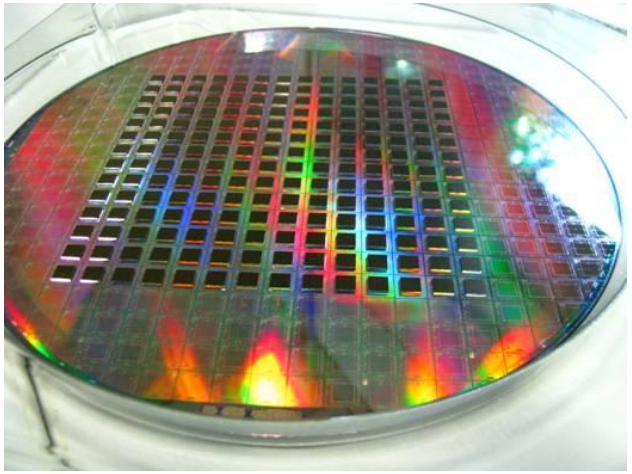


HYBRID BACKSIDE ILLUMINATED IMAGERS: HIGH DENSITY BUMPING

- Bonding:
  - Thermo-compression (high T and force)
  - Different options:
    - Flip-chip: D2D, D2W
    - Wafer bonding: W2W
    - Collective bonding: 1) populate D2W 2) W2W bonding + anneal
  - Specialty: bonding of thin dies/wafers (on carrier)

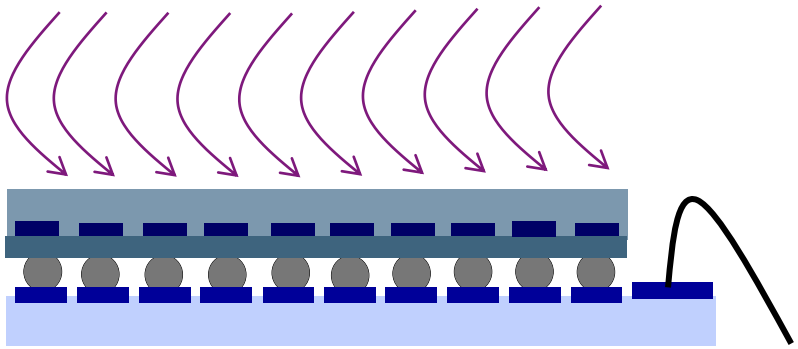






HYBRID BACKSIDE ILLUMINATED IMAGERS: HYBRID IMAGERS

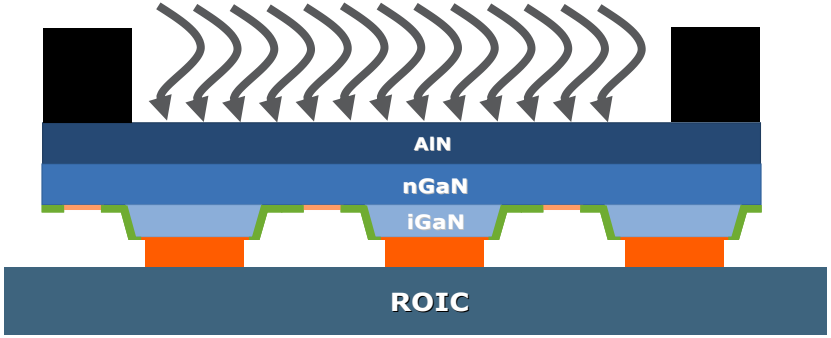
- Concept:
  - Face to face bonding using microbumps
  - 1 microbump per pixel
  - Top layer:
    - (typ.) passive photodiodes
    - Choice of materials: Si (ev. high res), InGaAs, CdTe, (Al)GaN, ... for specific wavelength range detection (X-ray, UV, visible, IR, ...)
  - Bottom layer:
    - CMOS read-out circuit (ROIC)

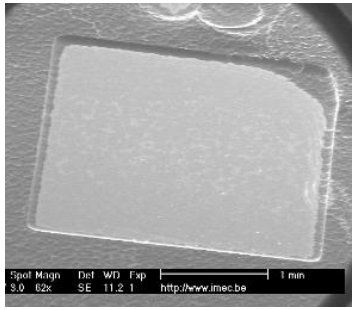


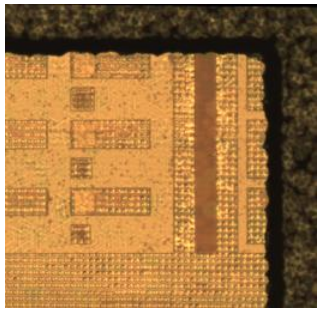
- Advantage:
  - Different wafer material and/or technology top vs. bottom allows separate optimization
- Disadvantage:
  - Pixel pitch limited to bump pitch

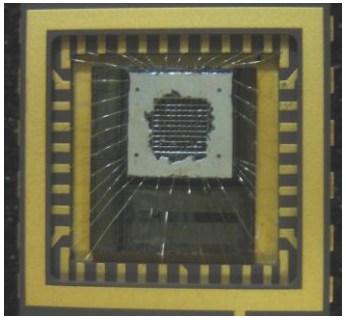
HETEROGENEOUS HYBRID IMAGERS:
(E)UV DETECTION USING ALGAN SCHOTTKY DIODES

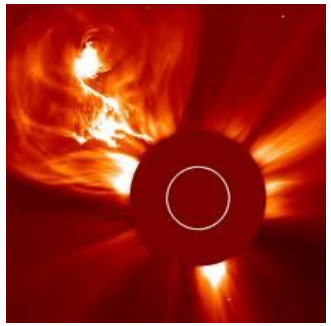
- Concept:
  - AlGaN growth on Si
  - Photodiode process
  - Flip-chip integration on ROIC
  - Backside etch of Si
    - Till membrane of < 1 um (!)
- Advantages vs. Si photodiodes:
  - Visible blind:
    - Due to large bandgap
    - Interest for e.g. sun observation
  - UV radiation tolerant
- Demonstration of 256x256 10 um pitch imager





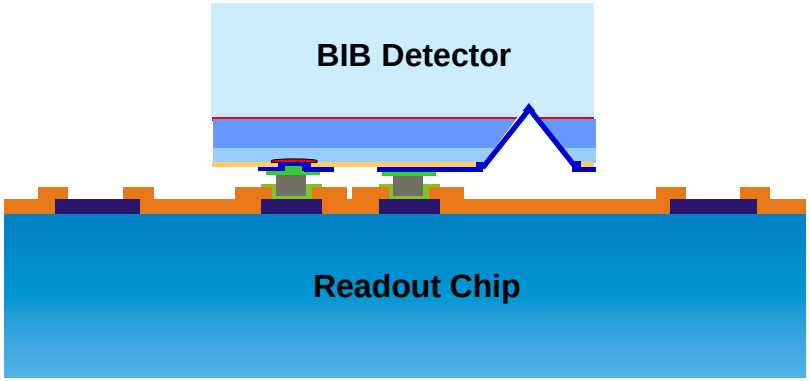


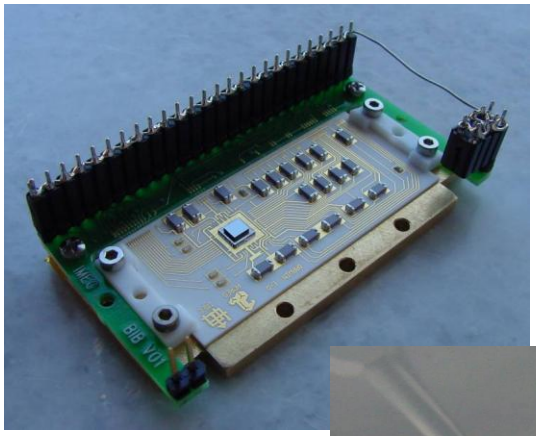


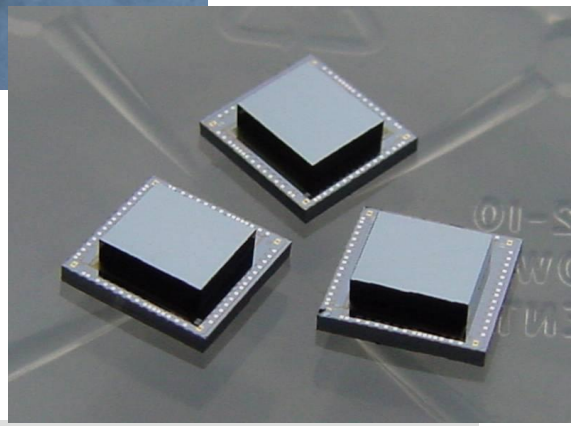


HETEROGENEOUS HYBRID IMAGERS:
FAR IR DETECTION USING CRYOGENIC BIB DETECTORS

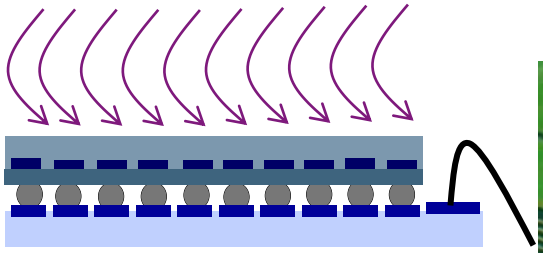
- Far IR detection (6-18 um)
- Concept:
  - Si:As Blocked Impurity Band (BIB) detector array operating at 4 Kelvin
  - Backside illuminated through high resistivity Si
  - Dedicated epi stack growth on Si
  - Contact process for buried contact and individual pixel
  - Flip-chip integration on cryogenic ROIC
  - In microbumps (for ultra-low temperature)
- Demonstration of bilinear array: 2x 88 pixels @ 30 um pitch
- Application: DARWIN mission:
  - Exoplanet atmosphere analysis

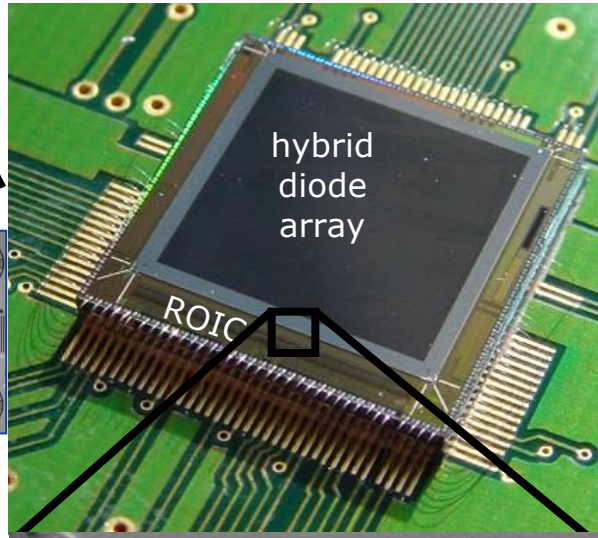




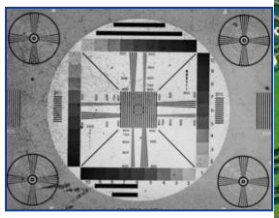


SI HYBRID IMAGERS FOR VISIBLE DETECTION: 'HYBRID APS'

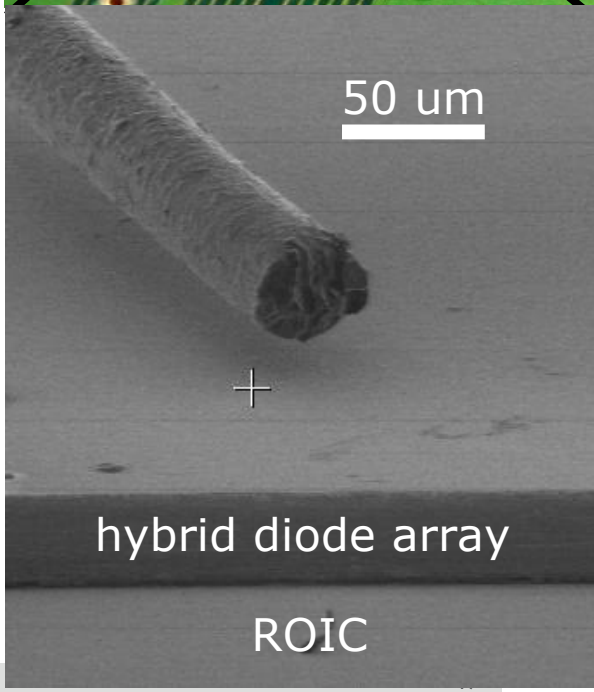


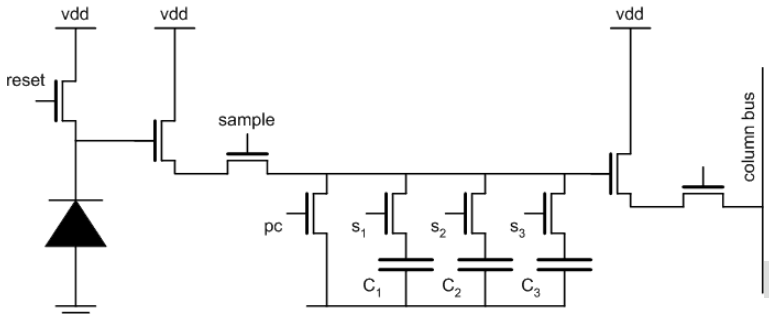


- Specifications:
  - 22.5 um pitch
  - Stitched design: 512x512, 1024x1024
  - **QE> 80% from 400 – 850 nm**
  - Thick epi: final thickness ~ 35 um



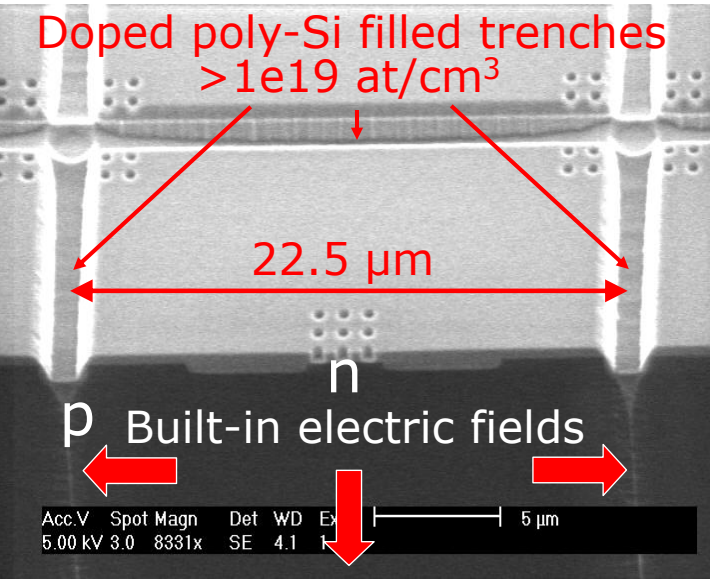
- ROIC designed by FillFactory/Cypress, fabricated in CMOS 0.35um foundry process:
  - **Snapshot**: synchronous pipelined shutter using 3 analog storage capacitors
  - On-chip Correlated Double Sampling (CDS)

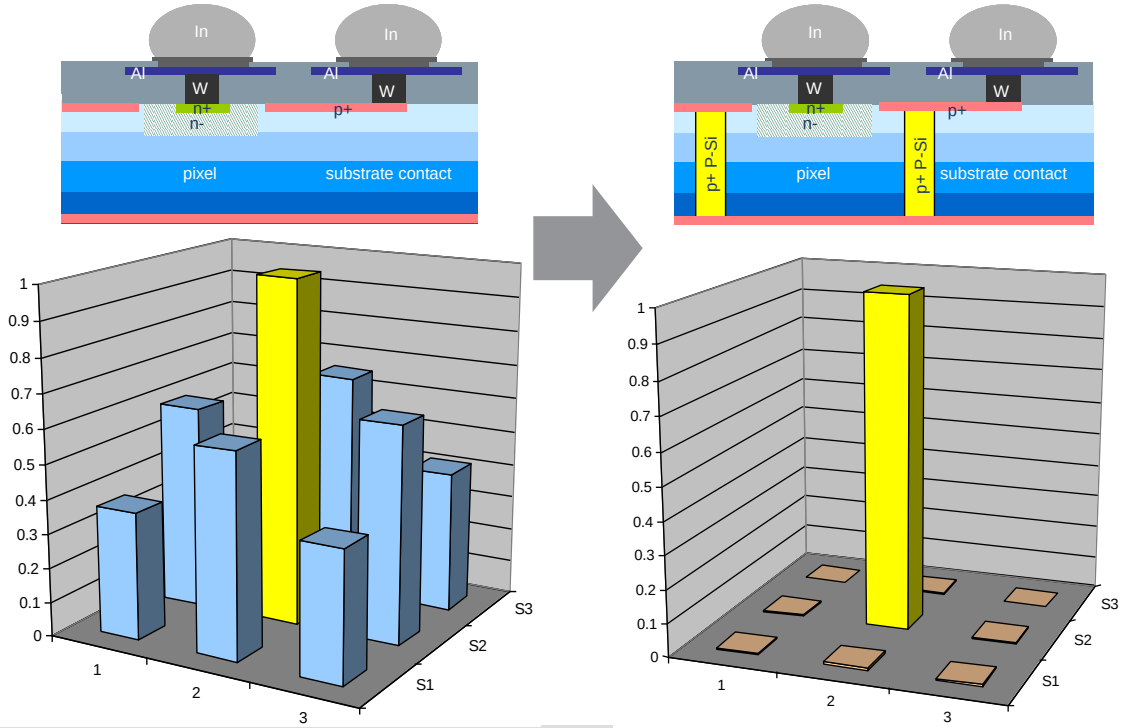




HYBRID BACKSIDE ILLUMINATED IMAGERS : TRENCHES FOR ZERO CROSS-TALK

- Poly-Si doped trenches separating pixels:
  - Disadvantage: (limited) reduction in fill-factor
  - Advantage: no cross-talk
- Demonstrated using laser point source





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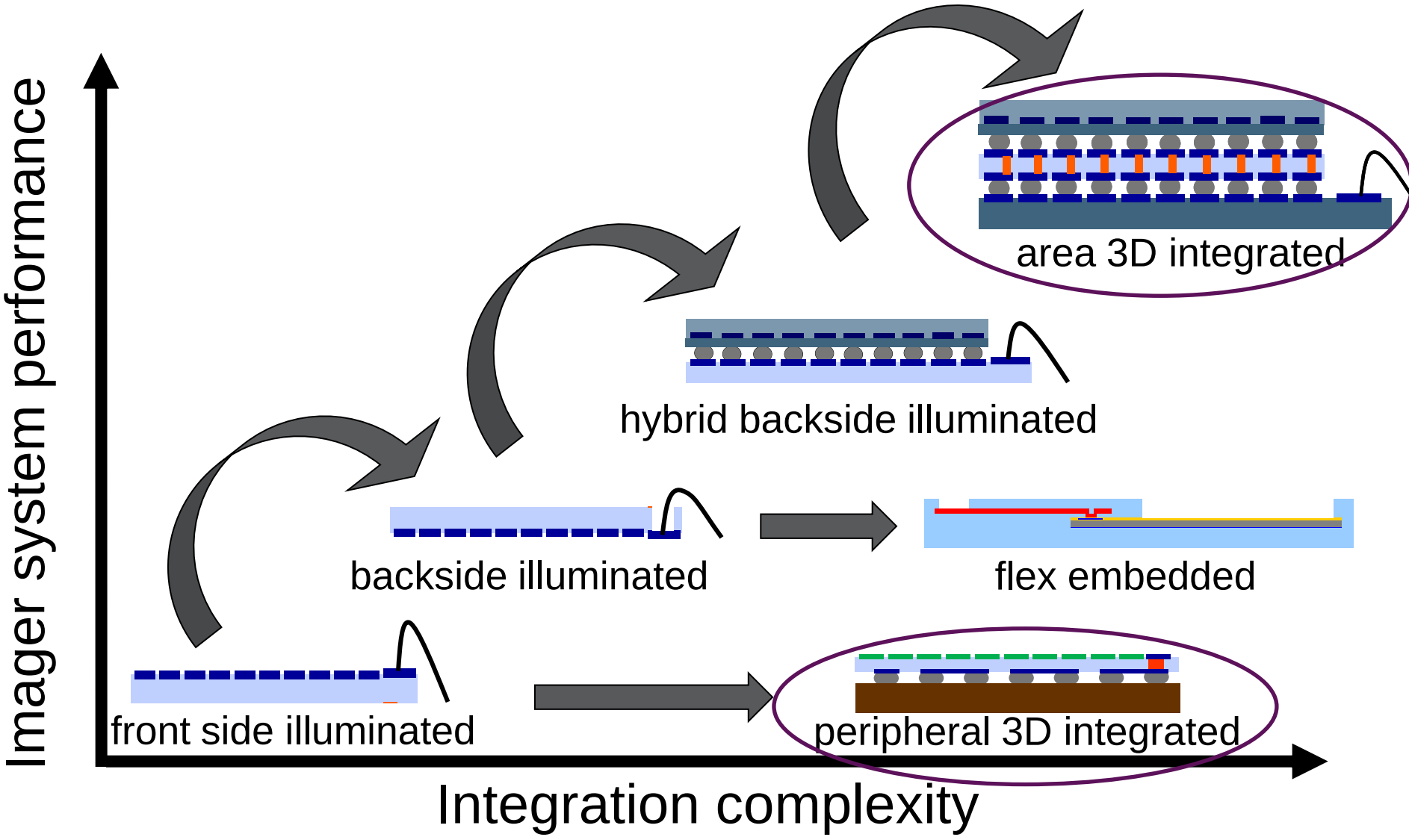
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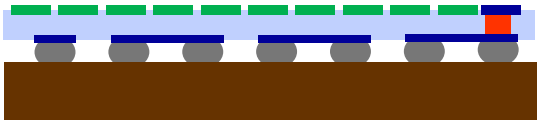
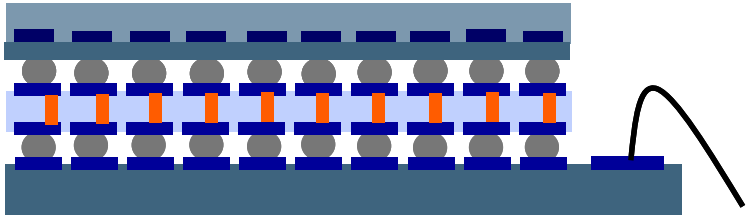
3D INTEGRATED IMAGER TECHNOLOGY: INTRODUCTION

- = create vertical interconnect using combination of
  - Through-Si vias (TSVs)
  - High density microbuming





- Process sequence:

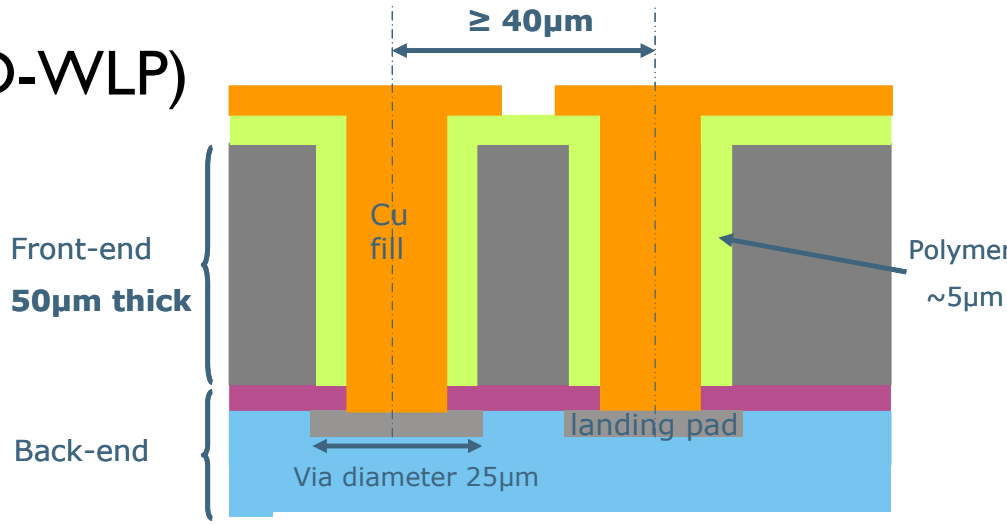
  1) Process TSVs and UBM/microbumps – on wafer level

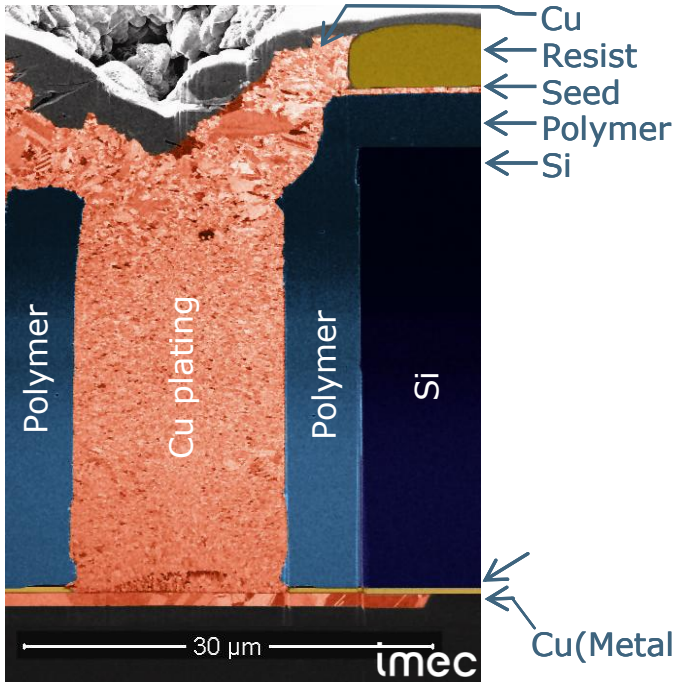
  2) Assembly – D2D/D2W/W2W

- 2 options for TSV process:
  - After finishing CMOS processing = post-processing
  - During CMOS process

3D INTEGRATED IMAGER TECHNOLOGY:
3D-WAFER LEVEL PACKAGING

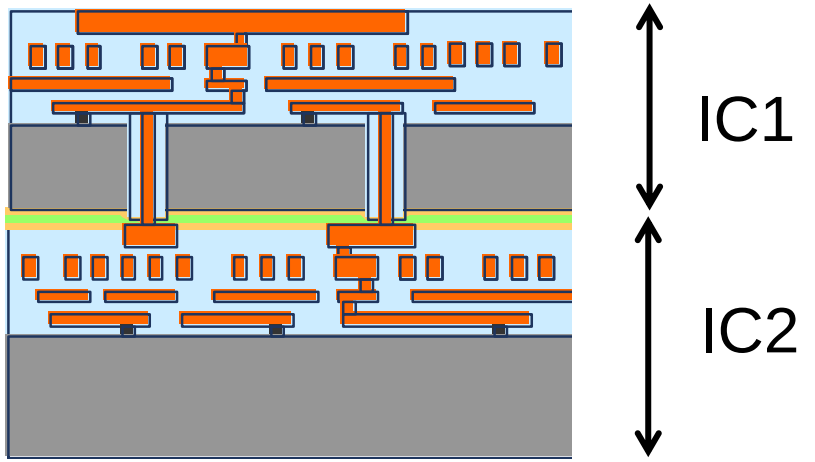
- 3D- Wafer evel packaging (3D-WLP) = post-processed TSVs
- Approach =
  - 1) Thinning
  - 2) TSV processing from the back
- Dimensions:
  - Minimal pitch = 40 um
  - Via diameter ~ 25 um
  - Si thickness ~ 50 um
- Via resistance < 20mΩ
- Low Capacitance: ~ 20 fF
- Design considerations:
  - Landing pad to be designed at lowest metal
  - Area consumption by TSV

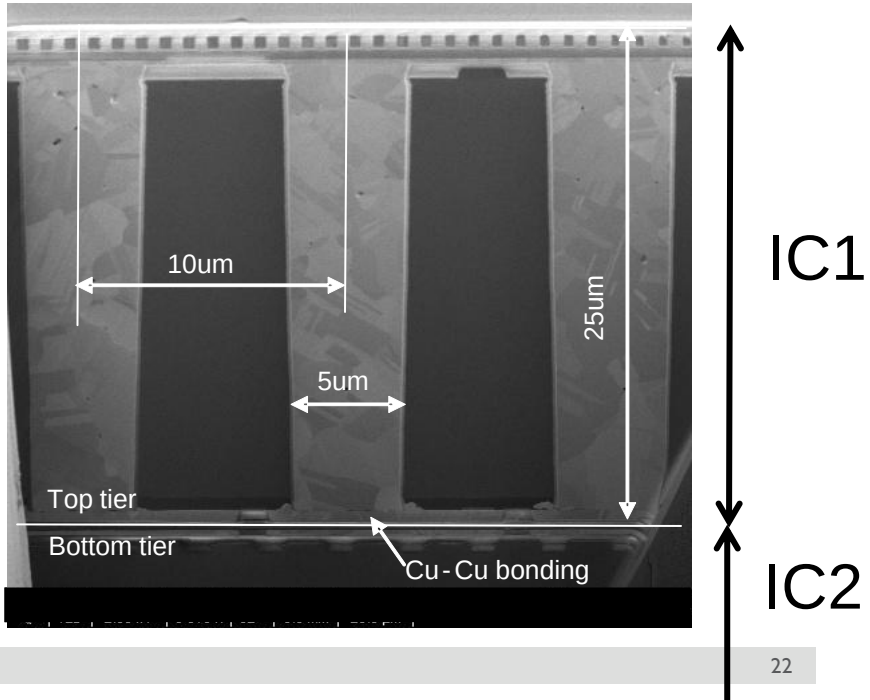




3D INTEGRATED IMAGER TECHNOLOGY: 3D STACKED IC (3D-SIC)

- 3D- Wafer level packaging = process TSVs as a part of the CMOS process:
  - At the level of the 1st metallization in the BEOL
  - Advantage: use of area above TSV
- Approach =
  - 1) CMOS process (incl. TSV)
  - 2) Thinning, TSV exposure, bonding
- Dimensions:
  - Minimal pitch = 10 um
  - Via diameter ~ 3-5 um
  - Si thickness ~ 15 um
- Via resistance ~ 20mΩ
- Via Capacitance: 40 fF (depletion)
- Design considerations:
  - Area consumption by TSV

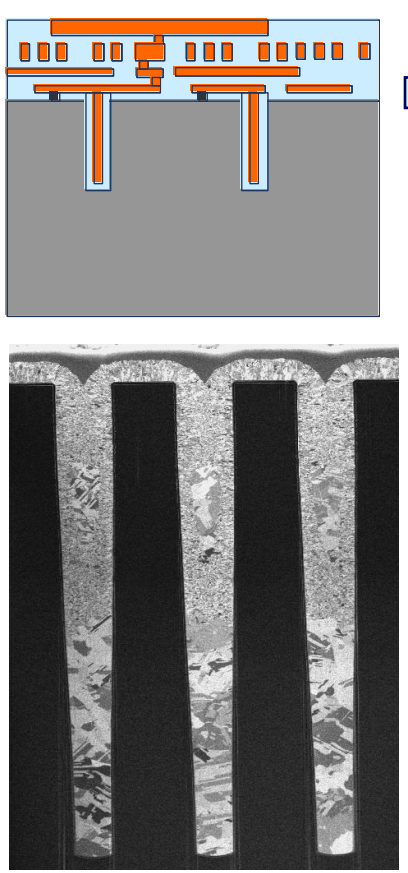


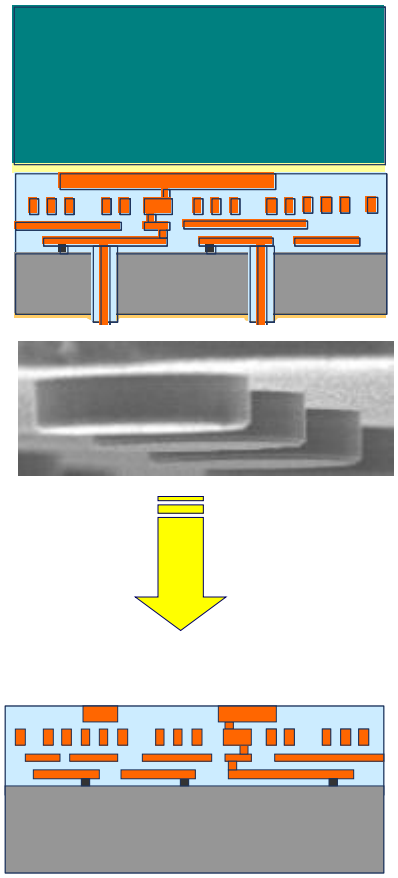


3D INTEGRATED IMAGER TECHNOLOGY: 3D STACKED IC (3D-SIC) PROCESS FLOW

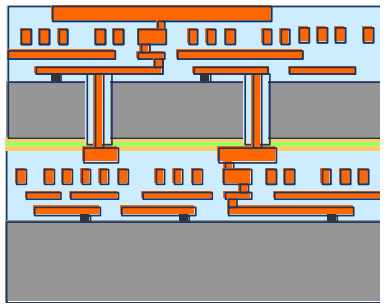
Via processing

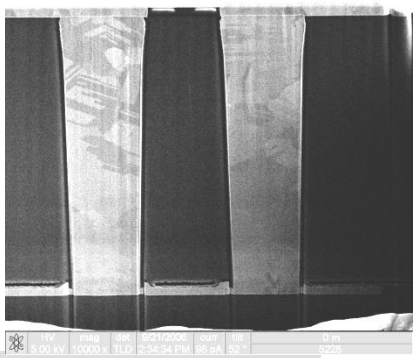
Extreme thinning
(on carrier)





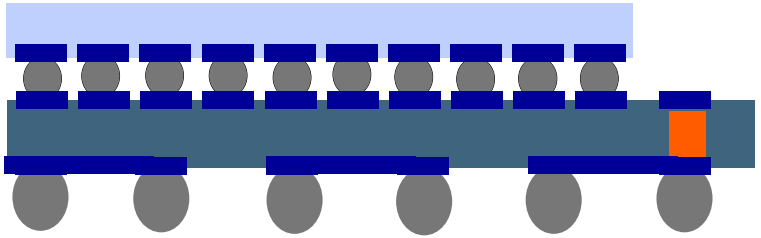
Mixed polymer and Cu-Cu
thermocompression bonding

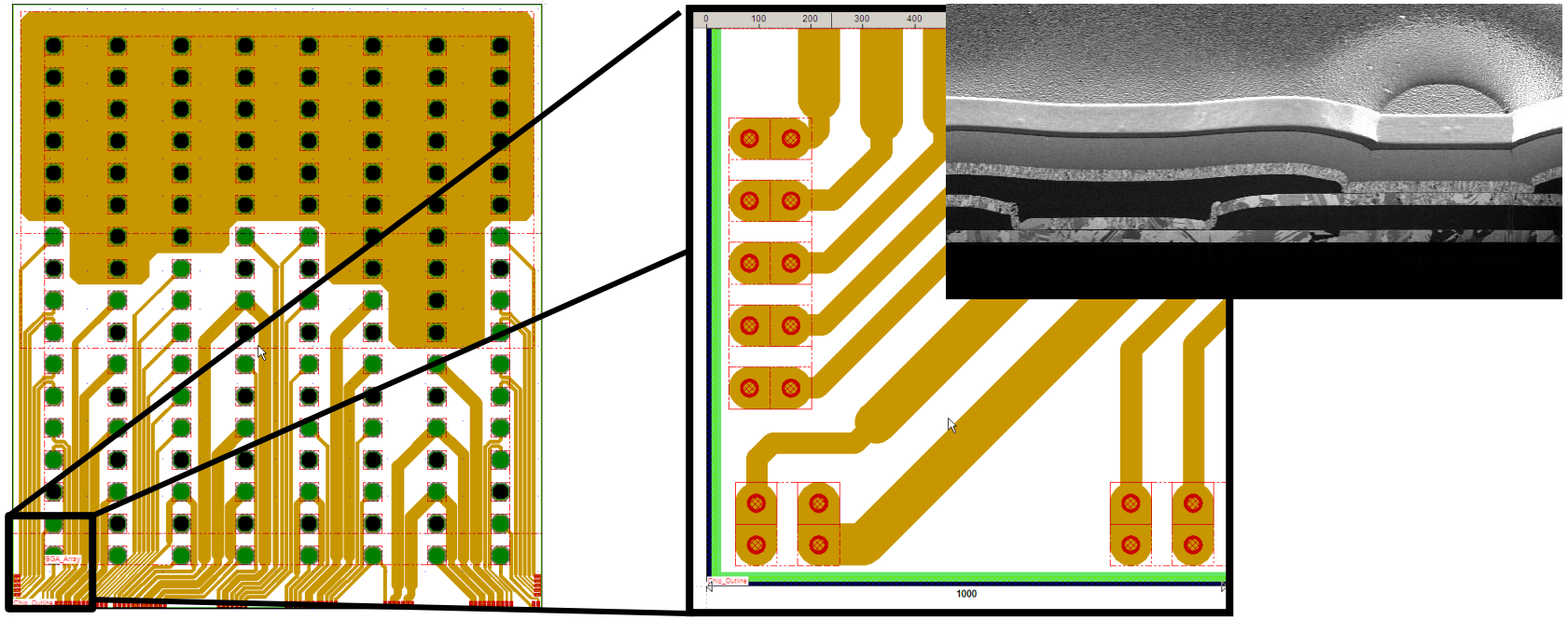




3D INTEGRATED IMAGER TECHNOLOGY: REDISTRIBUTION LAYER

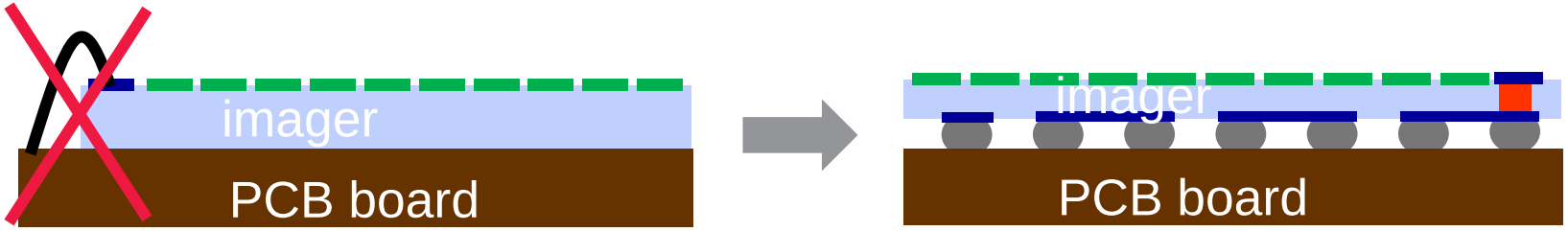
- Redistribution layer options:
  - Part of CMOS
  - At backside of (e.g.) TSV wafer
    - using e.g. Cu/dielectric





PERIPHERAL 3D INTEGRATED IMAGERS

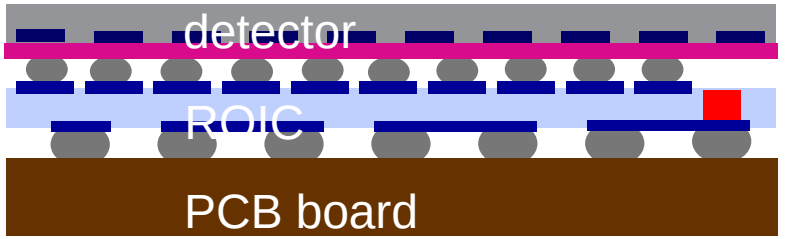
- Advanced packaging technology for front side illuminated imagers:
  - From traditional lateral wire bonding to TSV per bond pad + bump ball bonding
  - = 3D integration at package level using Through Si Vias (TSVs)

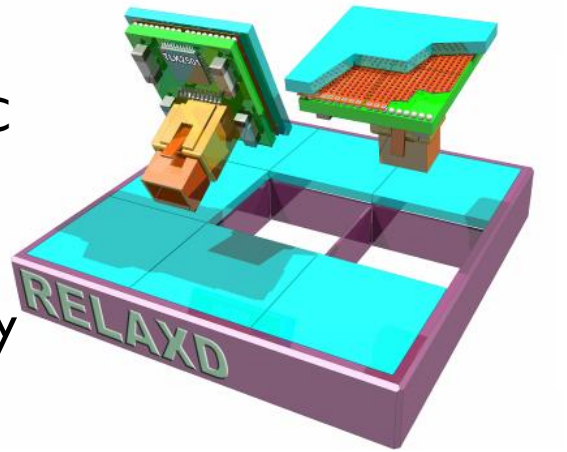


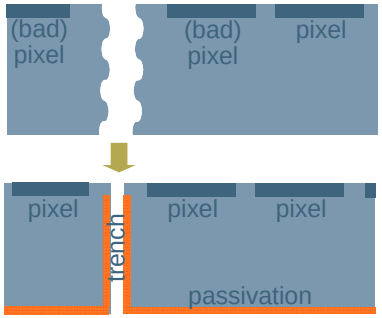
- Advantages:
  - Smaller footprint
  - Reduced capacitance → faster/low power interconnect
  - Buttability with mimimal area loss
- Applications:
  - Consumer imagers
  - Large area tiled imagers
  - Endoscopes

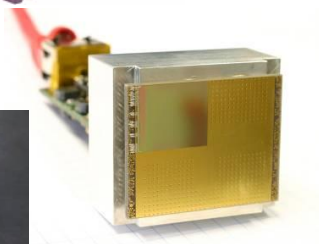
PERIPHERAL 3D INTEGRATED IMAGERS: LARGE AREA X-RAY DETECTION

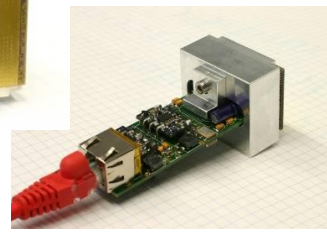
- Application: large area direct X-ray detection by **tiling**
- Concept:
  - **Vertical interconnect** architecture using
    - TSV at bondpad level in CMOS ROIC chip
    - Redistribution layer at backside
  - **Edgeless detectors** using dicing by grinding and sidewall passivation
- Status:
  - Standalone hybrid X-ray detectors realized
  - Demonstrator fabrication ongoing
  - System hardware ready



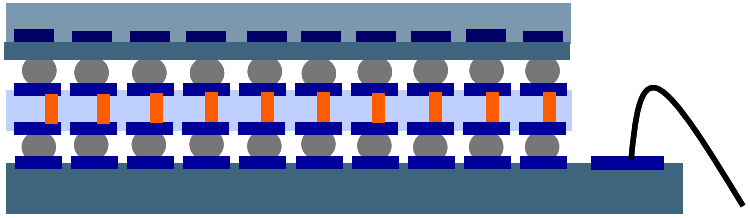








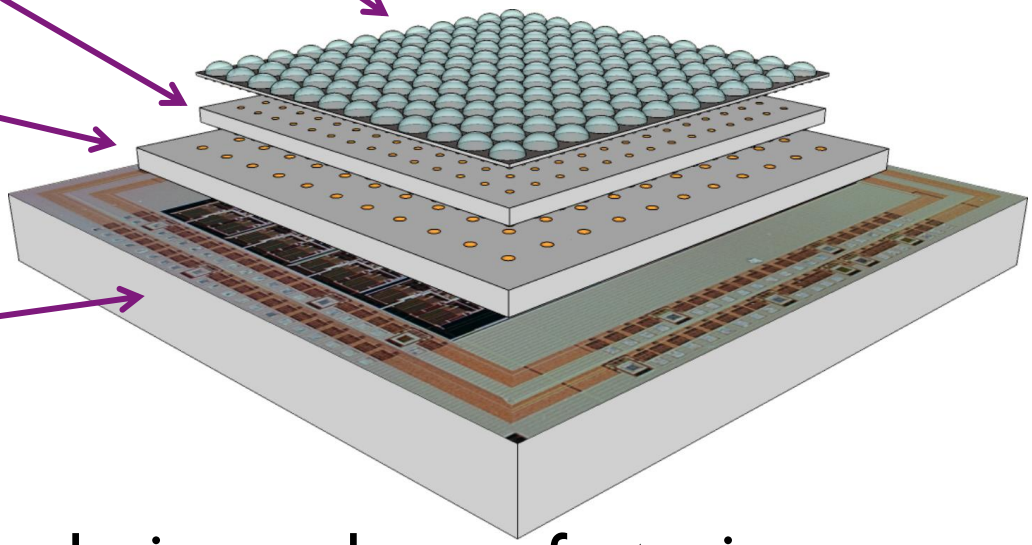
AREA 3D INTEGRATED IMAGERS



- Concept:
  - Stacking of multiple (>2) layers: detection layer + ROIC layers
    - Example: passive photodetector layer + analog ROIC + digital image processor
  - Using high density bumping + area redistributed TSVs
- Advantages:
  - General: optimization of (CMOS) technology for different layers
  - Imager system:
    - Vertical parallel readout chain allows high speed
    - Triple (n-fold) area per pixel allows complex electronics per pixel
    - Low capacitance interconnect to digital image processor allows high speed and low power
- Challenge: system architecture:
  - Optimal split in different layers of functionality and technology

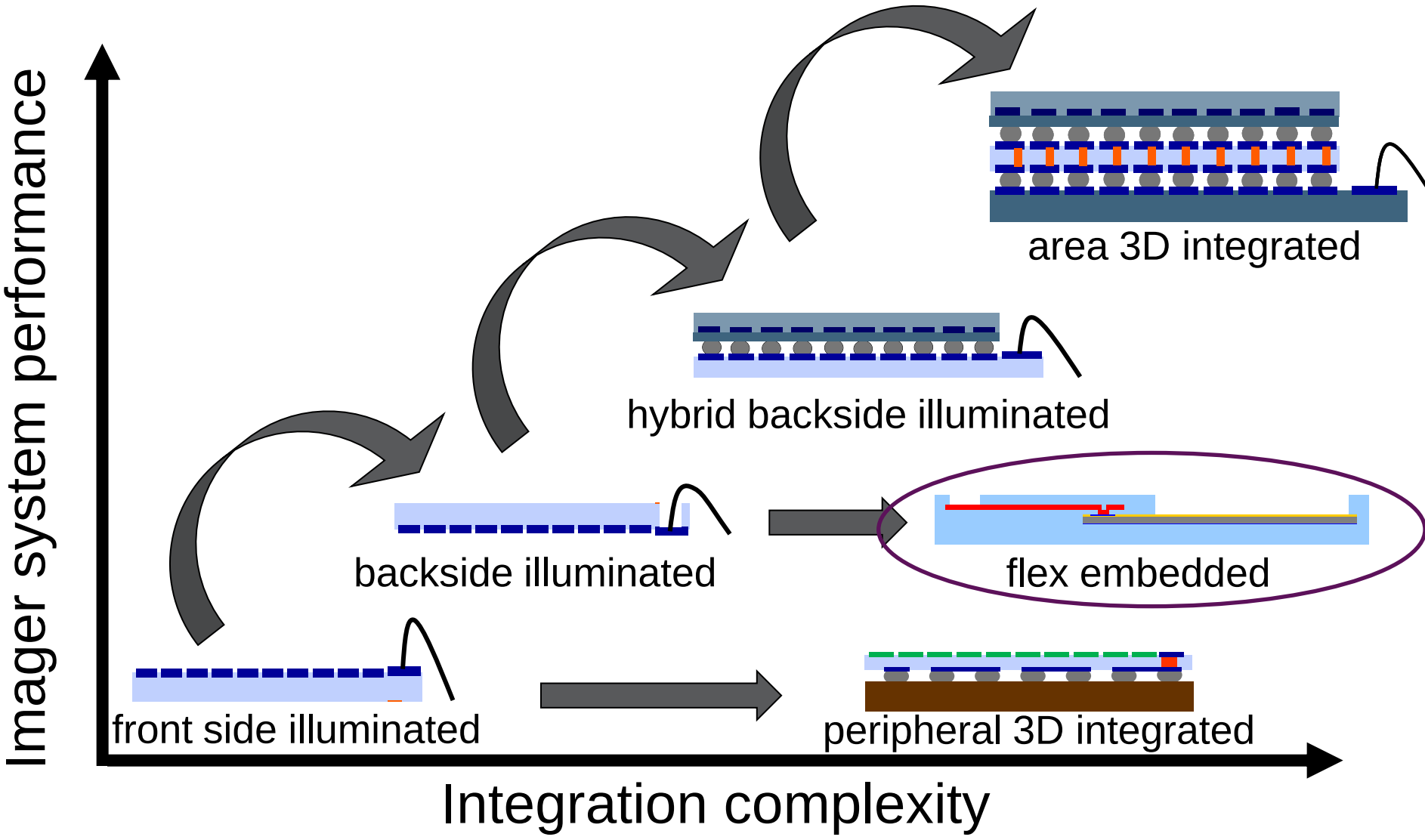
AREA 3D INTEGRATED IMAGERS

- Status: system architecture study of an **imaging system on a chip-stack**
  - Integration of micro-optics layer:
    - Ultra wide field of view
    - Filters for hyperspectral imaging
  - Shared pixels = multiple pixels per bump
  - Smart analog/digital read-out:
    - Ultra high dynamic range
    - ADC per group of pixels
    - Variable resolution (active binning)
  - Smart digital processing:
    - 2D distributed group of processors
    - Face recognition



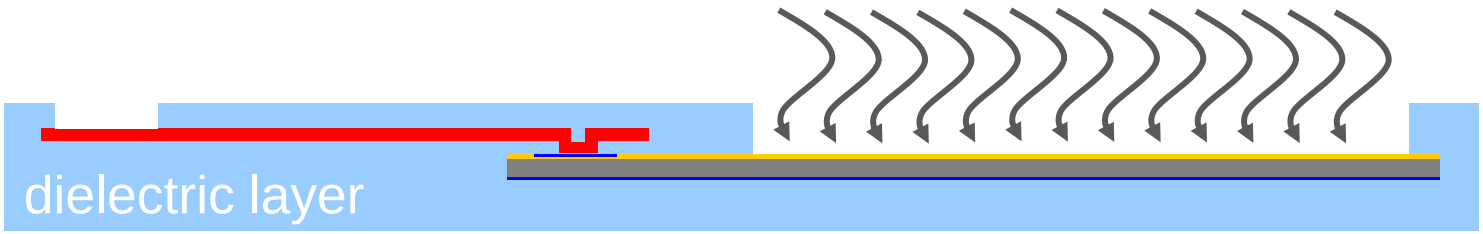
- Next step: demonstrator design and manufacturing

OUTLINE

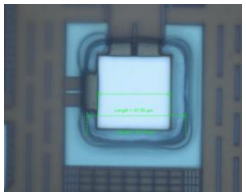

Imager system performance
Integration complexity
front side illuminated
backside illuminated
hybrid backside illuminated
area 3D integrated
flex embedded
peripheral 3D integrated

FLEX EMBEDDED IMAGERS

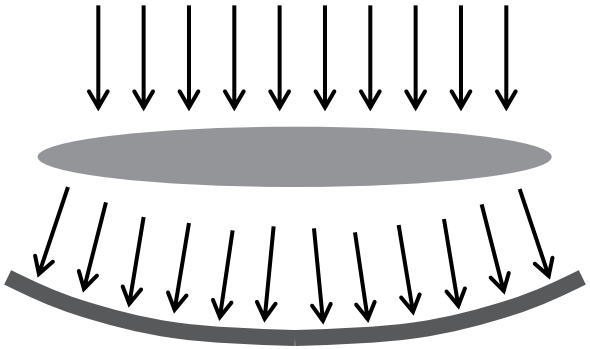
- Concept: embedding of a thinned imager in a flexible foil



- Status:
  - On-the-body demonstrator
  - Imager embedding ongoing



- Applications:
  - Non planar (bended) focal plane camera:
    - Low cost & optimized lens design
  - On/in the body radiation monitoring for cancer therapy
  - Tracking detectors for high energy particles



CONCLUSIONS

- Advanced 3D integration technology enables smart imagers with high performance
- The best integration scheme is application dependent
- imec has capabilities in:
  - Backside thinning and passivation
  - High density bumps
  - Through Si vias
  - Advanced assembly
- imec can offer development on demand up to small volume production (CMORE)

ASPIRE
INVENT
ACHIEVE

imec