

Radiation Pre-Evaluation of FPGA

ESTEC Contract No. 11407/95/NL/MV, CCN-3, COO-2

- SEL Testing of QuickLogic, Lattice and Lucent Technologies Devices
- TID Results on Actel RT54SX16
- SEE Results on Xilinx Virtex
- SET Results on LT1009 (Stanley)



Latch-up screening

FPGA Manufacturers

- LUCENT

- SRAM-based
- ORCA Series 2 family
- OR2C06A
- 16k System Gates
- TQFP-144
- $V_{CC} = 5.0V$

- LATTICE

- PROM-based
- ispLSI SuperWIDE family
- IspLSI5384VA
- 18k System Gates
- PQ-208
- $V_{CC} = 3.3V$

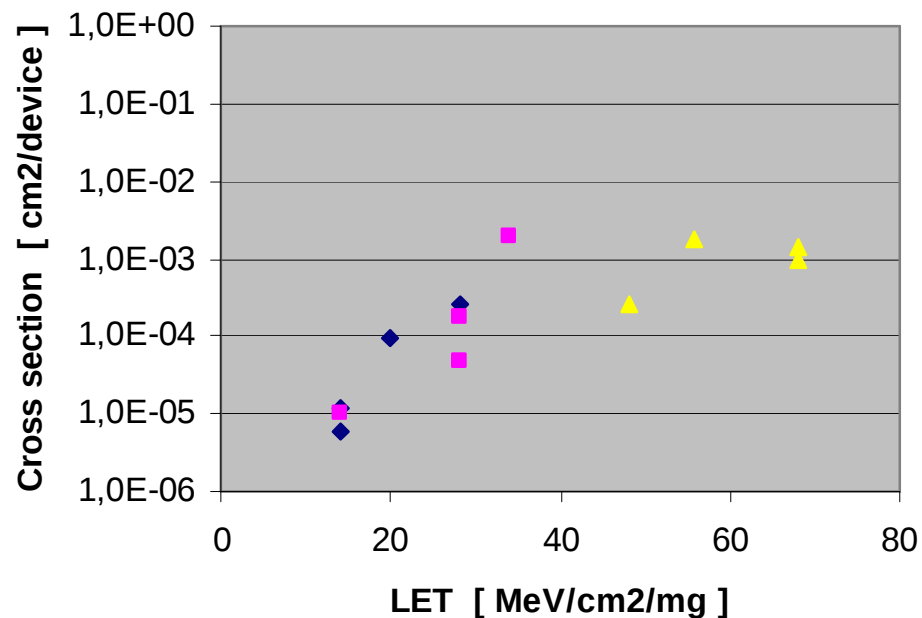
- QUICKLOGIC

- Antifuse
- QuickRAM ESP family
- QL4090
- 90k System Gates
- CQFP-208
- $V_{CC} = 3.3V$



Latch-up Results

All three Manufactures showed Latch-up



- ◆ QuickLogic
QL4090
- Lucent
OR2C06A
- ▲ Lattice
IspLSI5384VA

LET _{TH} MeV/mg/ cm ²	SEL σ _{SAT} cm ² / device
14,1	~3·10 ⁻⁴
14,1	~2·10 ⁻³
48	~2·10 ⁻³



Xilinx QPRO Virtex

- Radiation Hardened
- 0,22 μm 5-layer epitaxial process
- Total Ionizing Dose ~ 100 kRad
- Latch-up immune
- 300k / 600k / 1M System Gates
- SRAM-based in-system configuration

Test object - XQVR300

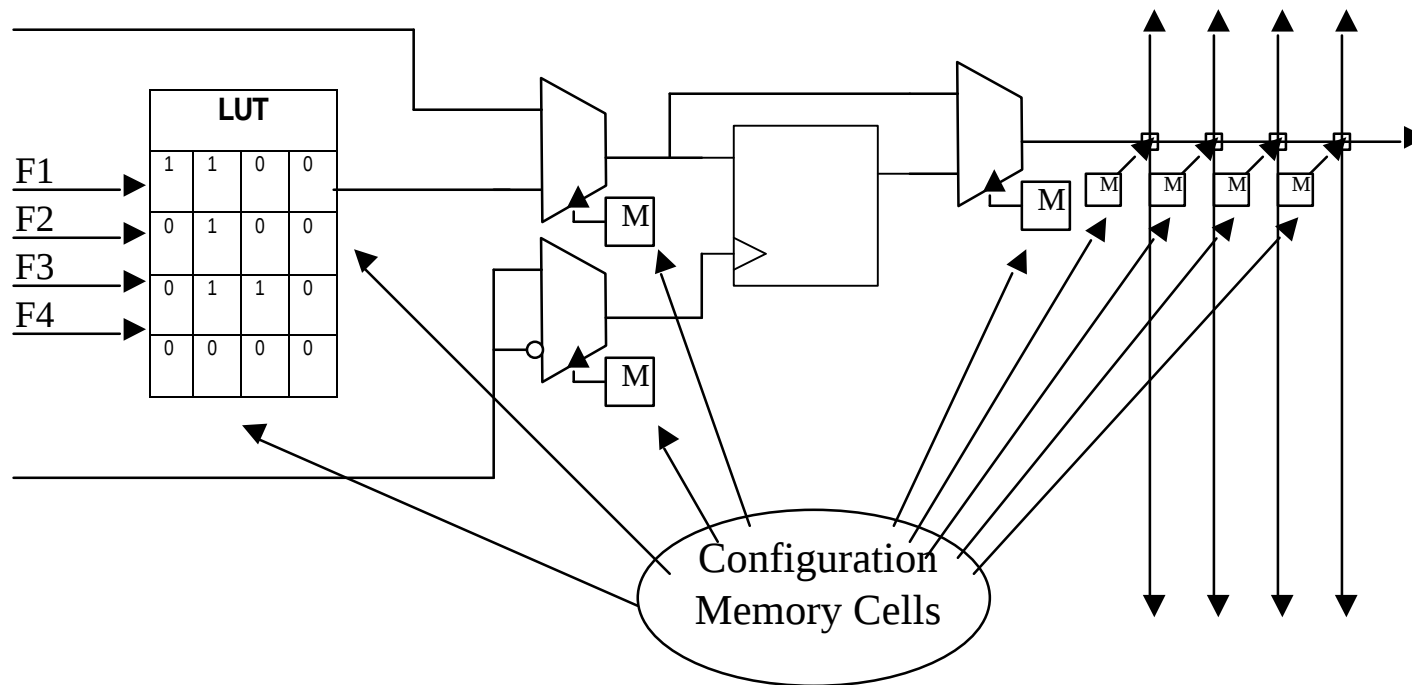
- 300k System Gates
- 6,912 Logic Cells
- 316 maximum available I/O

SEE test on Xilinx Devices

- Dynamic SEE tests
- Two designs
 - Non Redundant
 - One Chip Triple Module Redundant solution by Xilinx
- Scrubbing of device with configuration data



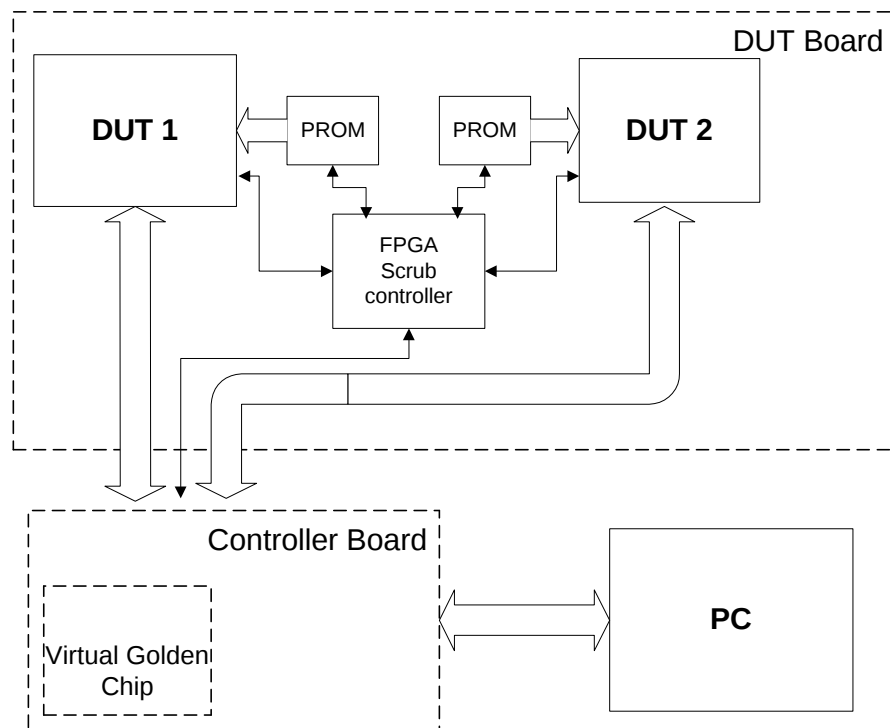
Single Event Upsets in Configuration Cells



- Reconfiguration in Operation



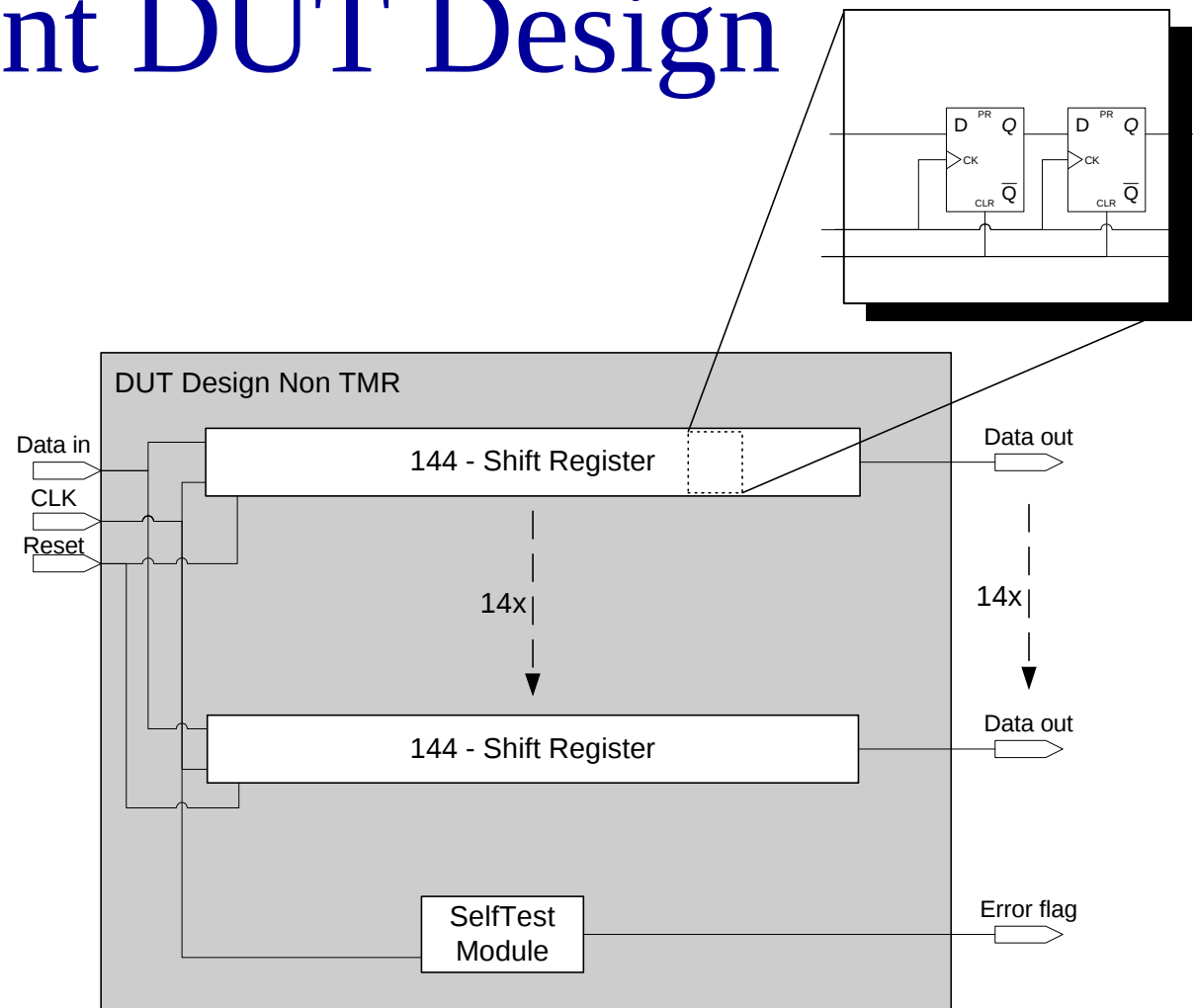
Test System



- Scrub DUT with configuration data
- Function Test of DUT by Virtual Golden Chip
- Error Data Analyzed in PC

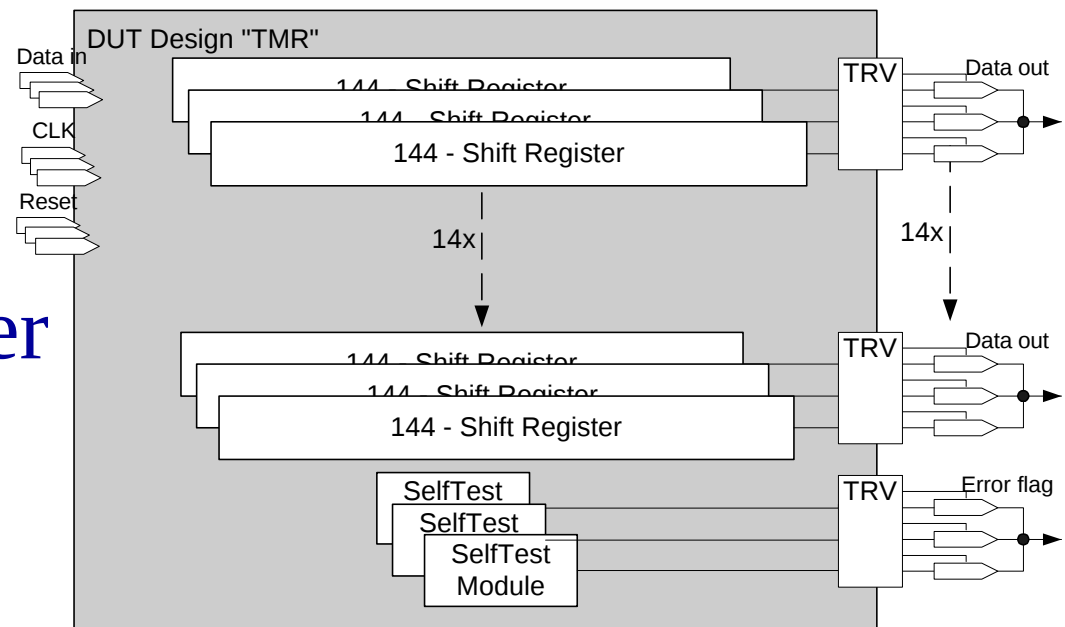
Non Redundant DUT Design

- 14 Shift-Registers
144 bits long
- 32 % usage of register cells
- 2 % usage of Look up Tables (LUT)
- 1 Self Test Module



Triple Module Redundant (TMR) DUT Design

- Same design, triple redundant
- Tripled In- and Outputs
- 98% usage of Register cells



Detected Error Types

Dynamic **"FF"**

- SEU in Flip-Flop Registers

"DataSwap"

- SEU in two Register cells adjacent to each other in the shift register

Corrected **"Routing"**

by

- SEU in Configuration Cell causing functional interrupt one Shift Register

scrubbing **"SelfTest"**

- SEU in Configuration Cell causing functional interrupt the Self-Test Module

Require
Reset
of
Device

"Persistent"

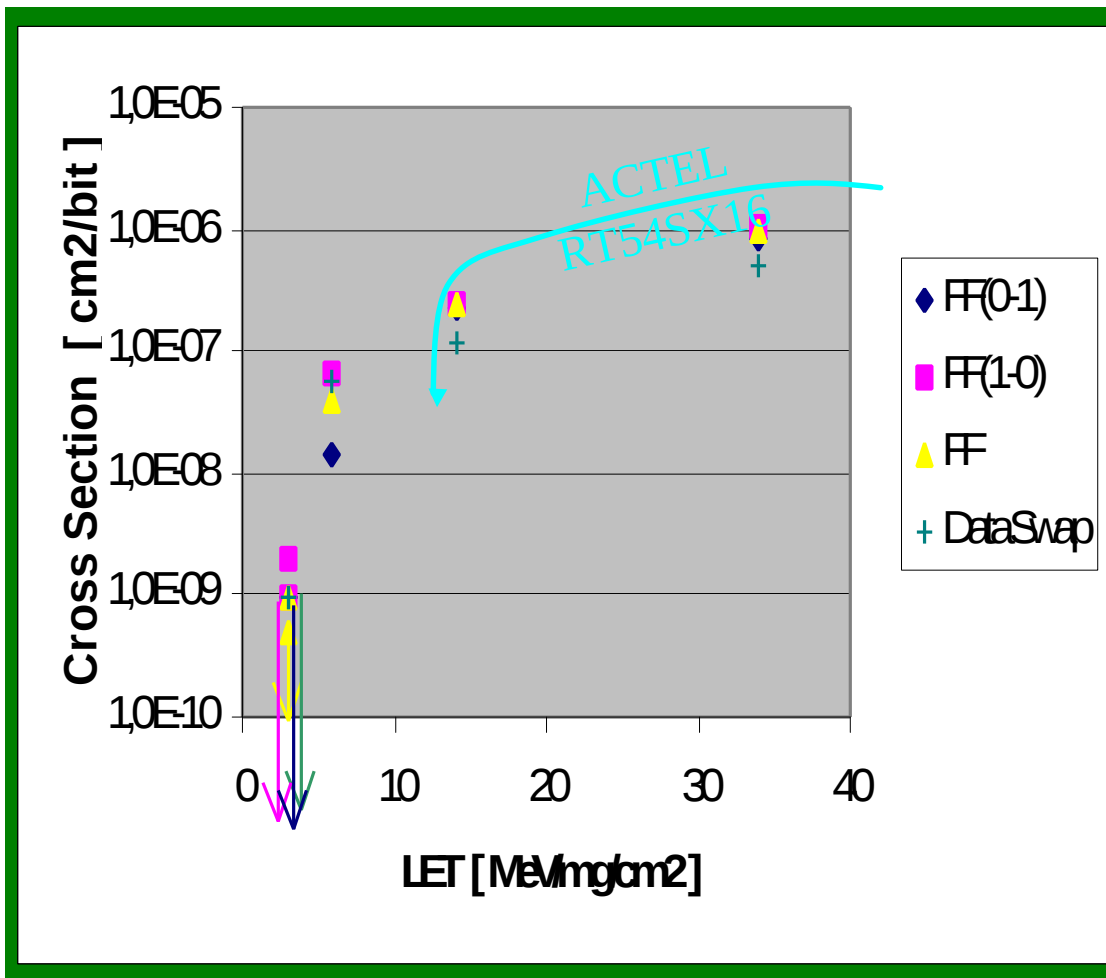
- Local interrupt of functionality.

"SEFI type"

- SEU in Control Register of Device, interrupt functionality of whole device



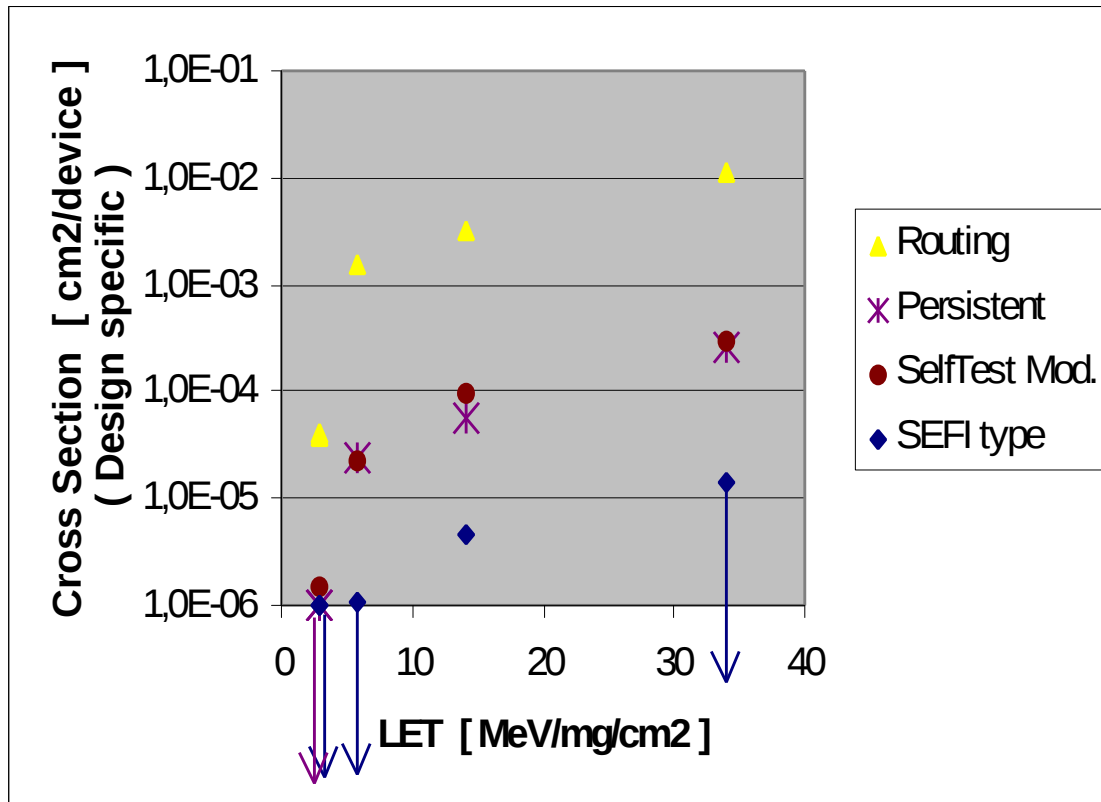
Non Redundant Dynamic



	LET _{TH} MeV/mg/ cm ²	σ _{SAT} cm ² / bit
FF	3-5,85	~1,0·10 ⁻⁶
DataSwap	~5,85	~7,0·10 ⁻⁷



Non Redundant Functionality



	LET _{TH} MeV/mg/ cm ²	σ _{SAT} cm ² / device
Routing	<2,97	~1,0·10 ⁻²
SelfTest	<2,97	~3,0·10 ⁻⁴
Persistent	>5,85	~3,0·10 ⁻⁴
SEFI type	>5,85	~1,0·10 ⁻⁶

Design Specific

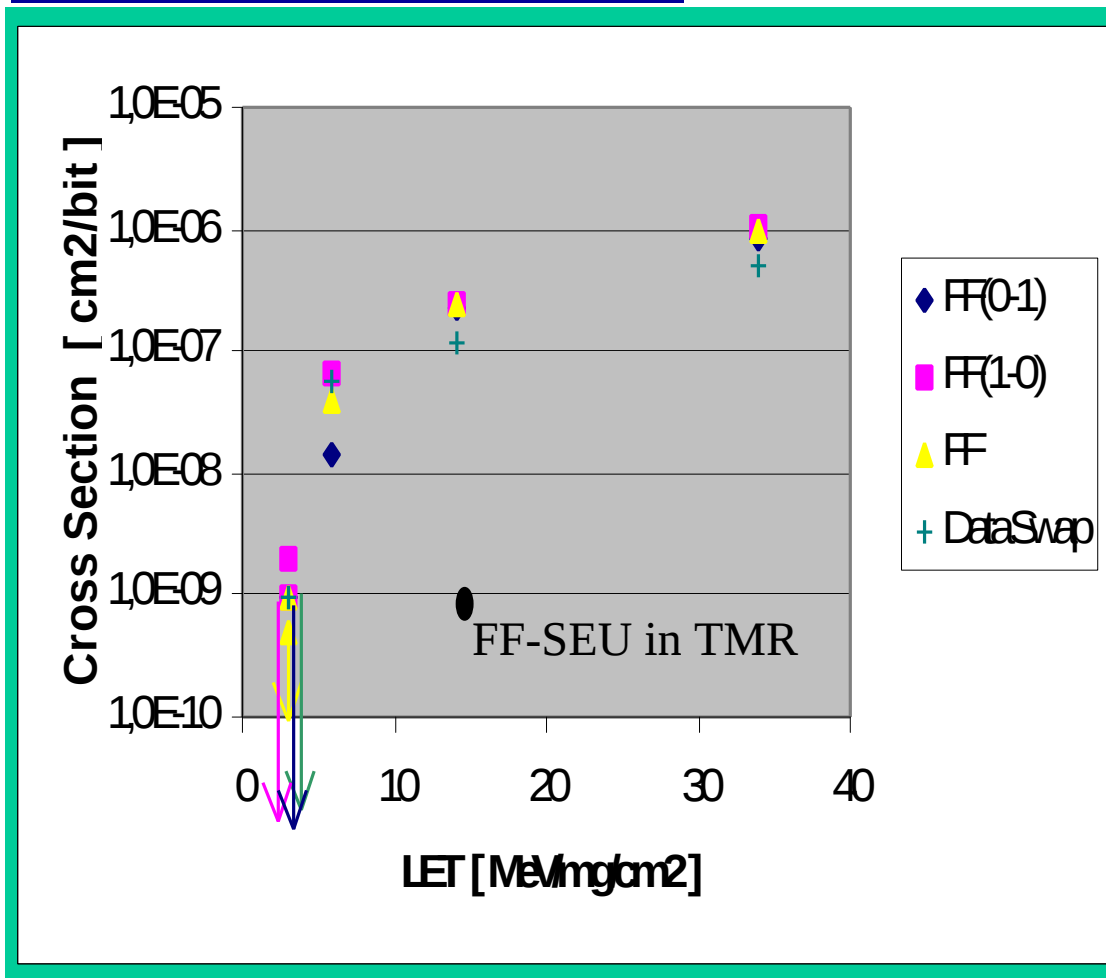


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Dynamic

Non Redundant

TMR



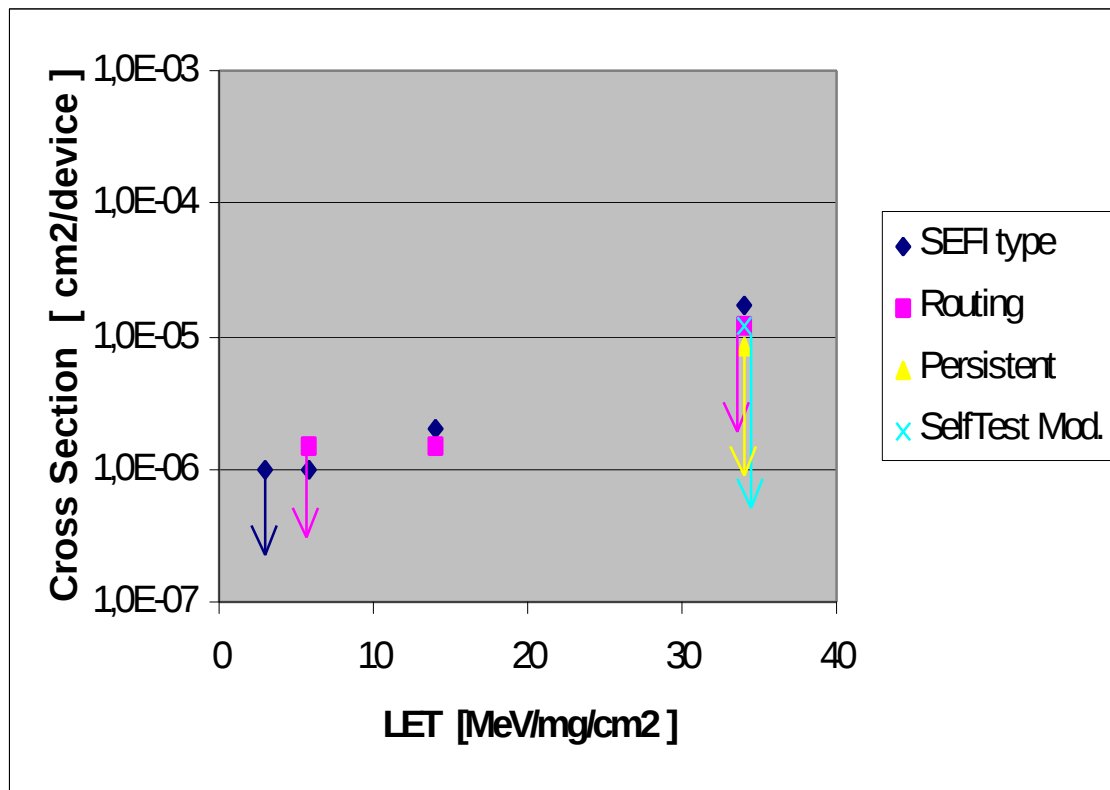
One Single SEU
(LET = 14,1 MeV/cm²/mg)

No Other Dynamic Errors
(10⁻⁶ ions/cm² for each ion)



TMR

Functionality



- No Persistent Error
- One Single Routing Upset
- Cross Section for SEFI errors $\sim 10^{-5} \text{cm}^2/\text{device}$



Summary

- TMR and scrubbing possible solution for SRAM-based FPGA
- GEO-orbit:
 $4 \cdot 10^{-5}$ Major Fails / day
- 1/3 usage of Available Gates and I/Os
- Restricted usage of Resources in Virtex

Impact of Test Conditions on TID Results for Commercial FPGA

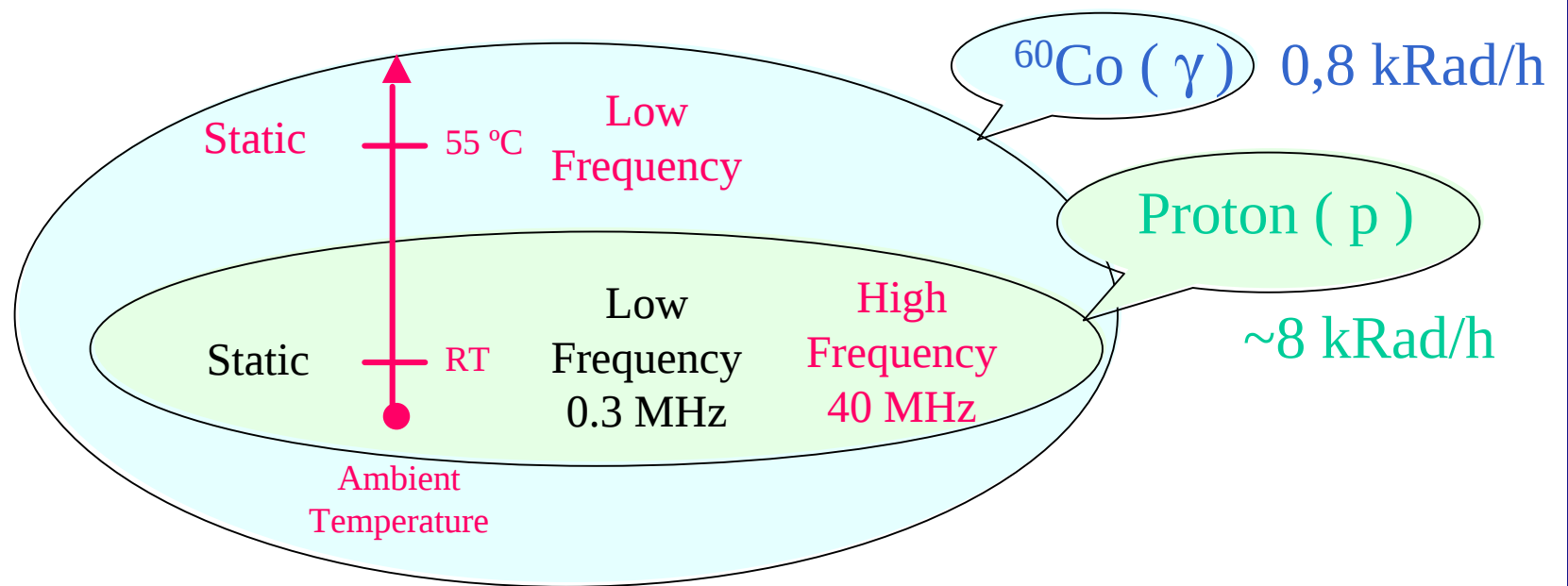
Fredrik Sturesson, Stanley Mattsson, Mikael Wiktorson
Saab Ericsson Space

Reno Harboe Sørensen
ESA/ESTEC



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Total Dose Effects by Protons



Results for ^{60}Co Tests

Source:

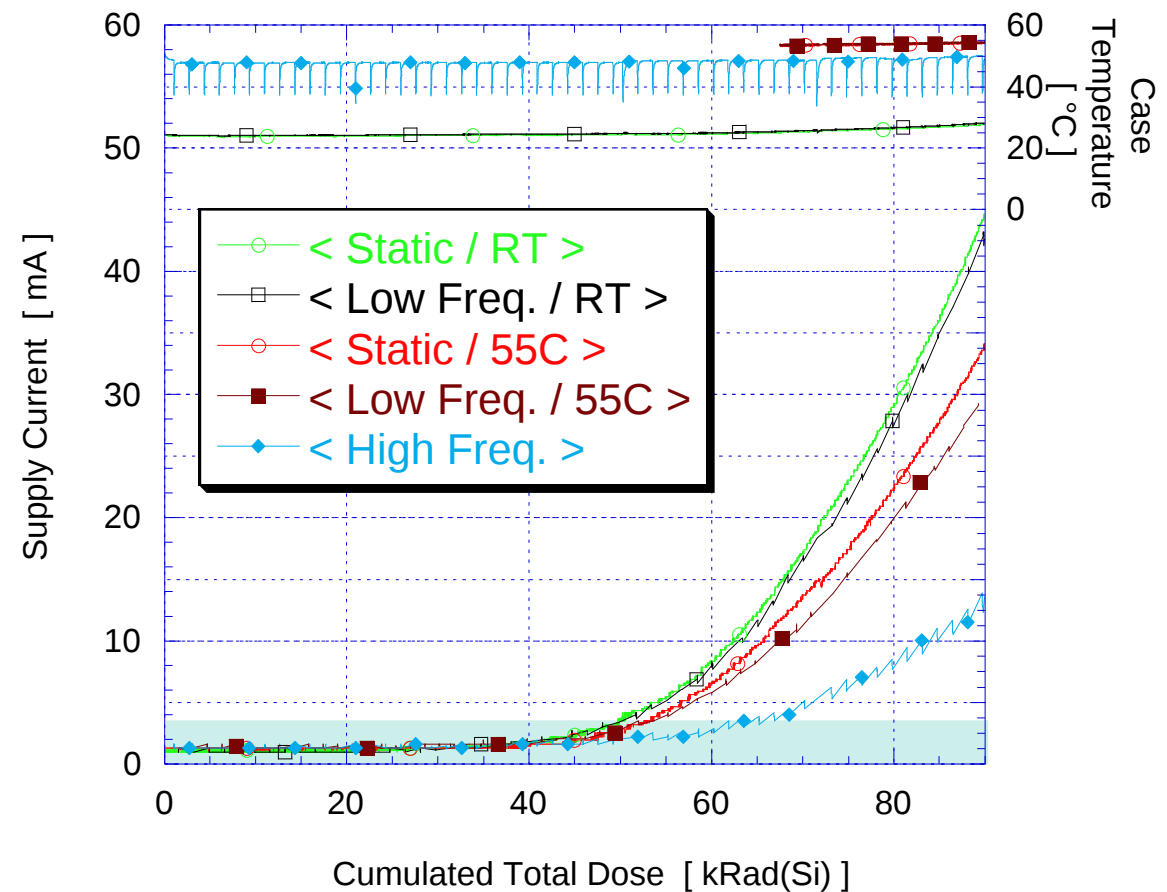
- ^{60}Co

TID Conditions:

- All 5

Parameter:

- Standby Current
- Case Temperature



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Results for Proton Total Dose

Source:

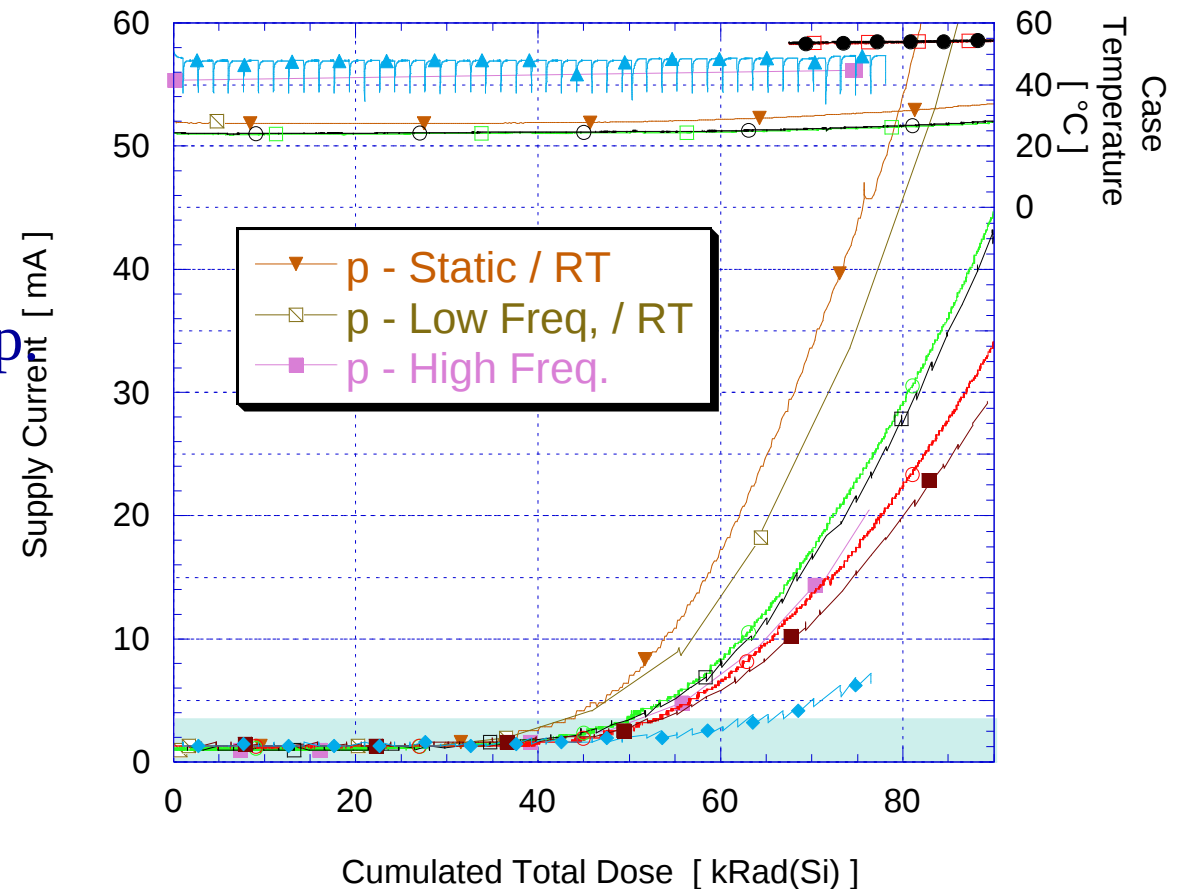
- Proton, 100 MeV

TID Conditions:

- All 3 in Room Temp

Parameter:

- Standby Current
- Case Temperature



Similar behavior as for Cobolt-60



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