MEMO

Date 27/02/2013

From Carole Villette
Tommaso Ghidini

To Industry, ESA PA Managers

Ref TEC-QT/2013/398/CV

Visa M. Nikulainen

Copy TEC-QTM: G. Corocher, J. Hokka, S. Heltzel,
TEC-QTC: L. Marchand
TEC-QQ: R. Ciaschi
TEC-Q: W. Veith
CNES: Th. Battault

Subject: SMT Verification as per ECSS-Q-ST-70-38C, revised work procedure

In order to improve the efficiency and ESA customer service of the ESA SMT verification
process per ECSS-Q-ST-70-38C, the following procedure is required for any new or delta
SMT verification request from Industry to ESA. This procedure may evolve once the ECSS-
Q-ST-70-38C will be updated.

1. A formal request shall be sent by Industry to ESA by an official letter. E-mails or
telephone requests shall not be served. Following the request, the verification
programme shall be sent by post and uploaded on the SMT server. The verification
programme shall contains the information requested in Annex 1.

2. Requests shall be addressed to Carole Villette TEC/QTM (ESTEC, PO Box 299-2200
AG Noordwijk ZH- The Netherlands) with a mandatory copy to T. Ghidini TEC-
QTM and to the relevant PA Manager (list enclosed in Annex 2) of the ESA project
concerned by the SMT verification.

3. In addition to the requested scope of the technical work, the concerned ESA project
and the expected time-line for the delivery of the results shall be indicated. Without
a clear indication of an ESA project customer, the SMT verification will not be
considered.

4. Furthermore, new or delta verification (eg. Change of soldering machine, solder
paste...) shall not be supported by ESA without a specific request from an ESA
project PA Manager.
In order to facilitate the review of the verification programme, the content of the different documents is Annexed to this letter.

In order to assure the quality of the input to ESA and avoid unnecessary iterations, it is recommended that the microsections are performed in the laboratories listed in Annex 4 or by Industry proposed laboratory that has been accepted by ESA TEC-QTM.

C. Villette  
Materials Technology Section

T. Ghidini  
Head of Materials Technology Section

Enclosed:
Annex 1: Content of the verification programme to be submitted to ESA
Annex 2: Additional information needed related to the verification programme
Annex 3: List of ESA PA Managers with its associated programme
Annex 4: List of companies recommended to perform microsections
Annex 5: TEC-QT/2012/206/CV
Annex 6: TEC-QT/2010/38/CV
Annex 1

Content of the verification programme to be submitted to ESA

The verification programme shall be delivered to ESA for review and approval. It is also recommended to provide the associated PID with the verification programme. The verification programme shall contain as a minimum the following:

1. Indication of the method of assembly

   • Assembly method such as machine reflow (Vapour Phase, convection reflow)
     Note: When machine reflow is used then hand soldering shall also be considered for verification.
   • Assembly by hand using a soldering iron
   • Assembly using hot air (repair station)
   • Statement of compliance of assembly with respect of the PID

2. PCB information

   • PCB material (Polyimide, epoxy, thermount, duroid...)
   • Number of layers. A single sided or double sided PCB shall not be considered valid for a verification exercise exception
   • Thickness
   • Built up with identification of signal and full copper plane
   • Location of the devices on the PCB
   • Connection of the pads to the internal layer shall be representative of the flight hardware
     o By via in pad
     o By track connected to vias
     o By tracks to other location
   It is recommended to have at least the corner leads (to be microsectioned) connected to the internal layers when applicable
   • Location of the mechanical fixation
     o Location of the stiffener
     o Location of the mechanical holes
   The mechanical fixation of the verification PCB shall be representative of the flight configuration.
   • Schematic of the mechanical stiffener if any.
   • Number of PCB used for the verification programme.
   • In case of verification of grid arrays device the technology used for the manufacturing of the pads and internal connections shall be the same than the FM
For grid array devices the type of laminate used for the verification boards shall be the same as for the FM.

3. Material used
- Solder paste designation and composition (to be compliant to the ECSS-Q-ST-70-08C or 38C)
- Solder wire composition with its associated flux (to be compliant to the ECSS-Q-ST-70-08C or 38C)
- Flux used (for pretiling and soldering). Designation of flux class (ROLO, ROL1...) shall be identified.
- Conformal coating
- Adhesive (for mechanical, for thermal, for grounding...)
If these information are available in the PID compliance to the PID shall be made.
- Solvent
- Any others

4. List of components

The information shall be provided as follow

<table>
<thead>
<tr>
<th>Component</th>
<th>Package</th>
<th>manufacturer</th>
<th>Assembly method</th>
<th>Bonding</th>
<th>Terminal material</th>
<th>Lead finish</th>
<th>Degold/pretin</th>
<th>Number of devices</th>
<th>Number of repair</th>
</tr>
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<tbody>
<tr>
<td>Chip ceramic capacitor</td>
<td>Co805 type 2</td>
<td>XXX</td>
<td>VP</td>
<td></td>
<td>Sn/Pb</td>
<td>N/A</td>
<td>N/A</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Chip ceramic capacitor</td>
<td>Co805 type 2</td>
<td>YYY</td>
<td>HS</td>
<td></td>
<td>Sn/Pb</td>
<td>N/A</td>
<td>N/A</td>
<td>3</td>
<td>1 part of the 3</td>
</tr>
<tr>
<td>IC</td>
<td>COFP 352 top brazed, Pitch: Lead thickness:</td>
<td>ZZZ</td>
<td>HS</td>
<td>In the corner using EC2216</td>
<td>Kovar</td>
<td>gold</td>
<td>Yes</td>
<td>3</td>
<td>1 part out of the 3 assembled</td>
</tr>
<tr>
<td>IC</td>
<td>FP16 Bottom brazed</td>
<td>VVV</td>
<td>HS</td>
<td>Alloy 42</td>
<td>gold</td>
<td>yes</td>
<td>3</td>
<td>1 part out of the 3 assembled</td>
<td></td>
</tr>
</tbody>
</table>
Note 1: A dedicated assembly form is recommended where all information which concern preparation of the device, assembly method and bonding are available.

Note 2: It is under the responsibility of the company to ensure that the soldering method and temperature is compliant with the manufacturer datasheet and or technical notes.

Note 3: The devices assembled by machine reflow shall not be reworked. Reworking will be decided during the MIP1.

- When the purpose of the verification is to verify the assembly by machine, 3 devices assembled by machine shall be mounted and 3 devices assembled by hand shall be mounted on the PCB. 1 of the hand soldering device shall be removed and replaced by hand to demonstrate the ability of the company to perform a repair.
- When the purpose of the assembly is to verify the assembly by hand only, 3 devices assembled by hand shall be mounted on the PCB exception made for the critical devices listed in the document TEC-QT/2012/206/CV (enclosed). One of the hand soldering device shall be removed and replaced by hand to demonstrate the ability of the company to perform a repair.
- Exception to the number of devices shall be considered for critical devices (See TEC-QT/2012/206/CV). In this case a minimum of 5 devices instead of 3 shall be assembled.

The actual considered critical devices are the following:
- Ceramic chip resistors: R1206, R2010, R2512 due to extensive cracks in the solder
- LCCs package: All packages due to extensive cracks in the solder
- JLCC4 (currently package of oscillators) due to extensive cracks in the solder
- SMDs package: SMD0.5, SMD5C, SMD1, SMD2 due to crack in the ceramic package
- Ceramic chip capacitors for which the failure is identified in the ceramic as a crack. The crack is not visible from the outside during visual inspection.
- CWRo6 packages: Cracks in the silver loaded epoxy.

- The number of devices to be assembled in case electrical monitoring is considered as a pass/fail criteria shall be as a minimum of 32 devices (with exception to grid array devices).
- A minimum of 3 devices to be verification tested by electrical monitoring shall be microsectioned at To in order to ensure compliance of the assembly (reproductibility of stand-off if applicable, acceptable wetting, absence of damage of the component, PCB, ...)
- As a minimum one failed device shall be microsectioned to identify the failure mechanism.

Note: The electrical monitoring parameters and procedure will be defined case by case as this technic is a novel procedure.
When the device is bonded underneath demonstration of the removal after bonding shall be made. In this case it is recommended to have the repair configuration used for this purpose.

5. Environmental test conditions

- Compliance of the environmental conditions of the mission (including ground testing) with the ECSS-Q-ST-70-38C, in order to ensure that the tests requested in the ECSS are sufficient to cover the application. The analysis shall identify if the mission has condition that are generally not enveloped by the test defined in the ECSS-ST-Q-70-38C as: long storage, extensive ground testing, mechanical stress after launch, high temperature application with or without thermal cycles. Compliance to the -55°C/+85°C for mission shall be clearly stated.
- The levels and duration of the vibration shall be identified. Statement such as compliance with the ECSS-Q-ST-70-38C will not be considered acceptable as different levels exist. It is the responsibility of the contractor to ensure that the levels applied are sufficient to cover the mission.
- The mounting configuration for the vibration tests shall be identified. The PCB shall be mounted in a way representative of the mounting of the flight hardware. Hard mounting with the PCB being in direct contact with the vibration plate shall not be considered acceptable.
- As per the ECSS-Q-ST-70-38C the accelerometers shall be placed on the PCB as well as on the base plate in order to evaluation the acceleration as well as the deformation of the PCB.
- The thermal cycling between -55/+100°C is only valid when the thermal analysis for the mission shows that the electronic hardware will be working (functional and not functional) between -55°C and +85°C.
- In case electrical monitor is used (grid array devices) acceptance failure criteria based on the most demanding use shall be defined by the contractor.
- Shock tests shall be added when assembly of Area Array devices is part of the verification programme.

6. Microsections

The microsections shall be performed at the completion of the environmental test and in compliance with the TEC-QT/2010/38/CV (enclosed document).

1. The company which will perform the microsections shall be identified in the verification programme.
2. Microsection shall be performed in the companies laboratories approved by ESA. A list of laboratories recommended by ESA is provided in Annex 3.
3. When in house microsection facilities exist, the company shall demonstrate its capability on a representative sample (chips, LCCs, FP) having been conformally coated. In addition the understanding of the ECSS shall be
demonstrated. A report with associated microsections shall be sent to ESA for review and assessment of quality of microsectioning.

4. Other laboratories. The company shall ensure when conditions 2) and 3) are not met that the quality of microsectioning is acceptable as well as that the ECSS requirements are understood. A report with associated microsections shall be sent to ESA for review and assessment of quality of microsectioning. At least one device per type and size shall be microsectioned. Devices being assembled in different configurations such as machine reflow, hand soldering, hot air assembled, different bonding configurations,... shall be microsectioned.

5. All critical devices whatever their assembly configuration shall be microsectioned.

7. Pass-fail criteria parameters

In addition to the ECSS-Q-ST-70-38 any cracks in the adhesive, lifting of the adhesive, damage to the component, damage to the printed circuit board shall be considered as a failure.

Note: It is recommended to have an intermediate visual inspection during thermal cycling in order to assess when crack, lifting in adhesive appears.

8. Manufacturing work flow

In order to ensure full support from the Agency the progress of the verification programme shall be known. In order to ensure this the following steps shall be added in the verification programme.

1. Verification Review (VR) during which the verification programme will be reviewed and Approved by ESA. The verification programme can be signed by the Agency if deemed necessary by the company.
2. Design Review (DR) of the PCB. Information of the Paragraph 2 will be needed to conclude successfully the review. A successful DR will be concluded by the authorization to procure the PCB.
3. PID status review
4. Audit of the manufacturing line
5. Manufacturing Readiness Review (MRR). During the review the Agency will check that the verification programme has been approved by all parties and that all open actions have been closed.
6. Mandatory Inspection Point (MIP 1) before conformal coating. ESA shall be invited to the MIP1.
7. Test Readiness Review (TRR) during which the MIP records shall be reviewed. The Verification programme shall be at this stage approved and signed by all parties. The vibration, shocks and thermal procedures shall be provided and reviewed during this review.
8. Mandatory Inspection Point (MIP2) at the completion of the environmental test. The Agency shall be invited to the MIP2.
9. Test review board (TRB) during which the environmental tests results will be reviewed. All open NCRs (minor and major) shall be reviewed and closed.
10. Final verification review during which the microsections reports, electrical monitoring results will be reviewed. The Assembly processes will be reviewed during the meeting in order to have the PID issued. Verification of closure of the actions identified during the audit of the manufacturing line. It is the objective of the review to agree on the content of the Summary Tables.

11. Approval of Summary table and final approval of PID and related procedures

9. NCRs

Any NCRs related to the assembly shall be reported to the Agency. If needed NRBs shall be organised by the contractor.

It is the intention of the Agency to organise a ftp server such as NCTS where the NCRs will be uploaded. Contractor will be informed when the ftp server will be on service.

10. Verification by similarity

- Verification by similarity shall be applied in compliance with the ECSS-Q-ST-70-38C.
- It is advised for critical devices to add intermediate size in case the biggest device fails.
- Verification by similarity does not apply for LCCs package.

11. Certification status of the operators and inspectors

The compliance with the ECSS-Q-ST-70-08C shall be identified.

12. Compliance of the manufacturing room

The compliance with the ECSS-Q-ST-70-08C shall be identified.
Annex 2

Additional information needed related to the verification programme

1. Planning

The detailed chart shall be provided.
Update of the planning will be provided during the different step identified in Paragraph 7.

2. Vibration test procedure

The content of the vibration test procedure shall be as followed:

1. List of Applicable documents
   a. Project Requirement
   b. ECSS-Q-ST-70-08C
2. Company selected to perform the vibration
3. Test set up
4. List of the PCBs to be tested with their associated layout
5. Schematic of the PCB mounted with its frame (to ensure that the stiffener is sufficient for the vibration levels)
6. Schematic of the test adapter
7. List of the test instrumentation
8. Location of the accelerometers
9. Test conditions (Temperature, Pressure, Humidity, cleanliness) and tolerances (Frequency, Amplitude, sweep rate, power spectral density, random overall, test duration)
10. EMC conditions when applicable
11. Tests levels
   a. Resonance search
   b. Sine vibration
   c. Random vibration
12. Test flow
13. Success criteria

3. Thermal cycling test procedure

The content of the vibration test procedure shall be as followed:

1. List of Applicable documents
   a. Project Requirement
   b. ECSS-Q-ST-70-08C
2. Company selected to perform the thermal cycles
3. Test set up (thermo couple mounted on the boards)
4. List of the PCBs to be tested
5. Mounting configuration of the PCB in the thermal chamber
6. List of the test instrumentation
7. Test conditions (Temperature, Pressure, Humidity, cleanliness, slopes, dwell time, number of cycles, atmosphere of the thermal chamber) and temperature tolerances
8. EMC conditions when applicable
9. Test flow
## ANNEX 3

List of ESA PA Managers with its associated programme (List subjected to change in the future)

<table>
<thead>
<tr>
<th>Last name</th>
<th>First name</th>
<th>Position</th>
<th>Projects</th>
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<tbody>
<tr>
<td>Damiano</td>
<td>Giovanni</td>
<td>Product Assurance Manager</td>
<td>Expert</td>
</tr>
<tr>
<td>Ferrer</td>
<td>Sonia</td>
<td>Product Assurance Manager</td>
<td>ERA / ATV</td>
</tr>
<tr>
<td>Kaspers</td>
<td>Martin</td>
<td>Product Assurance Manager</td>
<td>EGNOS</td>
</tr>
<tr>
<td>Adriaan</td>
<td>Willem J.</td>
<td>Ground Segment Product Assurance Engineer</td>
<td>Galileo</td>
</tr>
<tr>
<td>Aldea Montero</td>
<td>Fernando</td>
<td>Galileo Software PA Manager</td>
<td>Galileo</td>
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<tr>
<td>Azcarate Lupioli</td>
<td>Jose</td>
<td>Msg Product Assurance Manager</td>
<td>MSG-Metop 3</td>
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<tr>
<td>Monteiro</td>
<td>David</td>
<td>Product Assurance Manager</td>
<td>Gaia</td>
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<tr>
<td>Beurtey</td>
<td>Xavier</td>
<td>Product Assurance Manager</td>
<td>Ariane</td>
</tr>
<tr>
<td>Brown</td>
<td>Andrew</td>
<td>Galileo Ground Segment PA Manager</td>
<td>Galileo</td>
</tr>
<tr>
<td>Pierre</td>
<td>Brunner</td>
<td>Product Assurance Manager</td>
<td>IXV</td>
</tr>
<tr>
<td>Bussu</td>
<td>Giancarlo</td>
<td>Product Assurance and Safety Manager</td>
<td>ISS Utilisation</td>
</tr>
<tr>
<td>Di Cosimo</td>
<td>Gianluigi</td>
<td>Head of the GMES Space Segment PA &amp; S Office</td>
<td>Sentinel 2</td>
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<tr>
<td>Chase</td>
<td>Richard</td>
<td>Product Assurance &amp; Safety Manager</td>
<td>ATV Operations</td>
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<tr>
<td>Chevrier</td>
<td>Muriel</td>
<td>Quality Engineer</td>
<td>D/QPS Quality Office</td>
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<tr>
<td>Hall</td>
<td>John</td>
<td>Product Assurance Manager</td>
<td>Galileo</td>
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<td>Di Mascio</td>
<td>Simone</td>
<td>Software Product Assurance Engineer</td>
<td>Galileo</td>
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<td>Massimo</td>
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<td>Fogli</td>
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<td>Quality Engineer</td>
<td>D/QPS Quality Office</td>
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<td>Garat</td>
<td>Francois</td>
<td>Product Assurance &amp; Safety Manager</td>
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<td>Geary Norrenbrock</td>
<td>James Hermann</td>
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<td>Vema</td>
<td>Marco</td>
<td>PA Engineer</td>
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<td>Small GEO Platform Programme</td>
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<td>Product Assurance &amp; Safety Manager</td>
<td>LISA Pathfinder</td>
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<td>Lefort</td>
<td>Eric</td>
<td>H/ Launchers Prod Assur and Safety Office</td>
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<td>Liner</td>
<td>Herbert</td>
<td>PA Engineer</td>
<td>Vega</td>
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<td>Lock</td>
<td>Tim</td>
<td>Product Assurance and Safety Manager</td>
<td>ESAC</td>
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<tr>
<td>Mantinelo</td>
<td>Alfio Roberto</td>
<td>Head of D/QPS Quality Office</td>
<td>D/QPS Quality Office</td>
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<td>Last name</td>
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<td>Meehan</td>
<td>John</td>
<td>Product Assurance &amp; Materials Eng</td>
<td>ISS Utilisation</td>
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<td>Norrenbrock</td>
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<td>Pinel</td>
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<td>Rautakoski</td>
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<td>Emmanuel</td>
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<td>Stefano</td>
<td>PA &amp; Safety Manager</td>
<td>D/OPS Quality Office</td>
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<td>Secchi</td>
<td>Patrizia</td>
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<td>Simonini</td>
<td>Andrea</td>
<td>Quality Assurance Manager</td>
<td>PDS / EOP Apps</td>
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<td>Soulez</td>
<td>Cyril</td>
<td>Product Assurance Engineer</td>
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<td>Torres Tomas</td>
<td>Eloy</td>
<td>Senior Product Assurance Engineer</td>
<td>Large Platform Programme</td>
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<td>Vicari</td>
<td>Emmanuel</td>
<td>Product Assurance Manager</td>
<td>D/OPS Quality Office</td>
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<td>Villar Ruijbal</td>
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<td>Vivar y</td>
<td>Maria de la</td>
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<tr>
<td>Wernham</td>
<td>Denny</td>
<td>Product Assurance Manager</td>
<td>Aeolus</td>
</tr>
<tr>
<td>Woop</td>
<td>Gregor</td>
<td>Head of the ISS PA&amp;S Coordination Office</td>
<td>ISS Programme</td>
</tr>
</tbody>
</table>
ANNEX 4

List of companies recommended to perform microsections (List subjected to change in the future)

- Hytek in Denmark
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  France
  Phone(Mobile): +33 (0) 684057599
  e-mail: m.leveque@serma.com
  Fax: +33(0)562131617

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  D-82234 Oberpaffenhofen
  Germany
  Phone: +49814340320
  e-mail: karl.ring@zve.izm.fhg.de
MEMO

Date 14 January 2013

From Carole Villette

To Companies having ESA Approved Summary Tables or under verification programme

Ref TEC-QT/2012/206/CV

Visa T. Ghidini

Copy PA Managers

Subject: Identified critical devices for the assembly as per ECSS-Q-ST-70-38 on PCB laminates

During the past years some failures on solder joints or in devices have been identified at the completion of the environmental testing performed in compliance with the ECSS-Q-ST-70-38C.

It is the intention of ESA to inform industry, when not already done in order to prevent the use of these devices or to identify possible corrective actions.

The list of devices is not exhaustive and some devices may be missing. In the future, this list will be updated every time new failures are documented. The criticality has been identified when the failures in the solder joints and/or in the devices have been noticed in many occasions by different end users. In many cases it has also been concluded that failures could occur to a process not compliant to the component manufacturer assembly recommendations. In these cases the component was not considered as critical. In general, these failures have been identified thanks to the improvement of the quality of the microsections requested by ESA in the last years as well as increase of number of microsectioned devices and terminals.

Some of the failures identified in the table may result to the large temperature range used during the thermal cycles and may not appear when the temperature range is reduced. Reduction of temperature range will result in an increase of number of cycles.

In addition to the failures listed in Table 1, a failure due to excessive conformal coating has also been identified. It is recommended that conformal coating is used such that it does not negate the stress relief and does not fully encapsulate the devices. Indeed during thermal cycling the conformal coating is responsible to additional stress and may lead at some extend to cracks in the solder joints.

Once verification test in compliance with the ECSS-Q-ST-70-38C have been completed and are considered successful, the amount of conformal coating shall not be modified since otherwise the ESA Approval status will no more be valid.
<table>
<thead>
<tr>
<th>Component</th>
<th>Package type</th>
<th>Type of failure</th>
<th>Recommendations and or notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Resistor</td>
<td>R1206, R2010, R2512</td>
<td>Cracks in the solder joint</td>
<td>- To increase the stand off. Such corrective action may not be sufficient.</td>
</tr>
<tr>
<td>Chip Capacitors</td>
<td>Any</td>
<td>Crack in the ceramic initiated at the end termination</td>
<td>- To follow component manufacturer recommendations (preheating of the board, device and limited temperature) - Rework of such capacitors shall not be performed. In case of rework needed replacement of the device is recommended.</td>
</tr>
<tr>
<td>LCCs</td>
<td></td>
<td>Crack in the solder joint</td>
<td>- Degolding and preheating temperature used to be compliant to component manufacturer datasheet - To increase the stand off - To solder the device upside down and add gull wing terminations (need of verification in compliance with ECSS). Change of solder footprint is required. - To solder upside down and have long wiring implemented. - Not to consider any verification by similarity for such package.</td>
</tr>
<tr>
<td>Tantalum capacitors</td>
<td>CWR06</td>
<td>Crack in the device. Crack in the epoxy between the tantalum and the terminal.</td>
<td>- Use of TAI/ CWR packages for which the temperature is not directly spread to the package.</td>
</tr>
<tr>
<td>SMDs</td>
<td>SMD0.5, SMD1, SMD2, SMD5C</td>
<td>Crack in the ceramic</td>
<td>- Procurement of package with terminations when possible which require a change of design of the solder footprint. - Assembly upside down using thermal adhesive and addition of wires or ribbons. This configuration may not be adapted for high thermal dissipation need.</td>
</tr>
<tr>
<td>Oscillator</td>
<td>JLCC4 with bottom brazed terminals</td>
<td>Crack in the solder joint</td>
<td>- Failure due to stiffness of the terminals combined with missing stress relief.</td>
</tr>
<tr>
<td>Stacked devices</td>
<td>SOP from 3D+</td>
<td>Crack in the solder</td>
<td>- Procurement of devices with</td>
</tr>
<tr>
<td>Device Type</td>
<td>Component</td>
<td>Issue</td>
<td>Solution</td>
</tr>
<tr>
<td>---------------------</td>
<td>--------------------</td>
<td>-----------------------------------------------------------------------------------------------------------</td>
<td>---------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Stacked capacitors</td>
<td>CNCXX</td>
<td>- poor wetting due to finish type 10 (Ag 98%)</td>
<td>- To pre-tin the device</td>
</tr>
<tr>
<td>Photo transistor</td>
<td>Pill from micropac</td>
<td>- Cracks in the solder joint of the two small terminals</td>
<td>- To degold and pretin at temperature compliant to the component manufacturer recommendations.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Not to solder the bottom part on the PCB but to make a wiring connection.</td>
</tr>
<tr>
<td>Inductor</td>
<td>Coilcraft inductor</td>
<td>Poor wetting of the terminals</td>
<td>- To request coilcraft for additional cleaning of the terminal to remove the contamination from the enamel present on the terminal.</td>
</tr>
<tr>
<td></td>
<td>AE235 type</td>
<td></td>
<td>- Recommendation to add an insulation (kapton, brady label, filled varnish...) to avoid contact with metallic traces.</td>
</tr>
<tr>
<td>Enamel wire</td>
<td></td>
<td>Short due to damaged enamel</td>
<td></td>
</tr>
</tbody>
</table>

Table 1: List of identified critical devices for the assembly as per ECSS-Q-ST-70-38 on PCB laminates.
**Microsection guidelines:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Diagram</th>
</tr>
</thead>
<tbody>
<tr>
<td>SO123</td>
<td>![Image]</td>
</tr>
<tr>
<td>LCC3</td>
<td>![Image]</td>
</tr>
<tr>
<td>TO252</td>
<td>![Image]</td>
</tr>
<tr>
<td>SO20</td>
<td>![Image]</td>
</tr>
<tr>
<td>LCC6</td>
<td>![Image]</td>
</tr>
<tr>
<td>D2 Pack</td>
<td>![Image]</td>
</tr>
<tr>
<td>FP</td>
<td>![Image]</td>
</tr>
<tr>
<td>SES1</td>
<td>![Image]</td>
</tr>
<tr>
<td>Chip resistor</td>
<td>![Image]</td>
</tr>
<tr>
<td>Component</td>
<td>Description</td>
</tr>
<tr>
<td>---------------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>MM series resistors</td>
<td><img src="image" alt="MM series resistors" /></td>
</tr>
<tr>
<td>CRA 12E and array resistors</td>
<td><img src="image" alt="CRA 12E and array resistors" /></td>
</tr>
<tr>
<td>CTC</td>
<td><img src="image" alt="CTC" /></td>
</tr>
<tr>
<td>LCC with terminations on 4 faces</td>
<td><img src="image" alt="LCC with terminations on 4 faces" /></td>
</tr>
<tr>
<td>MPC1</td>
<td><img src="image" alt="MPC1" /></td>
</tr>
<tr>
<td>DO213</td>
<td><img src="image" alt="DO213" /></td>
</tr>
<tr>
<td>D5-B</td>
<td><img src="image" alt="D5-B" /></td>
</tr>
<tr>
<td>SMD</td>
<td><img src="image" alt="SMD" /></td>
</tr>
<tr>
<td>SOT223</td>
<td><img src="image" alt="SOT223" /></td>
</tr>
<tr>
<td>PM94-S4</td>
<td><img src="image" alt="PM94-S4" /></td>
</tr>
<tr>
<td>CWR</td>
<td><img src="image" alt="CWR" /></td>
</tr>
</tbody>
</table>

- To check during microsection of other pins
- To check ceramic cracks
- Only one termination for the new devices
<table>
<thead>
<tr>
<th>CH51</th>
<th><img src="CH51.png" alt="Diagram" /></th>
</tr>
</thead>
<tbody>
<tr>
<td>CQFP</td>
<td>To cut after embedding</td>
</tr>
<tr>
<td>MQFP</td>
<td><img src="MQFP.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>

```
| Location of the microsection      |                |
| Leads to be microsectioned       |                |
```

To check absence of damage of the PCB