SCSB Decisions Regarding OTP FPGA PPBI

(List of Heritage OTP FPGA Types Exempted from PPBI)

and

Best Practices for Programming

ESCC REP 010

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Scope

Under the authority of the SCSB an ESCC Working Group was established in September 2012 and tasked to analyse available data and experience gained from Post Programming Burn-in performed in accordance with ECSS-Q-ST-60Crev1 (clauses 4.6.4, 5.6.4, 6.6.4) on one time programmable FPGA types and to formulate recommendations toward a potential revision of the subject Post Programming Screening Requirements.

The results and findings are documented in the WG report ESCC WG 01/13 'PPBI for OTP FPGA'. The recommendations of this WG have been endorsed by the SCSB. The corresponding requirements have been introduced in ECSS-Q-ST-60Crev2 which makes reference to this document listing the OTP FPGA types that are found to have sufficient heritage data to renounce the requirement for PPBI and additionally defines best practices to be adopted for the programming of OTP FPGA types.

Part types regarded to have a 'clear and defined heritage'

The following FPGA types have been assessed to have accrued sufficient PPBI test data and space application heritage to renounce the requirement for PPBI as part of the post programming screening sequence. These types meet the criteria of "clear and defined heritage".

Manufacturer : Microsemi Corp. (USA)

- A1280XL
- RT1020
- RT1280A
- RT1425A
- RT1460A
- RT14100A
- A54SX32A on 0.22um UMC fab technology
- A54SX72A on 0.22um UMC fab technology
- RTSX32SU
- RTSX72SU
- RTAX250S
- RTAX1000S
- RTAX2000S
- RTAX4000S
- RTAX2000D
- RTAX4000D

For the part types listed above the criteria of "clear and defined heritage" is no longer fulfilled in the event of any major change according to MIL-PRF-38535 table A-I :

- change type d (mask changes affecting die size or active element, wafer diameter, final die thickness),

- change type f (metallization changes)
- change type o (fab move)
- change type w (modification of programming algorithms)

Best Practices for OTP FPGA Programming

As regards programming best practices for OTP Microsemi FPGAs, they shall include (but not necessarily be limited to) the following:

- Incoming control, storage management, device traceability and programming operations of the OTP FPGA devices shall be documented in procedures.
- Only trained personnel shall be allowed to program flight FPGAs.
- A method of configuration shall guarantee the programming file used for the programming. Verification of the conformity shall be performed after programming.
- Software version used for programming shall be recorded against the serial number of the programmed part.
- Calibration verification of the programming hardware shall be performed and recorded. Refer to the manufacturer's recommendation for calibration periodicity
- Self-diagnostic shall be run at the beginning of each programming campaign or prior to each programming operation (depending on FPGA type). Refer to the manufacturer's recommendation concerning self-diagnostic.
- Cleaning and visual inspection of the programming socket shall be periodically performed.
- Power line supplying the programming hardware shall be filtered and protected (i.e. use of on-line UPS (Uninterruptible Power Supply)). Manufacturer's recommendations to be followed.
- Programming area shall be classified as an ESD Protected Area (EPA)
- A Programming Review Board shall be in charge of the acceptance of programmed parts.