VISHAY®

One of the World's Largest Manufacturers of
Discrete Semiconductors and Passive Components

ENLARGING THE PRODUCT OFFERING OF SPACE QUALIFIED RESISTORS AND NETWORKS

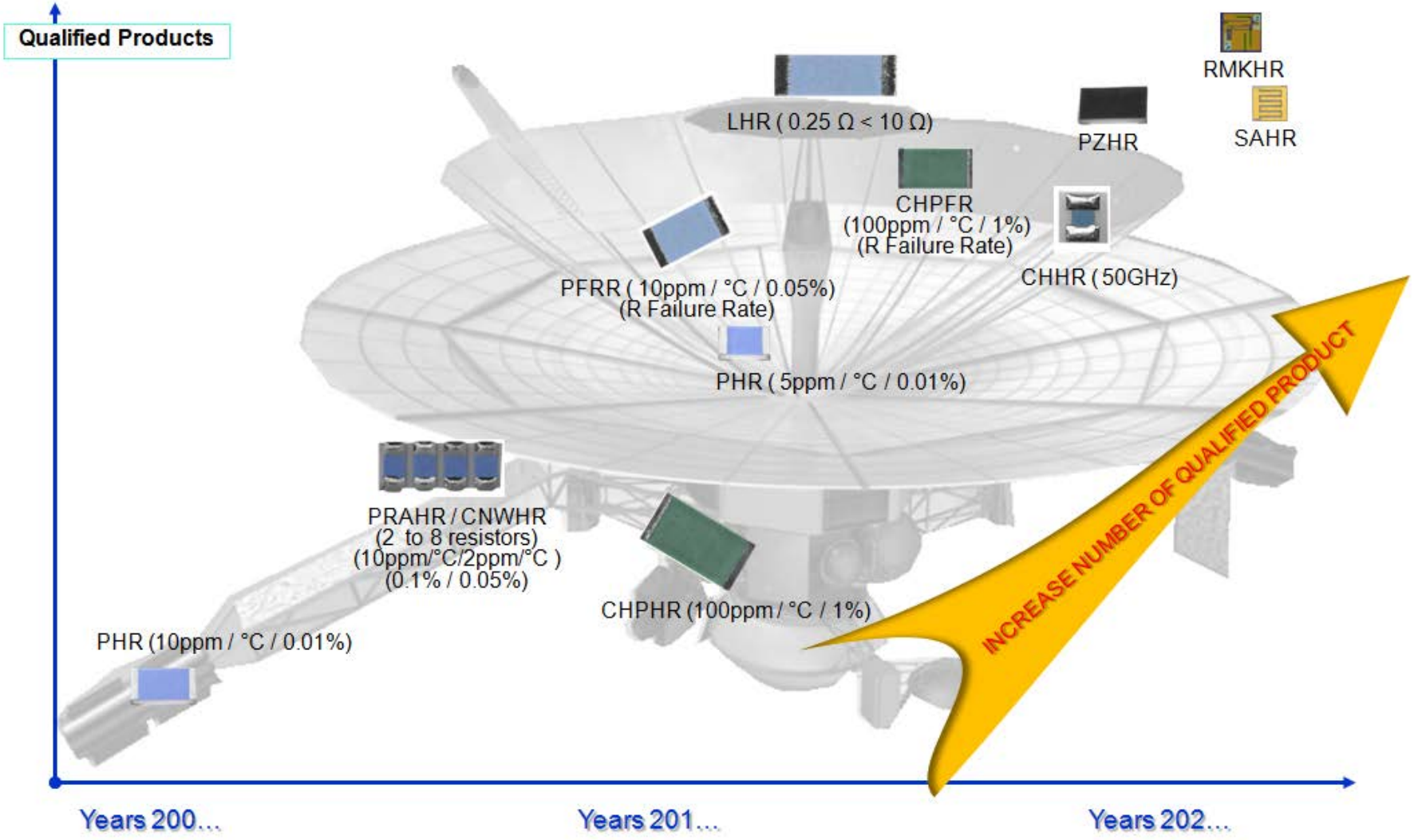
Ms D. Vignolo
Vishay / Sfernice

Build Vishay into your Design

Vishay Sfernice has been involved in Space business since the early 80’s.

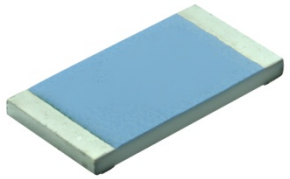
Vishay Sfernice is the first passive manufacturer to enter the ESCC/QML (ESCC Technology Flow Qualified Manufacturer List).

SPACE PRODUCT- ROAD MAP



Today's situation

Space Level



Thin Film (PHR)

Rationale:

No SMD product qualified neither in 0.01%, nor in 5ppm/°C

Qualified sizes: 0603 to 2010
Pending qualification: **0402 and 2512** (DCR raised)

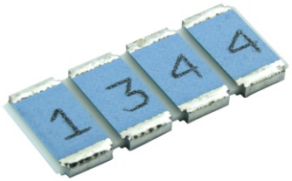
Qualified TCR: down to 5ppm/°C (-55°C; +155°C)
Qualified Tolerance: down to 0.01%
Qualified Ohmic Range: 10Ω to 3MΩ
Qualified Terminations: Tin/Lead and Gold

Operating temperature Range:

ESA qualified -55°C; +155°C
Customer qualified **-135°C**; +155°C

Today's situation

Space Level



Rationale:
No network qualified

Thin Film (PRAHR/CNWHR)

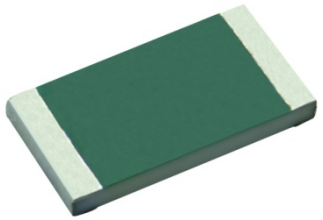
Qualified sizes:	100 – 135 - 182
New to be qualified:	**073 – 074** (smaller sizes)
Qualified TCR tracking:	down to 3ppm/°C (-55°C; +155°C)
Qualified Tolerance matching:	down to 0.05%
Qualified Ohmic Range:	100Ω to 1MΩ (like or alike values)
Qualified Terminations:	Tin/Lead

Operating temperature Range:

ESA qualified	-55°C; +155°C
Can operate	**-65°C**; +155°C

Today's situation

Space Level



Rationale:

No product qualified with Gold terminations

Thick Film (CHPHR)

Qualified sizes:	0603 to 2512
Qualified TCR:	down to 100ppm/°C (-55°C; +155°C)
Qualified Tolerance:	down to 1%
Qualified Ohmic Range:	1Ω to 10MΩ
Qualified Terminations:	Tin/Lead or gold

Operating temperature Range:

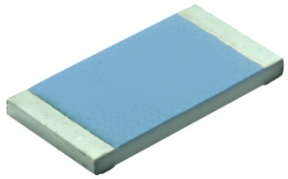
ESA qualified	-55°C; +155°C
Can operate	**-65°C**; +155°C

Today's situation

Rationale:

No product qualified neither in 0.05% nor in 10ppm/°C

R Failure Rate



Thin Film (PFRR)

Qualified sizes: **0402** to 2010

Qualified TCR: down to 10ppm/°C (-55°C; +155°C)
Qualified Tolerance: down to 0.05%
Qualified Ohmic Range: 100Ω to 3MΩ
Qualified Terminations: Tin/Lead

Operating temperature Range:

ESA qualified -55°C; +155°C
Can operate **-65°C**; +155°C

ESA R Failure Rate versus MIL R Failure Rate Sampling Plans and Procedures Specifications

Requirements	ESA Specification	MIL Specification	Comments
Failure Rate Level P	0.1% / 1000 hours	0.1% / 1000 hours	0.1% failure per 1000 componants hours
Failure Rate Level R	0.01% / 1000hours	0.01% / 1000hours	0.01% failure per 1000 componants hours
Failure Rate Level S	0.001% / 1000 hours	0.001% / 1000 hours	0.001% failure per 1000 componants hours
Duration of life test to cumulate unit hours	8000h Min	1000h Min	
Confidence Levels	60% / 90%	60% / 90%	Probability of disqualifying a product when the true failure rate of the product is at the failure rate specified for the qualification
Sampling Plans based on 60% confidence Level	20.2M cumulative unit hours: 1 failure permitted	20.2M cumulatuve unit hours: 1 failure permitted	R Failure Rate Initial qualification
Sampling Plans based on 90% confidence Level	38.9M cumulative unit hours: 1 failure permitted	38.9M cumulatuve unit hours: 1 failure permitted	R Failure Rate
Reconduction of qualification	5.32M cumulative unit hours	5.32M cumulative unit hours	Sampling Plans 10% confidence Level
Periodicity of Failure rate Maintenance Sampling plans	15 months	9 months	R Failure Rate. Periodicity based on volume of production on USA and in Europe

ESA specification: ESCC26000
MIL specification MIL-STD-690

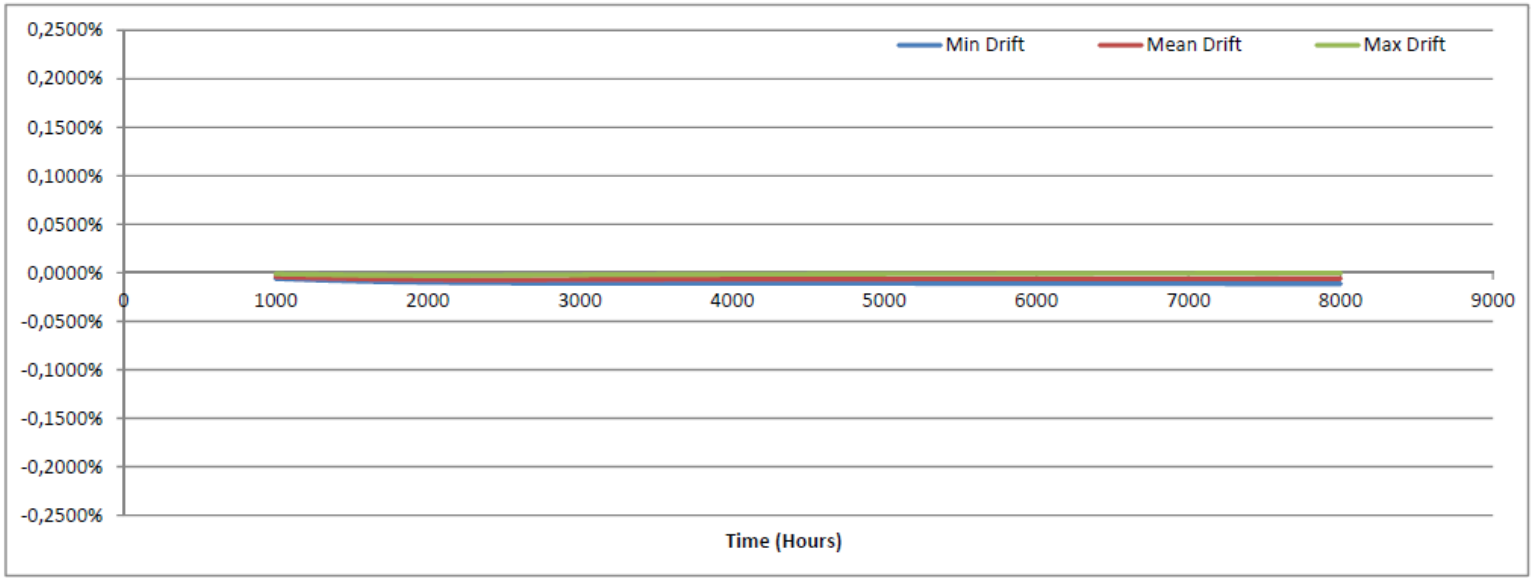
We might have following test results

FINAL RESULTS OF CUMULATED DRIFT AFTER 8000 HOURS (%)

Type : PFRR 2010

Values : 698 Ω

Time	500	1000	2000	4000	8000
Min Drift	-0,0036%	-0,0061%	-0,0101%	-0,0109%	-0,0116%
Mean Drift	-0,0020%	-0,0043%	-0,0070%	-0,0065%	-0,0059%
Max Drift	0,0004%	-0,0013%	-0,0028%	-0,0016%	-0,0004%



Almost same behavior after 1000h or 8000h

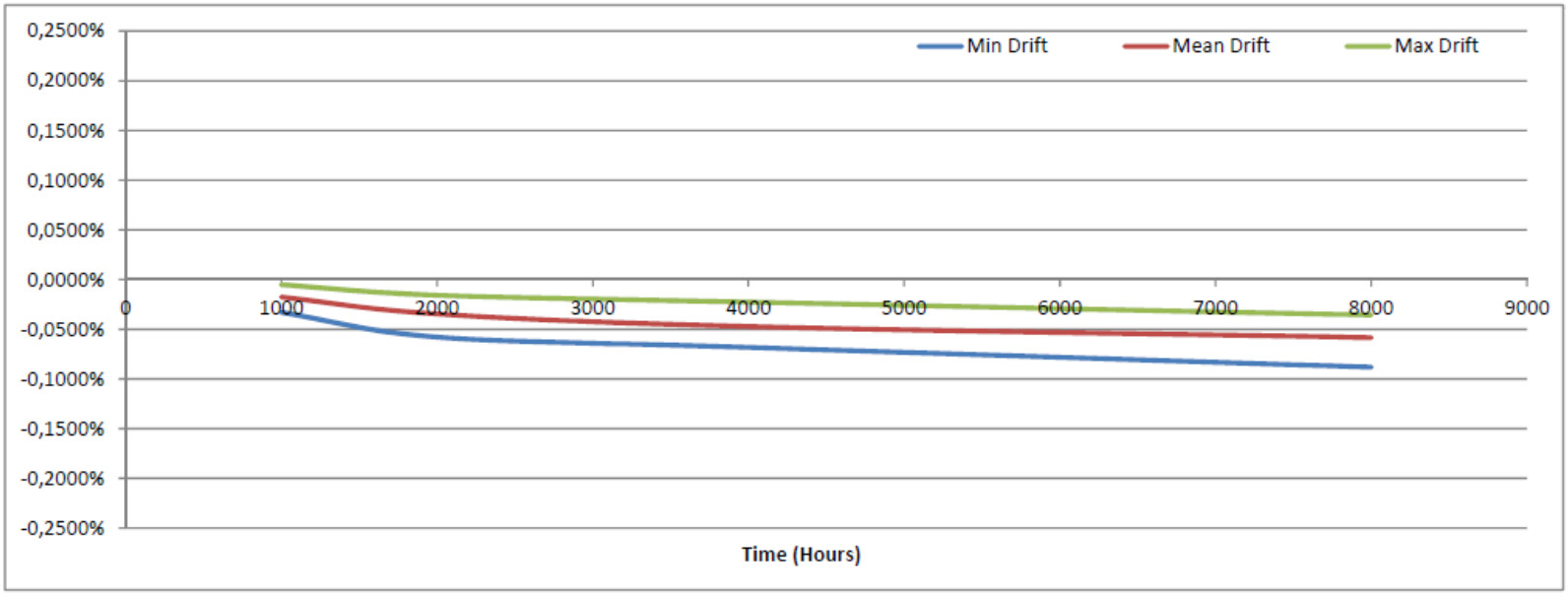
But also

FINAL RESULTS OF CUMULATED DRIFT AFTER 8000 HOURS (%)

Type : PFRR 0603

Values : 46400 Ω

Time	1000	2000	4000	8000
Min Drift	-0,0330%	-0,0578%	-0,0682%	-0,0881%
Mean Drift	-0,0177%	-0,0346%	-0,0473%	-0,0585%
Max Drift	-0,0052%	-0,0158%	-0,0227%	-0,0358%



One can see that parts had not stabilized after 1000h → 8000h
Load life is more relevant of the behavior of the parts

ESA R Failure Rate versus MIL R Failure Rate End of Production Testing

Requirements	ESA Specification	MIL Specification	Comments
Short Time Overload	100% of delivered parts	20 samples fom Inspection Lot	MIL spec: If the manufacturer can demonstrate that these tests have been performed five consecutive times with zero failures, the frequency of these tests, with the approval of the qualifying activity can be performed on an annual basis

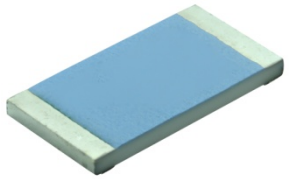
Purpose of short time overload:

To check if humidity has been trapped under protective coatings during the manufacturing of the parts (human contamination).
If so, parts will start drifting and eventually will be opened.

→ By performing 100% overload at end-of-production screening test, the ESA specification ensures that no part will fail in the field.

On going qualification

Space Level



Rationale:
No product qualified <1Ω

Thin Film (**LHR**)

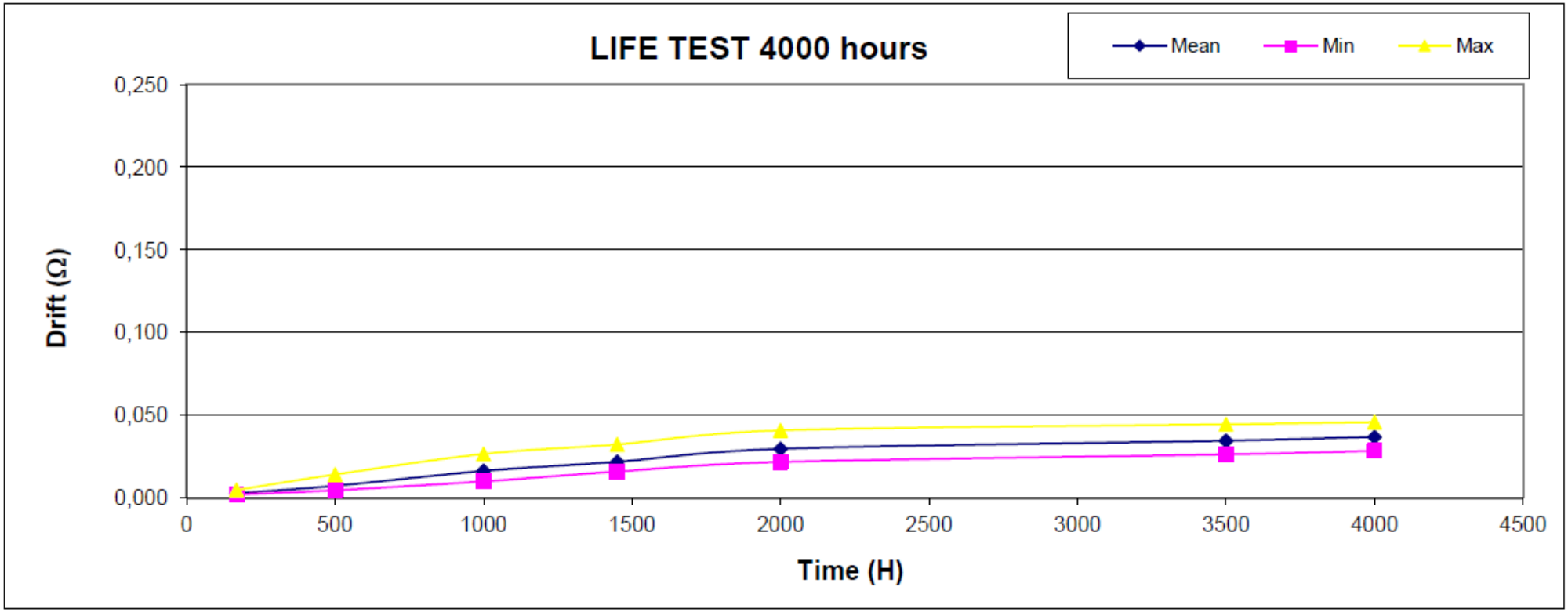
Qualified sizes:	0603 to 2512
Qualified TCR:	down to 100ppm/°C (-55°C; +155°C)
Qualified Tolerance:	down to 1%
Qualified Ohmic Range:	**250mΩ** to 9Ω99
Qualified Terminations:	Tin/Lead
Power Rating	125mW to 1W

Operating temperature Range:

ESA qualified	-55°C; +155°C
Can operate	**-65°C**; +155°C

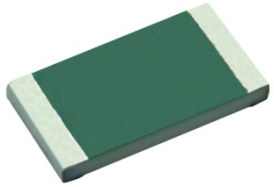
Thin Film (**LHR**)

Load life test: LHR0603 250mΩ, 150mW, 70°C



On going qualification

R Failure Rate



Rationale:
No product qualified

Thick Film (**CHPFR**)

Qualified sizes: 0603 to 2512

Qualified TCR: down to 100ppm/°C (-55°C; +155°C)
Qualified Tolerance: down to 1%
Qualified Ohmic Range: 1Ω to 10MΩ
Qualified Terminations: Tin/Lead

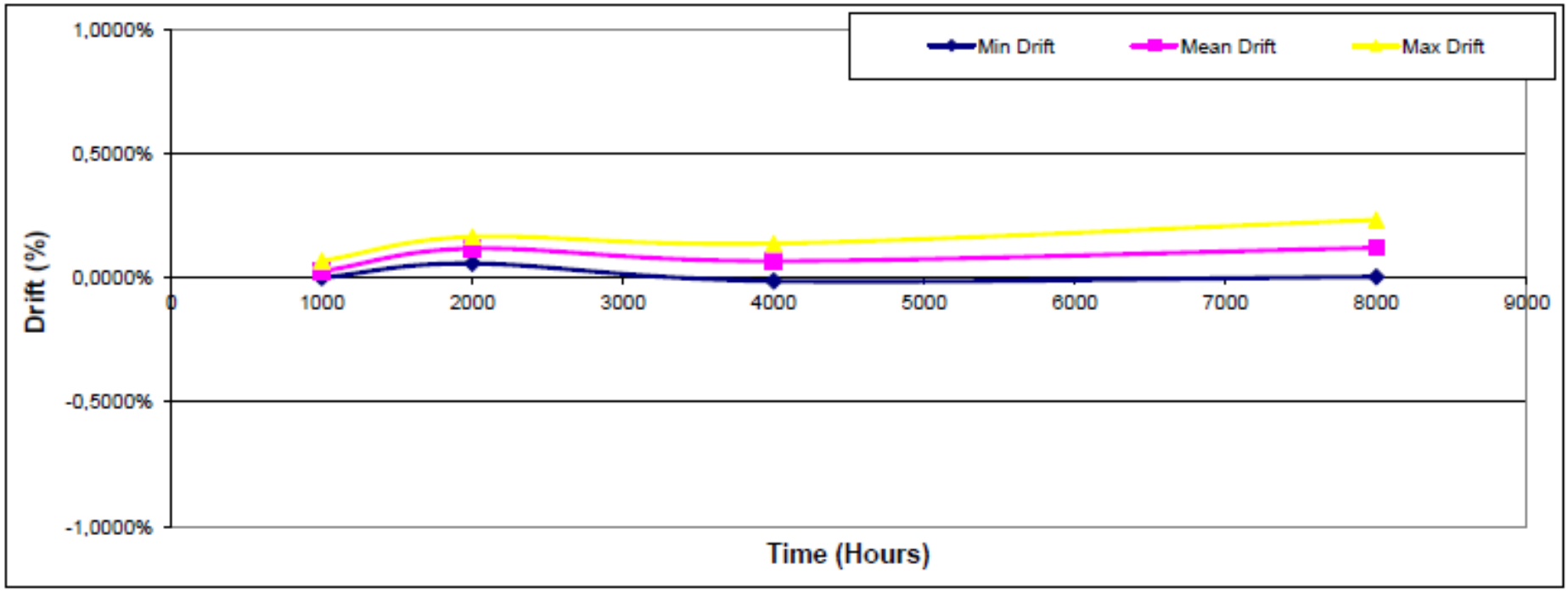
Operating temperature Range:

ESA qualified	-55°C; +155°C
Can operate	**-65°C**; +155°C

Thick Film (**CHPFR**)

Type : CHP0603
Value : 10Ω

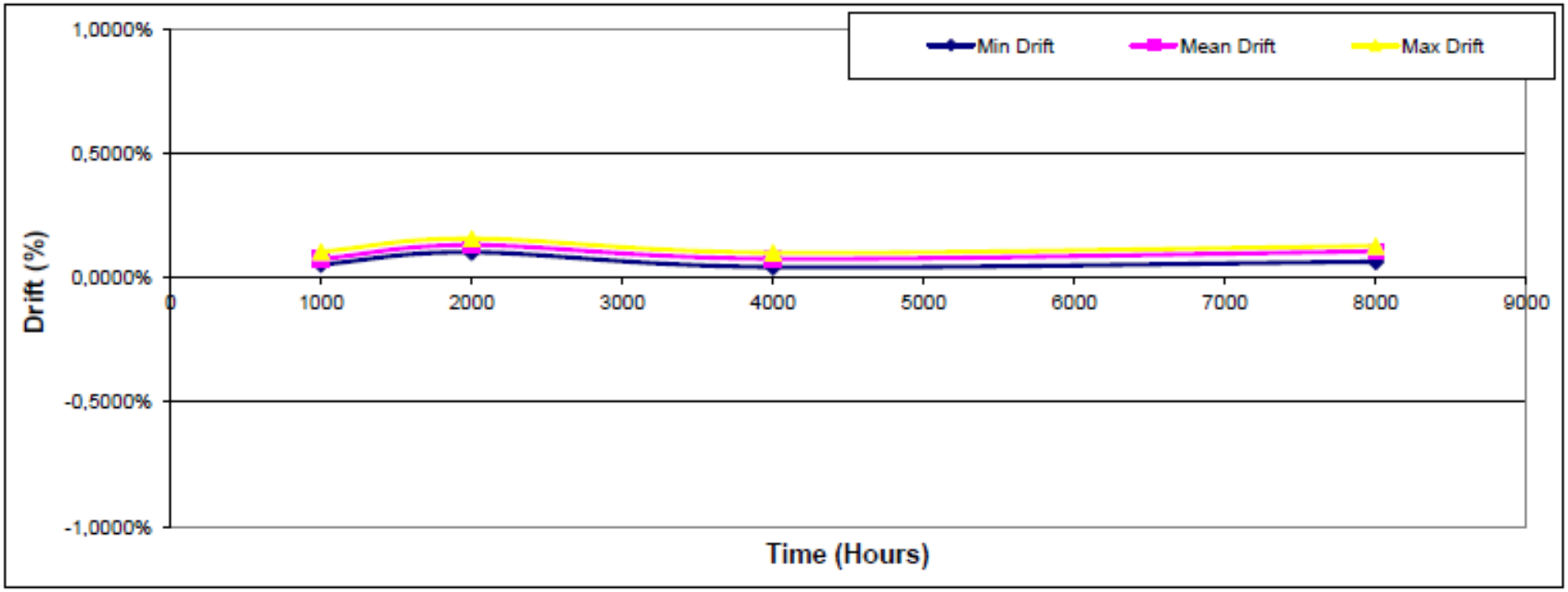
Time	1000	2000	4000	8000
Min Drift	0,0026%	0,0600%	-0,0113%	0,0057%
Mean Drift	0,0287%	0,1196%	0,0693%	0,1227%
Max Drift	0,0707%	0,1675%	0,1401%	0,2358%



Thick Film (**CHPFR**)

Type : CHP0603
Value : 1KΩ

Time	1000	2000	4000	8000
Min Drift	0,0557%	0,1042%	0,0450%	0,0664%
Mean Drift	0,0775%	0,1329%	0,0780%	0,1076%
Max Drift	0,1067%	0,1596%	0,1026%	0,1297%

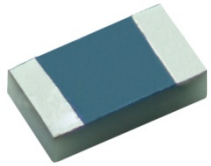


Customer Evaluation

Rationale

No hyper-frequency product qualified

Thin Film Hyper-frequency (**future CHHR**)

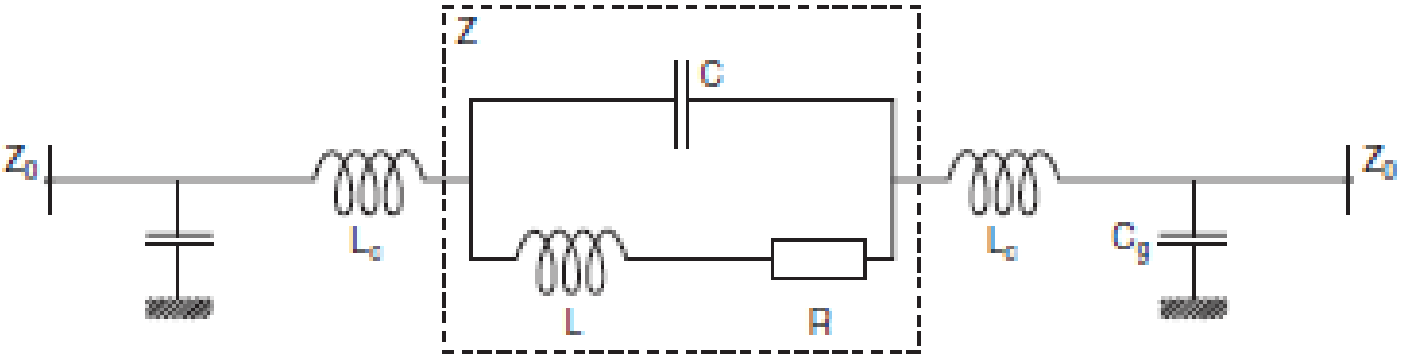


Sizes:	0402 and 0603
Operating frequency:	up to 50 Ghz
Tolerance:	down to 1%
Ohmic Range:	10Ω to 500Ω
Terminations materials:	Tin/Lead or gold
Terminations:	Wraparound or **Flip Chip** (better behavior)

Operating temperature Range:

ESA qualified	-55°C; +155°C
Can operate	**-65°C**; +155°C

Electrical Model



C	Internal shunt capacitance
L	Internal inductance
R	Resistance
Z	Internal impedance (R, L, C)
Ic	External connection inductance
Cg	External capacitance to ground

R, L and C are relevant to the chip resistor itself
Lc and Cg also depends on the way the chip resistor is mounted

After assembly, Lc and Cg will be combined to L and C. This combination can upgrade or downgrade the HF behaviour of the component

The complex impedance of the chip resistor is given by the following equation

$$Z = \frac{R + j\omega(L - R^2C - L^2C\omega^2)}{1 + C[(R^2C - 2L)\omega^2 + L^2C\omega^4]}$$

$$\frac{[Z]}{R} = \frac{1}{1 + C[(R^2C - 2L)\omega^2 + L^2C\omega^4]} \times \sqrt{1 + \left[\frac{\omega(L - R^2C - L^2C\omega^2)}{R}\right]^2}$$

$$\theta = \tan^{-1}\frac{\omega(L - R^2C - L^2C\omega^2)}{R}$$

ω=2 x π x f
f: frequency

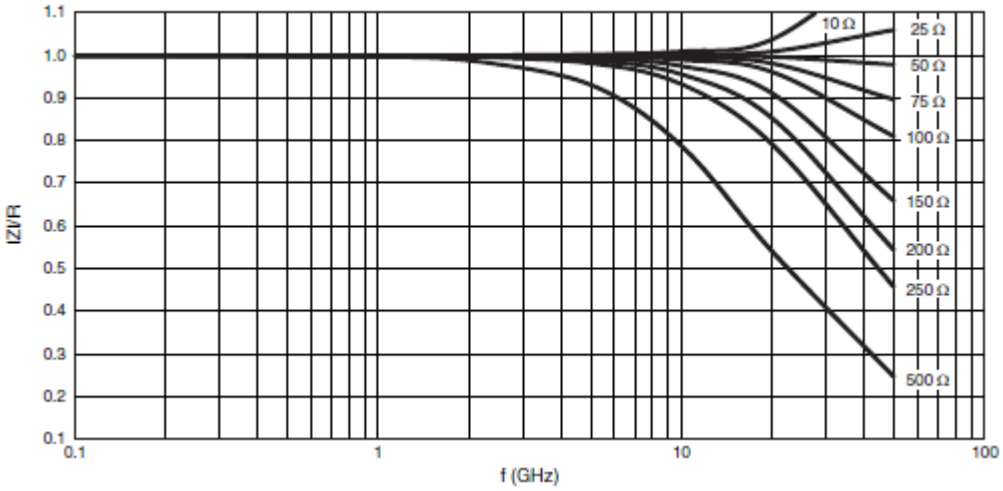
The chip resistor itself is purely resistive when $R = \sqrt{\frac{L}{C}}$.

The smaller the L x C product the greater the frequency range over which the resistor looks approximately resistive.

This can be seen on graphs of the following page

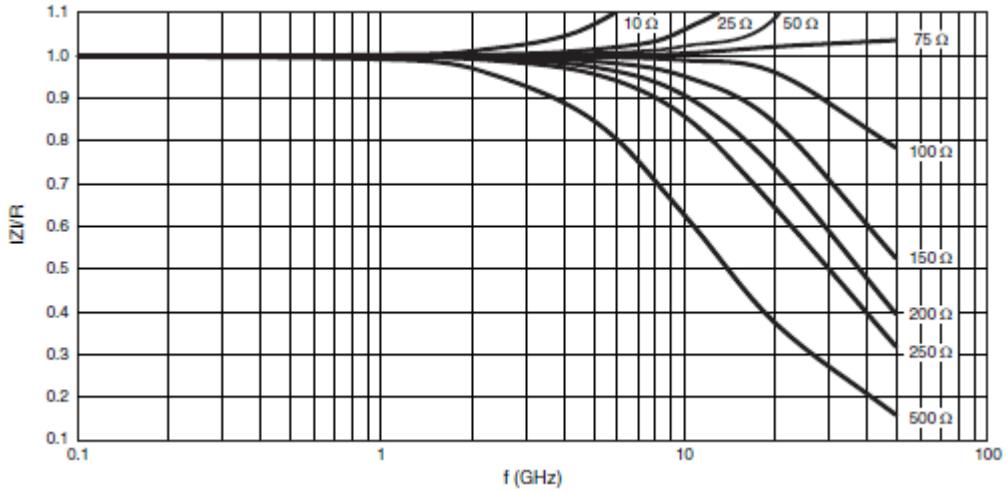
Experimental Data

Impedance Flip chip terminals (CH0402)



With wraparound terminals, at 10GHz there will be a parasite inductance/capacitance

Impedance Wraparound terminals (CH0402)



With flip chip terminals, a 50Ω chip resistor will act almost like a pure resistor until 30GHz.

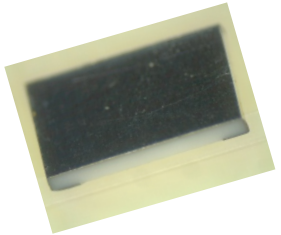
From previous example, and taking into account needs for space application of hyper-frequency chips resistors for High speed communications, it looks to us that a Flip Chip mounting process should be evaluated by ESA working groups in order to take the best from Hyper-frequency chip resistors

Customer Evaluation

Rationale:
No ESA strap qualified

SMD Straps (**future PZHR**)

Sizes: 0402 to 1206



Resistance value: <30mΩ
Maximum current through resistor: 0.5A to 6.3A
Terminations materials: Tin/Lead

Fully conform to MIL-PRF-32159

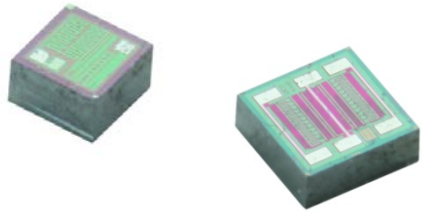
Heritage: Being used with option 57 for Space applications for 10 years

Customer Evaluation

Rationale:
No wirebondable qualified

Wirebondable chip resistors (**future RMKHR**)

Sizes: 22, 33, 44, 55, 515



Ohmic Range: 10Ω - 2MΩ
Temperature Coefficient: Down to 10ppm/°C (-55°C; +155°C)
Tolerance: Down to 0.01%
Substrate: Silicon
Terminations materials: Aluminum or **Gold**

Operating temperature range: -55°C; +155°C

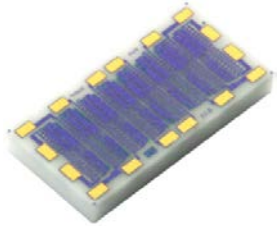
Heritage: Being used with an option corresponding to customer's specification, in Space applications, for a decade.

Customer Evaluation

Rationale:

No wirebondable qualified

Wirebondable resistor networks (**future RMKHR/ CNHR**)



Sizes:	33, 48, 408, 508, 714, 816, 914 **Custom**
Ohmic Range:	10Ω - 2MΩ
TC tracking:	Down to 2ppm/°C (-55°C; +155°C)
Tolerance matching:	Down to 0.01%
Substrate:	Alumina or Silicon
Terminations materials:	Aluminum or **Gold**

Operating temperature range: -55°C; +155°C

Heritage: Being used with an option corresponding to customer's specification, in Space applications, for a decade.

Customer Evaluation

Rationale:

No wirebondable qualified

Wirebondable shunts (**future SAHR, SBHR, SCHR**)

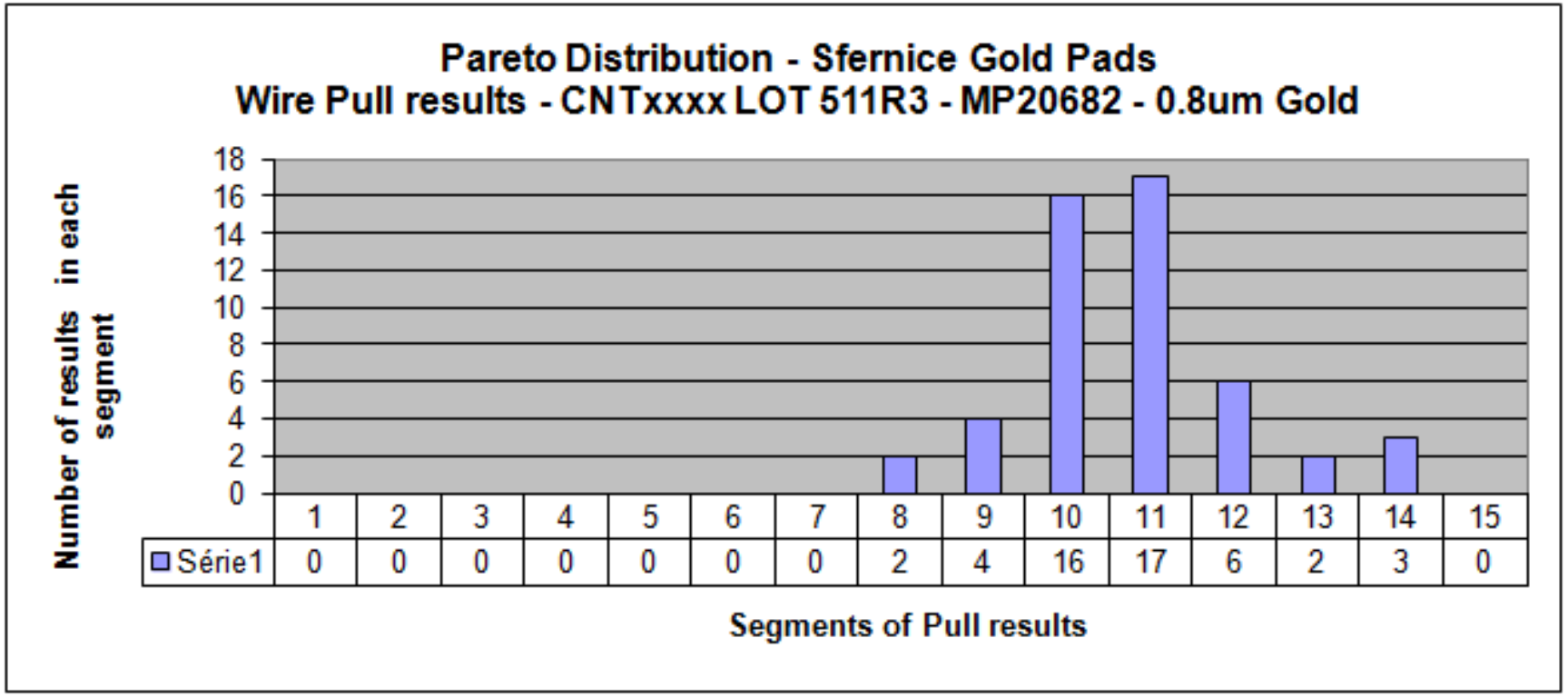
Sizes:	0606, 1212, 2020
Ohmic Range:	50mΩ - 1Ω
Temperatue Coefficient:	100ppm/°C (-55°C; +155°C)
Power Rating:	0.5W to 6W
Substrate:	Alumina
Terminations materials:	Gold

Operating temperature range: -55°C; +155°C

Heritage: Being used with an option corresponding to customer's specification, in Space applications, for a decade.

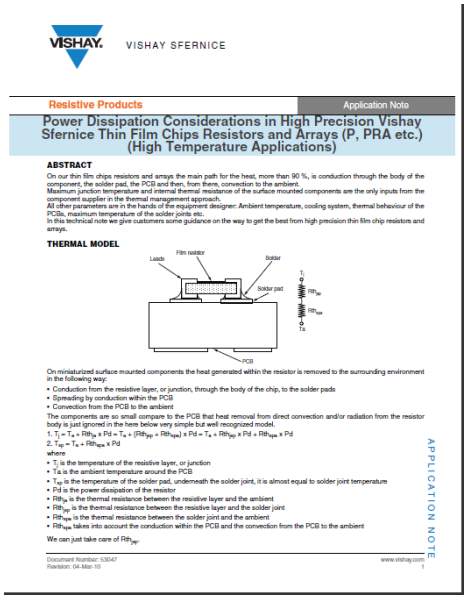
Experimental Data

Pull Test Results (Pull Force in Grams): gold wires on gold pads



Results show consistent behavior

Tools to help Designers


VISHAY SFERNICE

Resistive Products | Application Note

Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chips Resistors and Arrays (P, PRA etc.) (High Temperature Applications)

ABSTRACT

On our thin film chips resistors and arrays the main path for the heat, more than 90 %, is conduction through the body of the component, the solder pad, the PCB and then, from there, convection to the ambient.
Maximum junction temperature and internal thermal resistance of the surface mounted components are the only inputs from the component supplier in the thermal management approach.
All other parameters are in the hands of the equipment designer: Ambient temperature, cooling system, thermal behaviour of the PCBs, maximum temperature of the solder joints etc.
In this technical note we give customers some guidance on the way to get the best from high precision thin film chip resistors and arrays.

THERMAL MODEL

On miniaturized surface mounted components the heat generated within the resistor is removed to the surrounding environment in the following way:

- Conduction from the resistive layer, or junction, through the body of the chip, to the solder pads
- Spreading by conduction within the PCB
- Convection from the PCB to the ambient

The components are so small compare to the PCB that heat removal from direct convection and/or radiation from the resistor body is just ignored in the here below very simple but well recognized model.

1. $T_j = T_a + Rth_{ja} \times Pd = T_a + (Rth_{jsp} + Rth_{spa}) \times Pd = T_a + Rth_{jsp} \times Pd + Rth_{spa} \times Pd$
2. $T_{sp} = T_a + Rth_{spa} \times Pd$

where

- T_j is the temperature of the resistive layer, or junction
- Ta is the ambient temperature around the PCB
- T_{sp} is the temperature of the solder pad, underneath the solder joint, it is almost equal to solder joint temperature
- Pd is the power dissipation of the resistor
- Rth_{ja} is the thermal resistance between the resistive layer and the ambient
- Rth_{jsp} is the thermal resistance between the resistive layer and the solder joint
- Rth_{spa} is the thermal resistance between the solder joint and the ambient
- Rth_{spa} takes into account the conduction within the PCB and the convection from the PCB to the ambient

We can just take care of Rth_{jsp}.

APPLICATION NOTE

Document Number: 53047 | www.vishay.com
Revision: 04-Mar-10 | 1


VISHAY SFERNICE

Resistive Products | Application Note

Power Dissipation in High Precision Vishay Sfernice Chip Resistors and Arrays (P Thin Film, PRA Arrays, CHP Thick Film)

A. ABSTRACT

Datasheets for surface-mount components in general and for chip resistors and arrays in particular tend to offer very limited information on thermal performance. Typically they provide derating curves that are similar to the ones used for through-hole components, even though the respective heat dissipation properties of those two component types are quite different. In the larger, leaded components, heat dissipation occurs mainly by direct convection and radiation from the component to the ambient. Only a small portion of the heat is dissipated by conduction through the leads and PCB and then by convection and radiation to the ambient. Thus it makes sense to take the component body temperature as a basis for determining by how much the power needs to be derated when this temperature increases. In smaller surface-mount components such as Vishay's thin film chip resistors and arrays, by contrast, more than 90 % of the heat, is dissipated from the body of the component directly into the solder pad, from there to the PCB, and thence by convection to the ambient.
Unfortunately the only specifications on the datasheet that are key to the thermal management process are the maximum junction temperature and internal thermal resistance. Everything else depends on the system design, including the ambient temperature, cooling system, thermal behavior of the PCBs, maximum temperature of the solder joints, and so forth. This application note provides designers with additional guidance on how to get the best performance from high-precision thin film chip resistors and arrays from a thermal management point of view.

B. THERMAL MODEL

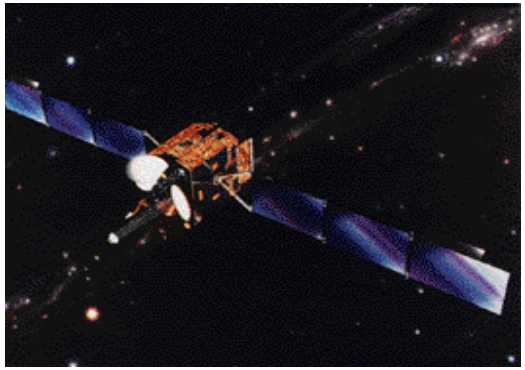
On miniaturized surface-mount components the heat generated within the resistor is dissipated to the surrounding environment in the following way:

- Conduction from the resistive layer, or junction, through the body of the chip, to the solder pads
- Spreading by conduction within the PCB
- Convection from the PCB to the ambient

APPLICATION NOTE

Document Number: 53048 | www.vishay.com
Revision: 29-Oct-09 | 1

Application Notes
Space product Selector Guide
Capability brochure



Vishay / Sfernice strategy is to be one stop shop for Space Customers
In this frame Vishay/Sfernice has run the qualification of

ESCC QML: ESCC Technology Flow Qualified Manufacturer

Vishay/Sfernice FIRST passive manufacturer qualified

Vishay Sfernice on going qualification: to offer a whole range of resistive products from 0Ω to 10M:

Thank you for your attention