Surge Current Testing and Derating for Solid Tantalum Capacitors

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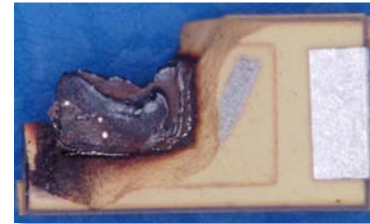
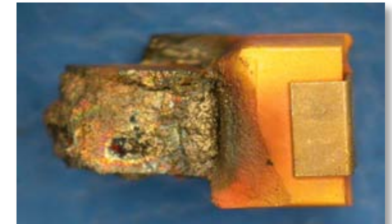
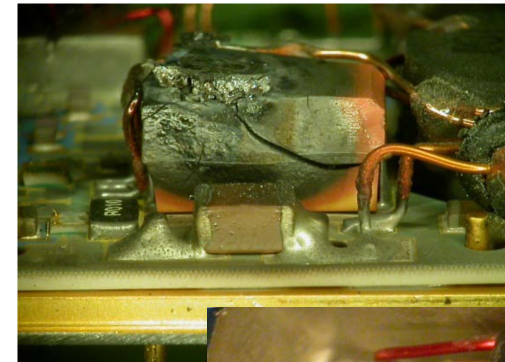
Outline

Do we need limiting resistors in series with tantalum capacitors?

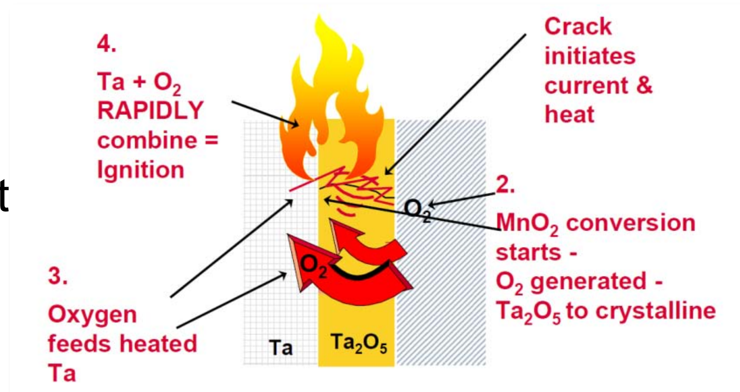



- Surge current testing (SCT).
  - Mechanism of failures.
  - History of current derating.
- MIL-PRF-55635 requirements.
- Specifics of SCT.
  - Effective resistance of the circuit, R_{eff}.
  - Correlation between R_{eff} and equivalent series resistance (ESR).
  - Effect of ESR on VBR.
- Specified and real ESR values.
- Derating of surge currents.
- Conclusion.

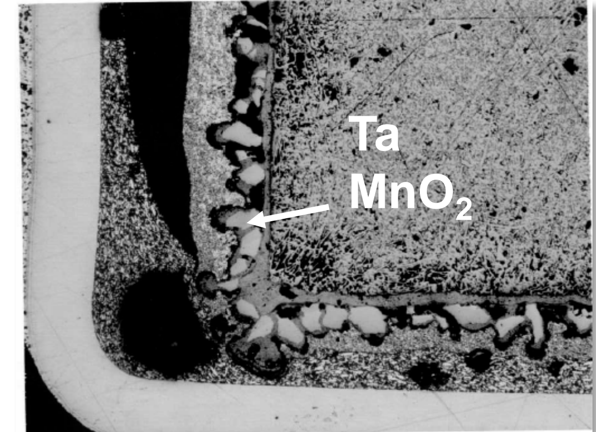


Mechanisms of Surge Current Failures

- Sustained scintillation breakdown. If current is not limited, self-healing does not have time to develop.
- Electrical oscillations in circuits with high inductance.
- Local overheating of the cathode.
- Mechanical damage to tantalum pentoxide dielectric caused by the impact of MnO_2 crystals.
- Stress-induced-generation of electron traps caused by electromagnetic forces developed by high currents.



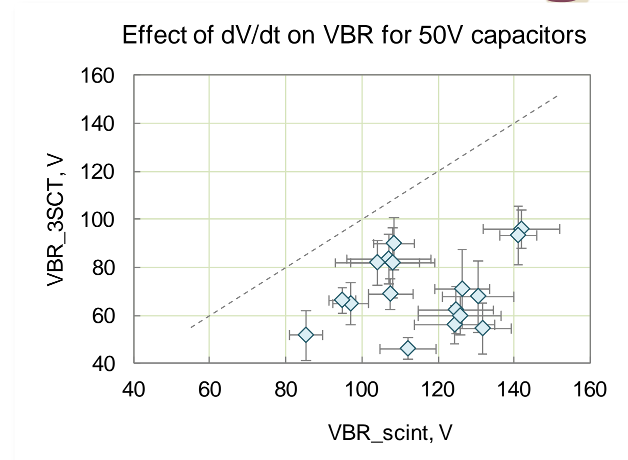
Ignition due to exothermic reaction in tantalum capacitors. Prymak 2006.



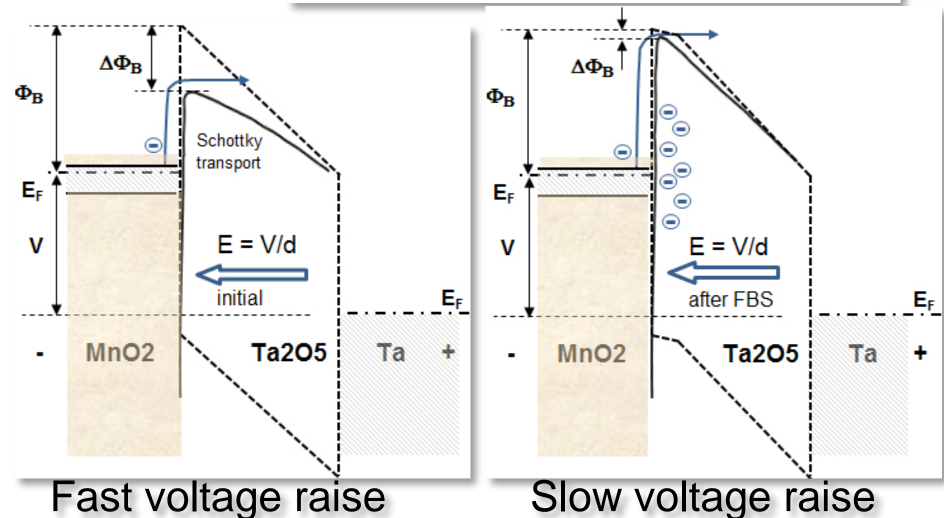
✓ All models require high currents that correspond to high rates of voltage increase.

Effect of *dV/dt* on Breakdown Voltage

- Scintillation breakdown voltage, VBR_{scint} (*dV/dt* ~ 1 to 5 V/sec) is always greater than the surge current breakdown voltage, VBR_{SCT} (dV/dt ~ 10^5 to 10^6 V/sec)
- The rate of voltage increase changes charges and electrical field at the interface.



Accumulation of electrons on traps at the MnO_2-Ta_2O_5 interface with time increases the barrier, the level of electron injection, and the probability of avalanching.



Fast voltage raise   Slow voltage raise

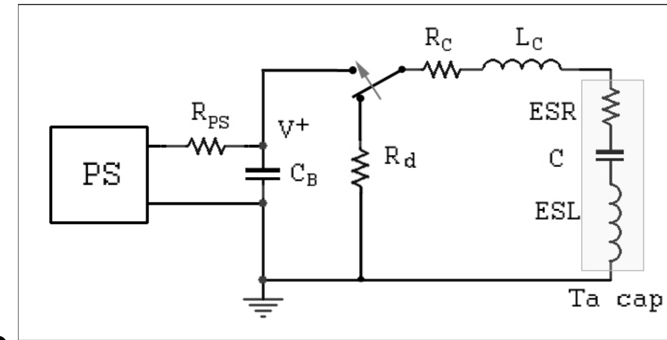
- ✓ A theory explains decreasing VBR with a rate of voltage increase.
- ✓ A resistor in series with a capacitor reduces *dV/dt* and failures.

Requirements for Limiting Resistors

- History of requirements for circuit resistance (R_{ac}):
  - In the 1960s: 3 Ω per each volt of operating voltage.
  - By the 1980s: 1 Ω per each volt.
  - From the 1990s: 0.1 Ω per volt or 1 ohm, whichever is greater.
- Manufacturers consider surge current failures as the major reason for voltage derating.
- Do we need derating of currents in addition to voltage?
- The limit for acceptable surge currents is set by the SCT conditions: the current during applications should not exceed the current during testing: $I_{appl.} < I_{test}$ *"use as tested"*

- ✓ Improvements in reliability and the need to increase the efficiency of power supply systems resulted in reduction of R_{ac}.
- ✓ Can we allow circuit designs without R_{ac}?
- ✓ Need a closer look at how the I_{test} is specified.

MIL-PRF 55365 Requirements



- SCT per MIL-PRF-55365H:
  - N_c = 4 surge cycles.
  - Energy storage capacitor, $C_B = 20 \times C_{DUT}$
  - Test voltage: VR
  - Charge time, t_{ch}, and discharge time, t_{disch}, ≥ 1sec.
  - Total DC resistance of the circuit, R_C, including the wiring, fixturing, and output impedance of the power supply should not exceed R_c = 1 Ω.
  - Measurements after SCT: DCL, C, DF (still no requirements for ESR)
  - $I_{test} \geq V_R/(R_{tc} + ESR_{spec})$, where resistance of the test circuit, $R_{tc} = 1$ Ω.
  - Failure condition: I = 1A after 1ms for $C \leq$ 330uF; 10ms for $C \leq$ 3.3mF, and 100ms for $C >$ 3.3 mF.
- Before 12/1/2012:
  - N_c = 10.
  - $t_{disch} = t_{ch}$ = 4 sec.
  - $R_c \leq$ 1.2 Ohms.
  - $C_B \geq$ 50 mF.
  - I_{test} was not addressed.

✓ New specification recognizes the role of ESR as a limiting factor for surge currents.

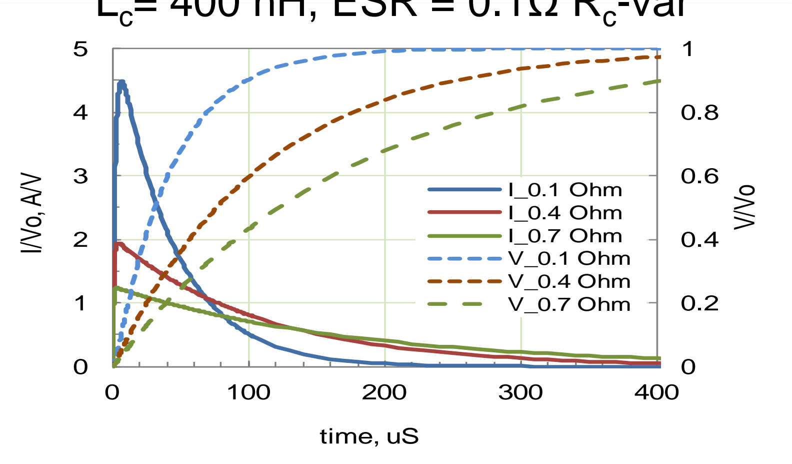
✓ Rated surge current: $$I_{surge} = \frac{V_R}{ESR_{spec} + 1}$$

✓ No specifics on I_{test} verification.

Verification of SCT Conditions

- Two methods of SCT verification:
  - measurements of voltage after some time of spike initiation;
  - measurements of a current spike amplitude.

SCT simulations for 220 µF capacitor at L_c= 400 nH, ESR = 0.1Ω R_c-var

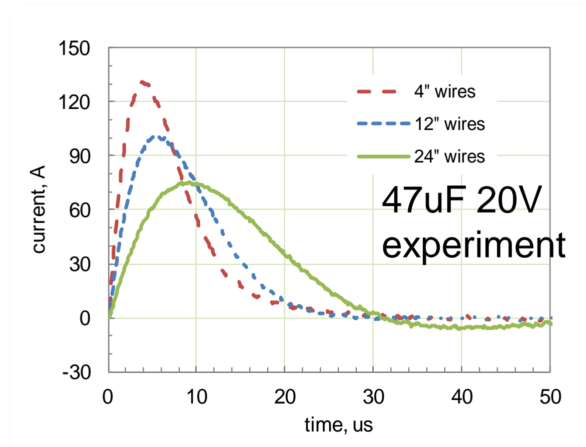


- ✓ The rate of voltage increase is critical for SCT.
- ✓ A high current spike is a byproduct of the fast voltage raise, rather than the major cause of failure.
- ✓ Even minor variations (~0.1 Ω) of R_c affect *dV/dt* and results of SCT.
- ✓ The amplitude of the current spike is the most adequate characteristic of the SCT conditions.

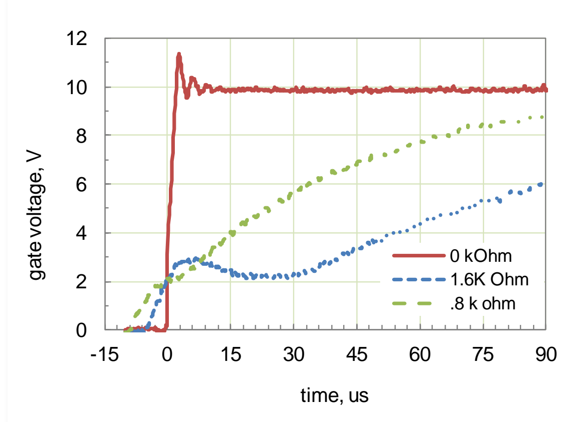
Factors Affecting SCT Results

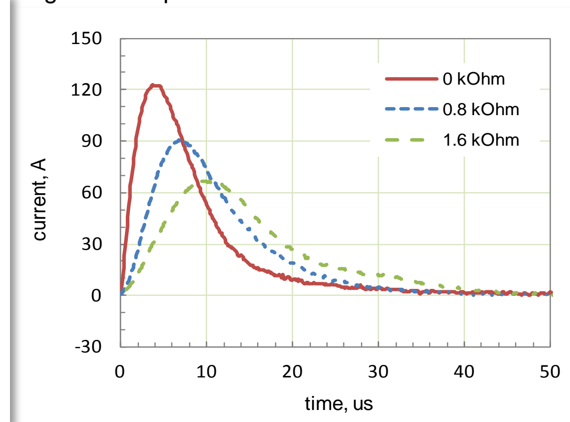
- R_c includes resistance of wires and contacts.
- The length of wires affects inductance.
- Type of switch.
- The rate of voltage increase in case of FET.

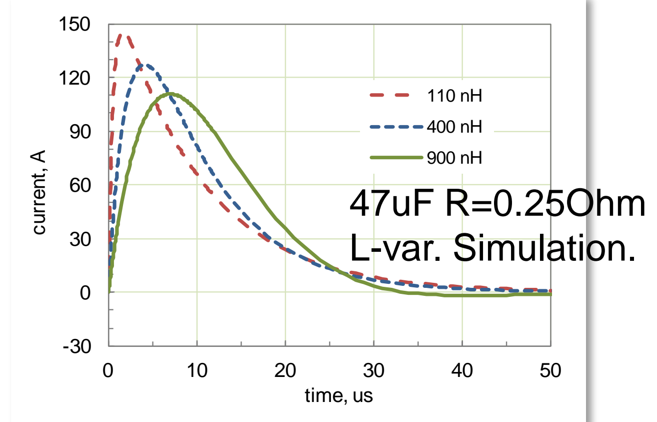
Effect of wire length



Effect of resistance to FET gate on V_g and I_{sp} for 47uF 20V capacitors

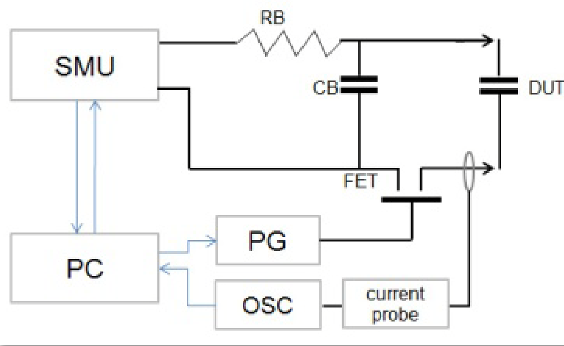


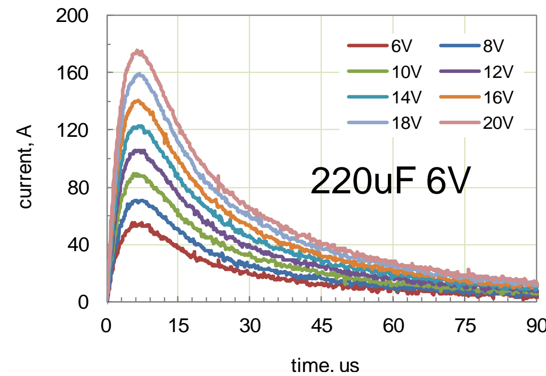


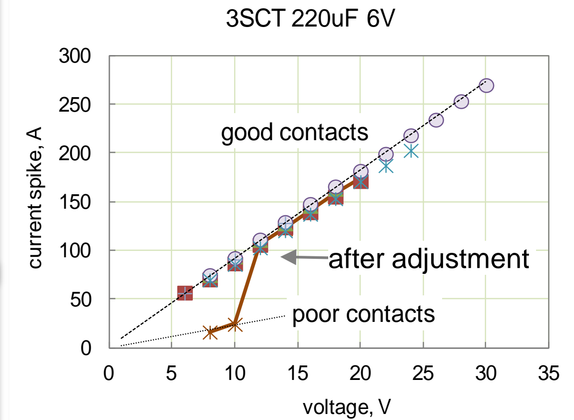


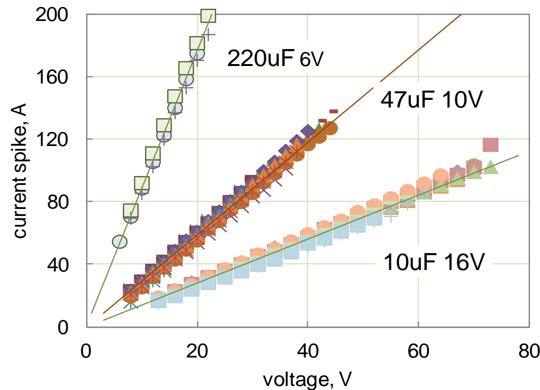
✓ SCT test conditions should be optimized by maximizing I_{sp}.

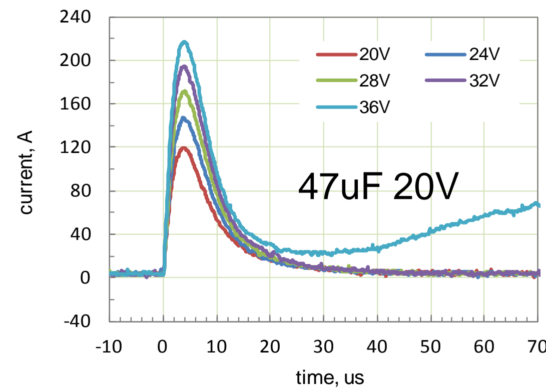
Effective Resistance of the Circuit









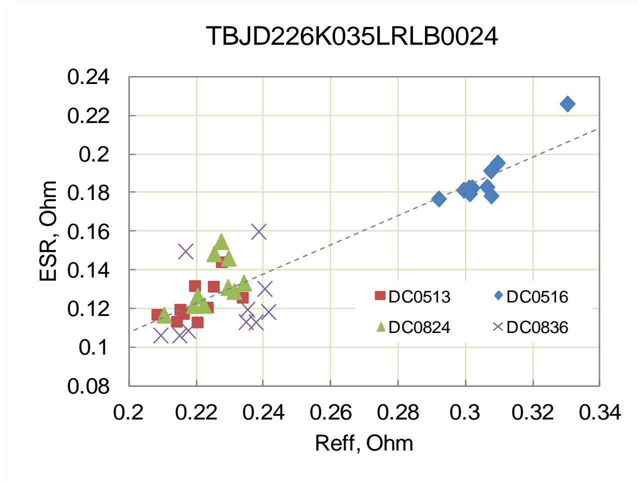


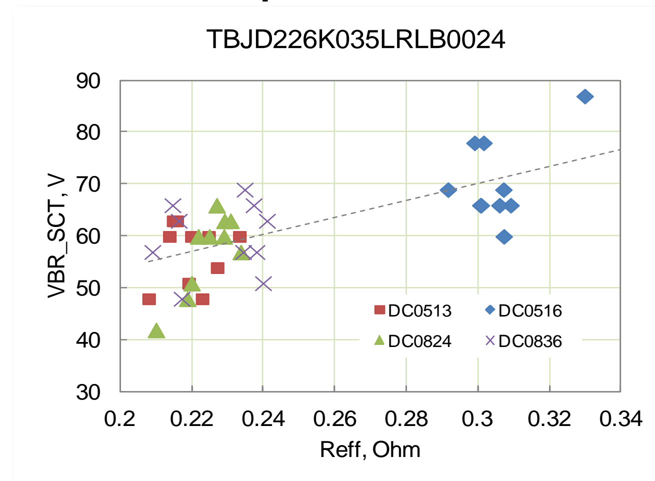
Test anomalies, e.g. poor contacts, can be revealed by I_{sp}(V) curves

- ✓ I_{sp} increases linearly with voltage allowing for calculations of the effective resistance of the circuit, R_{eff}.
- ✓ R_{eff} corresponds to the impedance of the circuit and includes R_c, *ESR*, resistance of contacts, and circuit inductance, L_c.

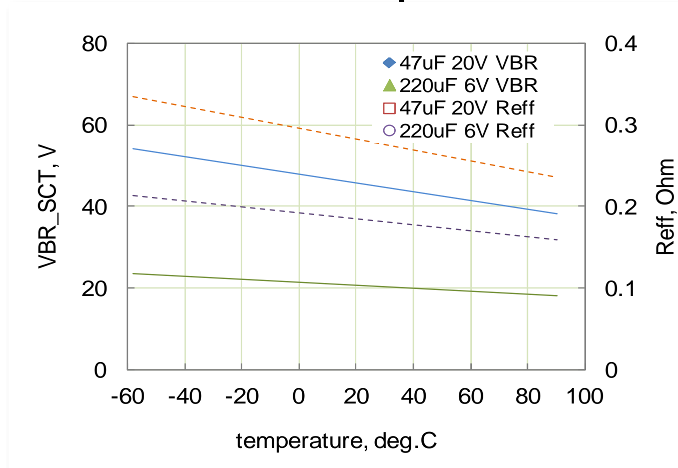
Effect of R_{eff} on Breakdown Voltage

- Different lot date codes of 22 μF 35V capacitors.



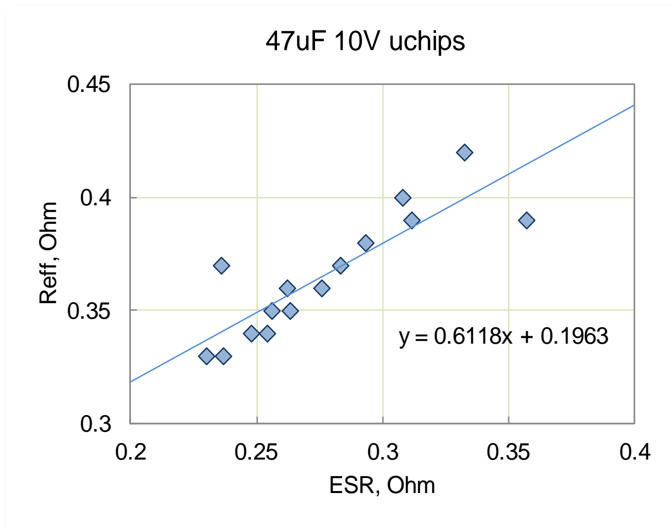


- Effect of temperature

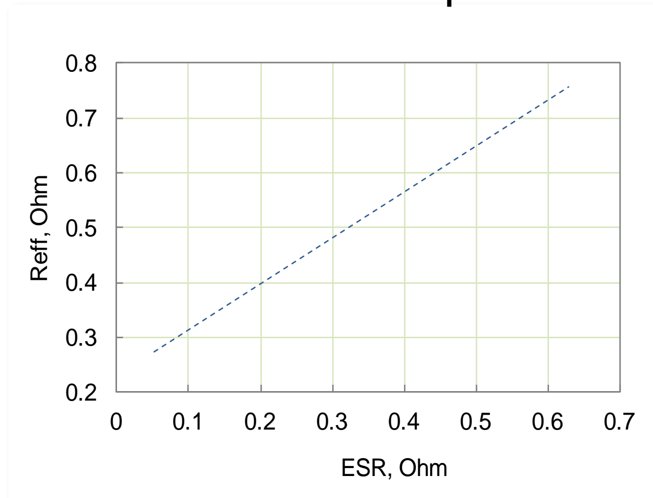


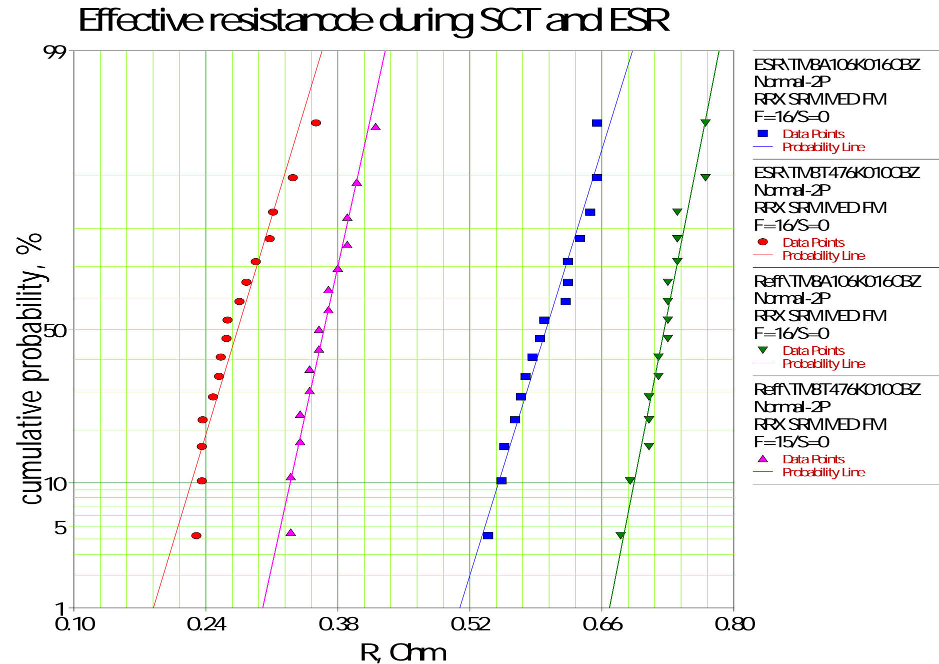
- ✓ Parts with larger *ESR* had greater VBR.
- ✓ Temperature decreases ESR resulting in lower VBR.
- ✓ An increase in R_{eff} by ~0.1 Ω results in increase of *VBR ~10%.*

Correlation between ESR and R_{eff}



20 lots of HV capacitors





- ✓ Effective resistance of SCT:

$$R_{eff} = \frac{V_R}{I_{sp}} \approx R_c + ESR$$

- ✓ Optimized set-up: R_c is in the range from 0.1 Ω to 0.2 Ω.

Application vs. Test Conditions

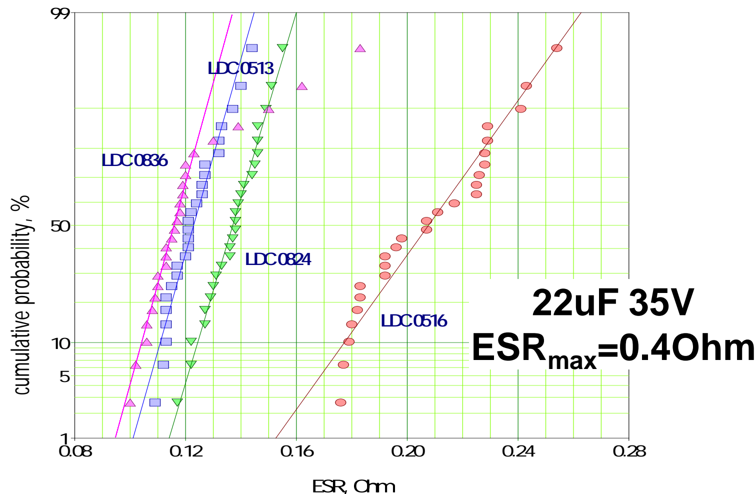
- Typical application conditions:
  - No limiting resistors, minimal inductance.
  - No contact resistance.
  - Resistance of the circuit, R_{ac}, is minimal.
- ➢ The current is limited mostly by ESR.
- Surge Current Test conditions:
  - Contact resistance of fixtures.
  - Limiting resistor (up to 1 Ω).
  - Relatively long wires and inductance.
  - No requirements for I_{test} verification.
- ➢ Parts with poor contacts in the fixture can pass the testing.

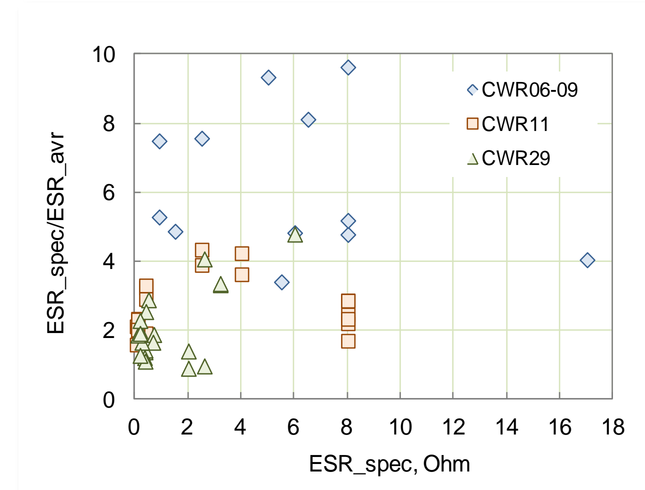
Example:

- A 15µF 10V CWR06 capacitor with specified ESR=2.5Ω and real ESR = 0.5Ω is used in a 5V line.
- During application the part can experience a spike:
  $I_{appl} = 5/0.5 = 10$ A.
- During the testing it will be verified to the current:
  $I_{test} \geq V_R/(R_{tc} + ESR_{spec})$
  $I_{test} = 10/(1+2.5) = 2.8$ A

✓ There might be a substantial difference in inrush currents between application and test conditions.

Real and Specified Values of ESR





- ✓ ESR distribution can be described by a normal function.
- ✓ The distributions are rather tight: STD ~ 30% to 50% of ESR_{avr}.
- ✓ Different lots of the same part type might have different ESR.
- ✓ Only a maximum value of ESR is limited. Real ESR values might not correlate with the limit.
- ✓ $N_{avr} = ESR_{limit}/ESR_{avr}$
- ✓ CWR06 have N_{avr} ~7, CWR29 ~2.

	CWR06	CWR11	CWR29
N_{avr}	6.92	2.72	2.04
STD	2.64	0.83	1.02
Lots QTY	14	20	23

Surge Current Derating

- SCT requirements (rated current): $I_{test} = \frac{V_R}{R_{test} + ESR_{spec}}$,
  R_{test} = 1 Ω.
- During applications, possible current spike: $I_a = \frac{\alpha \times V_R}{R_{ac} + ESR}$,
  derating $\alpha = V_a / V_R$, R_{ac} – additional resistance
- Derating Criterion: $I_a < \beta \times I_{test}$, where $\beta \leq 1$ is the current derating coefficient.
- Substitution gives: $R_{ac} > \frac{\alpha}{\beta} \times R_{test} + \frac{\alpha}{\beta} \times ESR_{spec} - ESR$
- At low voltages capacitors can tolerate much higher current spikes, so there is no need in derating currents on the top of voltage derating => $R_{ac} > \alpha \times R_{test} + \alpha \times ESR_{spec} - ESR$

✓ R_{ac} is not necessary if $I_{ps_max} < I_{test}$ at a clamping time $\tau \leq 10$ us.

✓ Unless SCT is done at the optimized conditions, or $\alpha < \frac{ESR}{ESR_{spec} + R_{test}}$ additional resistance is necessary.

When Additional Resistor is Necessary?

- If SCT is carried out at the optimized conditions (R_{tc}< 0.5 Ω, and I_{sp} is verified at real ESR values), then

$$R_{ac} > \alpha \times R_{tc} + (\alpha - 1) \times ESR$$

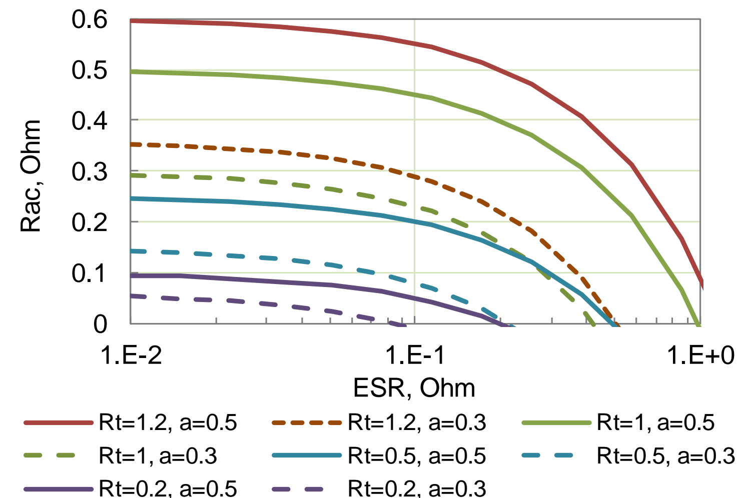
- If R_{ac} < 0.05 Ω, no resistance required.

✓ At the existing SCT requirements per M55365, additional resistance is necessary in most cases.

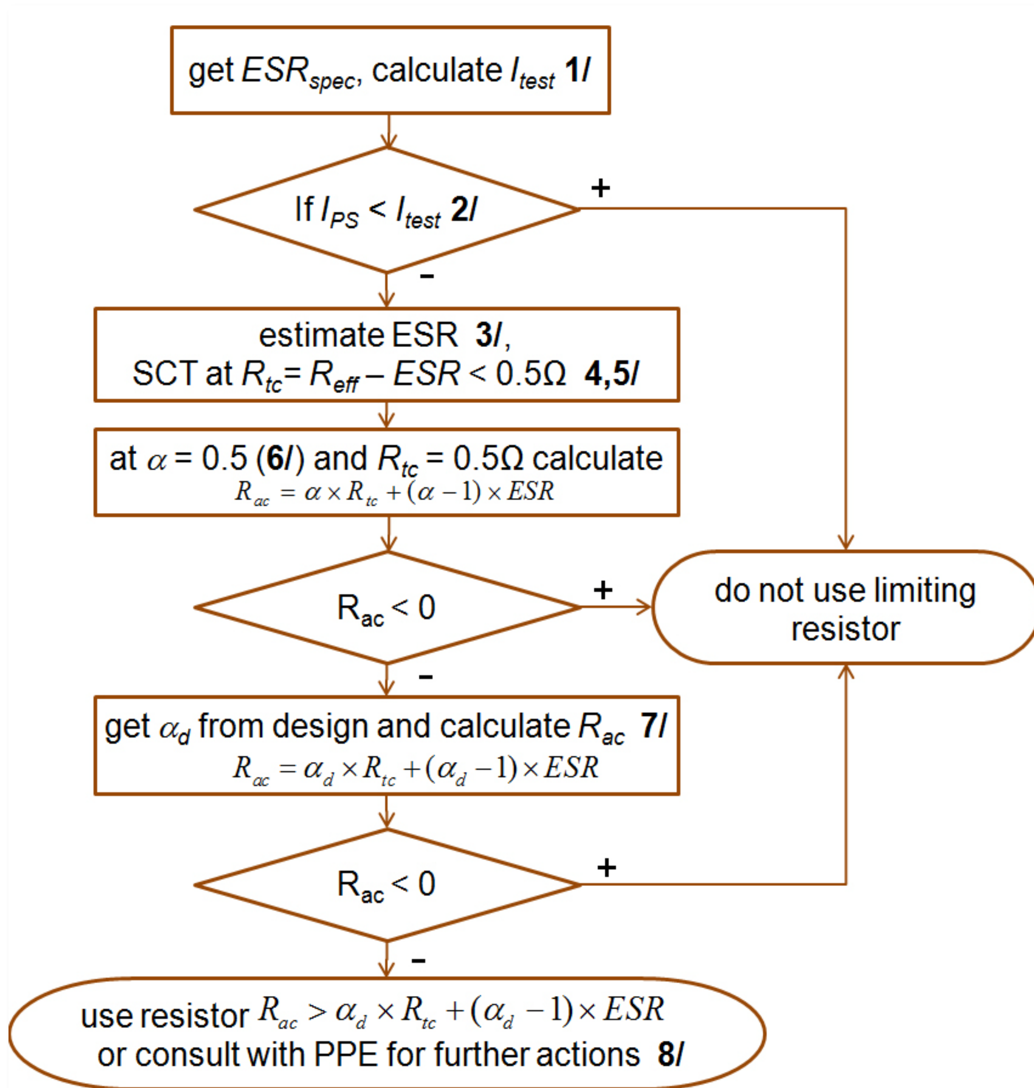
✓ If SCT is carried out at $R_{tc} = R_{eff} - ESR < 0.5$ Ω, the additional resistor is not necessary if

$$(1 - \alpha) \times ESR > \alpha \times R_{tc}$$

Required series resistance at different ESR, R_{tc} and α



Algorithm for Surge Current Derating



1/ $I_{test} = \dfrac{V_R}{R_{tc} + ESR_{spec}}$, $R_{tc} = 1\ \Omega$

2/ In case of using power supplies (PS) with current compliance, make sure that the clamping time $\tau \leq 10$us. $I_{PS} = I_{max}$ PS.

3/ Estimate ESR as ESR_{spec}/N, where N=7, 3, 2 for CWR06/11/29 respectively.

4/ $R_{eff} = V_R/I_{sp}$, where I_{sp} is the surge current spike amplitude.

5/ SCT should be carried out at a min. wire length, no limiting resistors, and I_{sp} should be verified to be greater than

$$I_{sp} > V_R/(0.5 + ESR)$$

6/ Standard voltage derating: $\alpha = 0.5$

7/ Actual derating: $\alpha_d = V_{app}/V_R$

8/ Suggestions for further actions:
- experimental data for ESR,
- calculate actual $R_{tc} = R_{eff} - ESR$,
- SCT at greater voltage levels, …

Conclusion

- Tantalum capacitors manufactured per MIL-PRF-55365 might fail because the surge current test conditions during manufacturing are less stressful compared to application conditions.
- Measurements of current spike amplitudes during SCT allow for estimations of the effective resistance of the test circuit, R_{eff}, and should be used to assure that the parts are properly stressed during the testing. Acceptable test conditions can be determined as $R_{eff} \leq 0.5 + ESR$.
- An algorithm and procedures necessary for selection of limiting resistors to derate surge currents or for making a decision to use tantalum capacitors without additional resistors are suggested.