Surge Current Testing and Derating for Solid Tantalum Capacitors

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Outline

Do we need limiting resistors in series with tantalum capacitors?

- Surge current testing (SCT).
  - Mechanism of failures.
  - History of current derating.
- MIL-PRF-55635 requirements.
- Specifics of SCT.
  - Effective resistance of the circuit, $R_{eff}$.
  - Correlation between $R_{eff}$ and equivalent series resistance (ESR).
  - Effect of ESR on VBR.
- Specified and real ESR values.
- Derating of surge currents.
- Conclusion.
Mechanisms of Surge Current Failures

- Sustained scintillation breakdown. If current is not limited, self-healing does not have time to develop.
- Electrical oscillations in circuits with high inductance.
- Local overheating of the cathode.
- Mechanical damage to tantalum pentoxide dielectric caused by the impact of MnO₂ crystals.
- Stress-induced-generation of electron traps caused by electromagnetic forces developed by high currents.

All models require high currents that correspond to high rates of voltage increase.

Ignition due to exothermic reaction in tantalum capacitors. Prymak 2006.
Effect of $dV/dt$ on Breakdown Voltage

- Scintillation breakdown voltage, $VBR_{scint}$ ($dV/dt \sim 1 \text{ to } 5 \text{ V/sec}$) is always greater than the surge current breakdown voltage, $VBR_{SCT}$ ($dV/dt \sim 10^5 \text{ to } 10^6 \text{ V/sec}$)

- The rate of voltage increase changes charges and electrical field at the interface.

  Accumulation of electrons on traps at the MnO$_2$-Ta$_2$O$_5$ interface with time increases the barrier, the level of electron injection, and the probability of avalanching.

- A theory explains decreasing VBR with a rate of voltage increase.
- A resistor in series with a capacitor reduces $dV/dt$ and failures.
Requirements for Limiting Resistors

- History of requirements for circuit resistance ($R_{ac}$):
  - In the 1960s: 3 Ω per each volt of operating voltage.
  - By the 1980s: 1 Ω per each volt.
  - From the 1990s: 0.1 Ω per volt or 1 ohm, whichever is greater.

- Manufacturers consider surge current failures as the major reason for voltage derating.

- Do we need derating of currents in addition to voltage?

- The limit for acceptable surge currents is set by the SCT conditions: the current during applications should not exceed the current during testing: $I_{appl.} < I_{test}$ “use as tested”

- Improvements in reliability and the need to increase the efficiency of power supply systems resulted in reduction of $R_{ac}$.
- Can we allow circuit designs without $R_{ac}$?
- Need a closer look at how the $I_{test}$ is specified.
MIL-PRF 55365 Requirements

- SCT per MIL-PRF-55365H:
  - $N_c = 4$ surge cycles.
  - Energy storage capacitor, $C_B = 20 \times C_{DUT}$
  - Test voltage: $V_R$
  - Charge time, $t_{ch}$, and discharge time, $t_{disch}$, $\geq 1$ sec.
  - Total DC resistance of the circuit, $R_C$, including the wiring, fixturing, and output impedance of the power supply should not exceed $R_c = 1 \ \Omega$.
  - Measurements after SCT: DCL, C, DF (still no requirements for ESR)
  - $I_{test} \geq \frac{V_R}{(R_{tc} + ESR_{spec})}$, where resistance of the test circuit, $R_{tc} = 1 \ \Omega$.
  - Failure condition: $I = 1$A after 1ms for $C \leq 330\mu$F; 10ms for $C \leq 3.3\text{mF}$, and 100ms for $C > 3.3 \text{ mF}$.

- Before 12/1/2012:
  - $N_c = 10$.
  - $t_{disch} = t_{ch} = 4$ sec.
  - $R_c \leq 1.2$ Ohms.
  - $C_B \geq 50 \text{ mF}$.
  - $I_{test}$ was not addressed.

✓ New specification recognizes the role of ESR as a limiting factor for surge currents.
✓ Rated surge current: $I_{surge} = \frac{V_R}{ESR_{spec} + 1}$
✓ No specifics on $I_{test}$ verification.
Verification of SCT Conditions

- Two methods of SCT verification:
  - measurements of voltage after some time of spike initiation;
  - measurements of a current spike amplitude.

- The rate of voltage increase is critical for SCT.
- A high current spike is a byproduct of the fast voltage raise, rather than the major cause of failure.
- Even minor variations (~0.1 Ω) of $R_c$ affect $dV/dt$ and results of SCT.
- The amplitude of the current spike is the most adequate characteristic of the SCT conditions.
Factors Affecting SCT Results

- $R_c$ includes resistance of wires and contacts.
- The length of wires affects inductance.
- Type of switch.
- The rate of voltage increase in case of FET.

Effect of resistance to FET gate on $V_g$ and $I_{sp}$ for 47uF 20V capacitors

SCT test conditions should be optimized by maximizing $I_{sp}$.
Effective Resistance of the Circuit

- $I_{sp}$ increases linearly with voltage allowing for calculations of the effective resistance of the circuit, $R_{eff}$.
- $R_{eff}$ corresponds to the impedance of the circuit and includes $R_c$, $ESR$, resistance of contacts, and circuit inductance, $L_c$.

Test anomalies, e.g. poor contacts, can be revealed by $I_{sp}(V)$ curves.
Effect of $R_{\text{eff}}$ on Breakdown Voltage

- Different lot date codes of 22 µF 35V capacitors.

- Effect of temperature
  - Parts with larger $ESR$ had greater $VBR$.
  - Temperature decreases $ESR$ resulting in lower $VBR$.
  - An increase in $R_{\text{eff}}$ by $\sim$0.1Ω results in increase of $VBR$ $\sim$10%.

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**Graphs:**

1. Graph showing $ESR$ vs $Reff$ for different parts.
2. Graph showing $VBR_SCT$ vs $Reff$ for different temperatures.
3. Graph showing $VBR_SCT$ vs temperature for different capacitance values.

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**Notes:**

- ESA Sept. 2013
- NASA Electronic Parts and Packaging (NEPP) Program
Correlation between ESR and $R_{eff}$

Effective resistance of SCT:

$$R_{eff} = \frac{V}{I_{sp}} \approx R_c + ESR$$

Optimized set-up: $R_c$ is in the range from 0.1 $\Omega$ to 0.2 $\Omega$. 

20 lots of HV capacitors
Application vs. Test Conditions

- **Typical application conditions:**
  - No limiting resistors, minimal inductance.
  - No contact resistance.
  - Resistance of the circuit, $R_{ac}$, is minimal.
  - The current is limited mostly by ESR.

- **Surge Current Test conditions:**
  - Contact resistance of fixtures.
  - Limiting resistor (up to 1 Ω).
  - Relatively long wires and inductance.
  - No requirements for $I_{test}$ verification.

- **Parts with poor contacts in the fixture can pass the testing.**

There might be a substantial difference in inrush currents between application and test conditions.

**Example:**

- A 15µF 10V CWR06 capacitor with specified ESR=2.5Ω and real ESR = 0.5Ω is used in a 5V line.
- During application the part can experience a spike:
  \[ I_{appl} = \frac{5}{0.5} = 10 \text{ A} \]
- During the testing it will be verified to the current:
  \[ I_{test} \geq \frac{V}{R_{tc} + ESR_{spec}} \]
  \[ I_{test} = \frac{10}{1+2.5} = 2.8 \text{ A} \]
**Real and Specified Values of ESR**

- ESR distribution can be described by a normal function.
- The distributions are rather tight: STD ~ 30% to 50% of ESR\(_{avr}\).
- Different lots of the same part type might have different ESR.
- Only a maximum value of ESR is limited. Real ESR values might not correlate with the limit.

\[ N_{avr} = \frac{ESR_{limit}}{ESR_{avr}} \]

- CWR06 have \(N_{avr}\) ~7, CWR29 ~2.

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<th>CWR06</th>
<th>CWR11</th>
<th>CWR29</th>
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<td>(N_{avr})</td>
<td>6.92</td>
<td>2.72</td>
<td>2.04</td>
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<tr>
<td>STD</td>
<td>2.64</td>
<td>0.83</td>
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<tr>
<td>Lots QTY</td>
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22uF 35V
ESR\(_{max}\) = 0.4 Ohm

ESR, Ohm
cumulative probability, %

LDC 0516
LDC 0824
LDC 0836
LDC 0513

ESR\(_{spec}/ESR_{avr}\)

LDC 0516
LDC 0824
LDC 0836

CWR06-09
CWR11
CWR29

ESA Sept. 2013

NASA Electronic Parts and Packaging (NEPP) Program
Surge Current Derating

- SCT requirements (rated current): $I_{test} = \frac{V_R}{R_{test} + ESR_{spec}}$, $R_{test} = 1 \, \Omega$.

- During applications, possible current spike: $I_a = \frac{\alpha \times V_R}{R_{ac} + ESR}$, $\alpha = \frac{V_a}{V_R}$, $R_{ac}$ – additional resistance.

- Derating Criterion: $I_a < \beta \times I_{test}$, where $\beta \leq 1$ is the current derating coefficient.

- Substitution gives: $R_{ac} > \frac{\alpha}{\beta} \times R_{test} + \frac{\alpha}{\beta} \times ESR_{spec} - ESR$

- At low voltages capacitors can tolerate much higher current spikes, so there is no need in derating currents on the top of voltage derating $\Rightarrow R_{ac}$ is not necessary if $I_{ps\_max} < I_{test}$ at a clamping time $\tau \leq 10 \, \mu s$.

- Unless SCT is done at the optimized conditions, or $\alpha < \frac{ESR}{ESR_{spec} + R_{test}}$ additional resistance is necessary.
When Additional Resistor is Necessary?

- If SCT is carried out at the optimized conditions ($R_{tc} < 0.5 \, \Omega$, and $I_{sp}$ is verified at real ESR values), then

$$R_{ac} > \alpha \times R_{tc} + (\alpha - 1) \times ESR$$

- If $R_{ac} < 0.05 \, \Omega$, no resistance required.

✔ At the existing SCT requirements per M55365, additional resistance is necessary in most cases.

✔ If SCT is carried out at $R_{tc} = R_{eff} - ESR < 0.5 \, \Omega$, the additional resistor is not necessary if

$$\left(1 - \alpha\right) \times ESR > \alpha \times R_{tc}$$

Required series resistance at different ESR, $R_{tc}$ and $\alpha$
Algorithm for Surge Current Derating

1/ \( I_{test} = \frac{V_R}{R_{tc} + ESR_{spec}} \), \( R_{tc} = 1 \Omega \)

2/ In case of using power supplies (PS) with current compliance, make sure that the clamping time \( \tau \leq 10\text{us} \). \( I_{PS} = I_{max\ PS} \).

3/ Estimate ESR as \( ESR_{spec}/N \), where \( N=7, 3, 2 \) for CWR06/11/29 respectively.

4/ \( R_{eff} = \frac{V_R}{I_{sp}} \), where \( I_{sp} \) is the surge current spike amplitude.

5/ SCT should be carried out at a min. wire length, no limiting resistors, and \( I_{sp} \) should be verified to be greater than \( I_{sp} > \frac{VR}{0.5 + ESR} \).

6/ Standard voltage derating: \( \alpha = 0.5 \)

7/ Actual derating: \( \alpha_d = \frac{V_{app}}{\sqrt{V_R}} \)

8/ Suggestions for further actions:
   - experimental data for ESR,
   - calculate actual \( R_{tc} = R_{eff} - ESR \),
   - SCT at greater voltage levels, …
Conclusion

- Tantalum capacitors manufactured per MIL-PRF-55365 might fail because the surge current test conditions during manufacturing are less stressful compared to application conditions.

- Measurements of current spike amplitudes during SCT allow for estimations of the effective resistance of the test circuit, $R_{eff}$, and should be used to assure that the parts are properly stressed during the testing. Acceptable test conditions can be determined as $R_{eff} \leq 0.5 + ESR$.

- An algorithm and procedures necessary for selection of limiting resistors to derate surge currents or for making a decision to use tantalum capacitors without additional resistors are suggested.