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STUDY OF RADIATION EFFECTS IN CRYOGENIC ELECTRONICS AND ADVANCED SEMICONDUCTOR MATERIALS

ESTEC Contract 11938/96/NL/NB

IMEC, Leuven, Belgium

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Project Structure

- Project timing : May 97 - April 00

- 2 Activities:

RADIATION EFFECTS IN CRYOGENIC ELECTRONICS

- Presentation day ESA - 2000
- ESA Deliverable - Literature Overview
- “Low Temperature Electronics- Physics, Devices, Circuits and Applications”, Academic Press, 2000

RADIATION EFFECTS IN ADVANCED MATERIALS

- ESA Deliverable - Literature Overview
- Book in preparation - Springer Verlag 2001

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Final Presentation Day 2001

FOCUSING ON THE MAIN EXPERIMENTAL WORK
PERFORMED DURING THE SECOND ACTIVITY

Radiation performance of Deep Submicron CMOS Technologies for Space Applications

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ESTEC, Noordwijk, The Netherlands

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Outline

- **Introduction**

COTS approach

Trends in scaling: ITRS Roadmap

- **Impact Scaling on Radiation Hardness**

Different radiation mechanisms: NIEL & LET

Importance of ionization damage

Short channel effects ▶ Gate length dependence?

- **Process Modules & Radiation Hardness**

Isolation schemes

Gate dielectrics

- **Conclusions**

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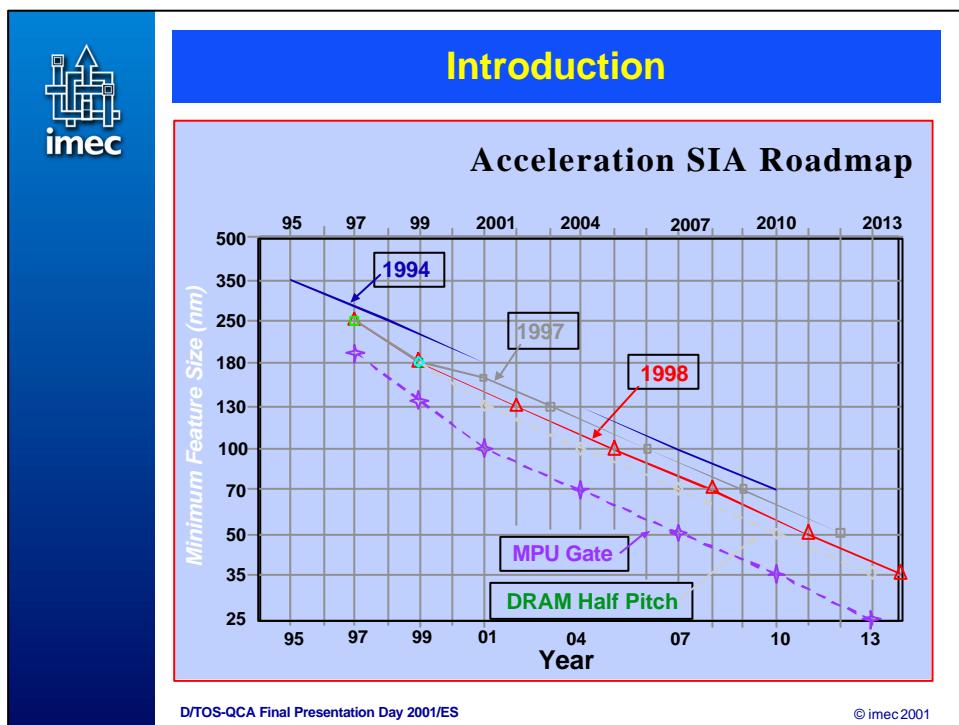
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Introduction

- **COTS Approach**
 - Cost effectiveness
 - Use state-of-the-art components and circuits
 - Lifetime of a technology
 - Radiation hardness ?
- **Trend in downscaling**
 - Moore's law
 - ITRS roadmap

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Impact Downscaling on Radiation Hardness

- **Physical Mechanisms of Radiation Response**
 - Ionization damage
 - electron-hole pairs in the oxide
 - Linear Energy Transfer (LET)
 - Displacement damage
 - radiation-induced lattice defects
 - Non-Ionizing Energy Loss (NIEL)
 - Single Event Upsets (SEU)
 - proton or heavy ions
 - scaling: natural alpha particles limit
 - 3D models needed
 - Single Event Latch-up (SEL)
 - reduces for thinner epilayer thickness
 - worse for scaled down technologies

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Scaling: Ionization Damage

- Dominant mechanism in CMOS devices
- Flatband voltage shift due to total dose
 - Formula Johnston (IEEE Nucl Sci, 45, 1339, 1998)
$$\Delta V_{ot} = \Delta V_T = \frac{q}{\lambda_{ox}\lambda_0} [b(t_{ox} - 2h_1)] \frac{t_{ox}}{2}$$
 - h_1 : distance in oxide for the trapped holes $\rightarrow 3\text{nm}$
 - oxides $< 6\text{ nm}$: no net hole trapping

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Scaling: Ionization Damage

- **Radiation-Induced Leakage Current (RILC)**
Dose in the Mrad(Si) range
- **Charge Trapping in the Field Oxide !**
Important in the bird's beak region
function oxide profile
- **Interface Trap Generation**
Remains important for scaled down technologies

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Radiation-Induced Leakage Current (RILC)

M. Ceschia et al., IEEE Trans. NS, 45, 2375 (1998)

The graph plots the radiation-induced leakage current I_g (in A/cm^2) on a logarithmic y-axis (from 10^{-10} to 10^{-4}) against the electric field $|E_{\text{ox}}|$ (in MV/cm) on the x-axis (from 2 to 8). Multiple curves are shown, representing different doses of radiation. The curves are labeled with their respective doses: "fresh" (representing 0 dose), "4", and "50". The current increases with both the electric field and the dose.

Dose (Mrad(Si)):

I_g (A/cm^2)

$|E_{\text{ox}}|$ (MV/cm)

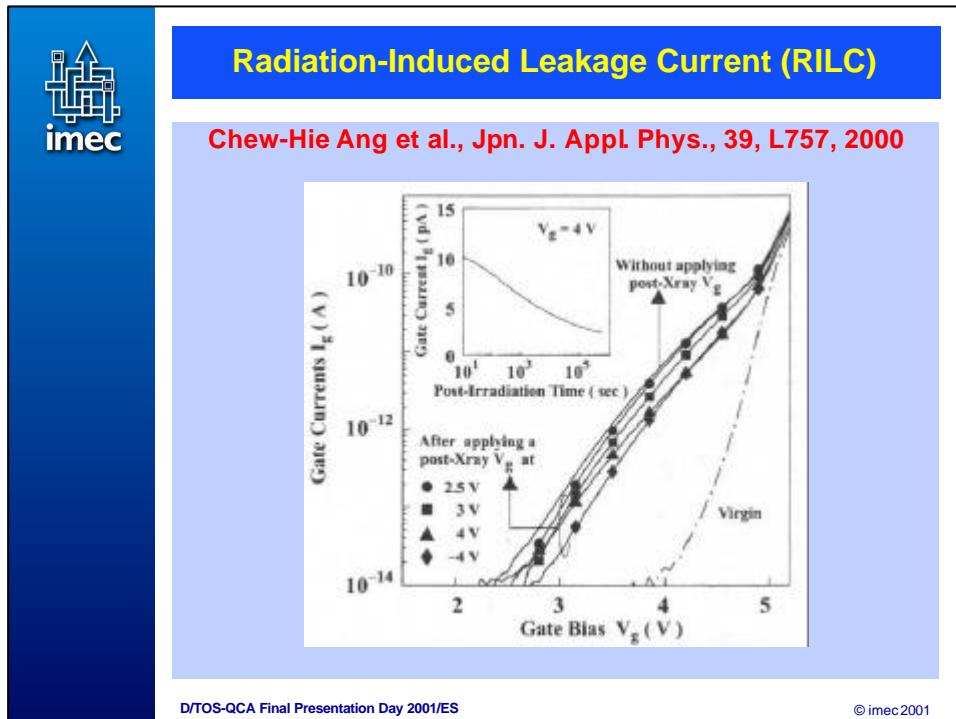
fresh

50

4

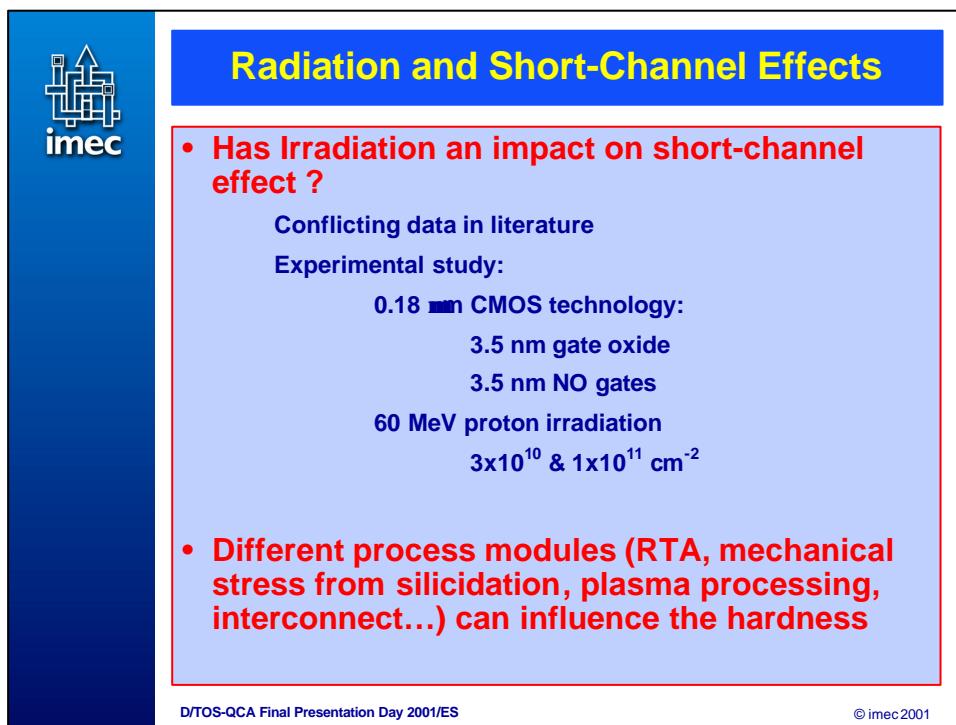
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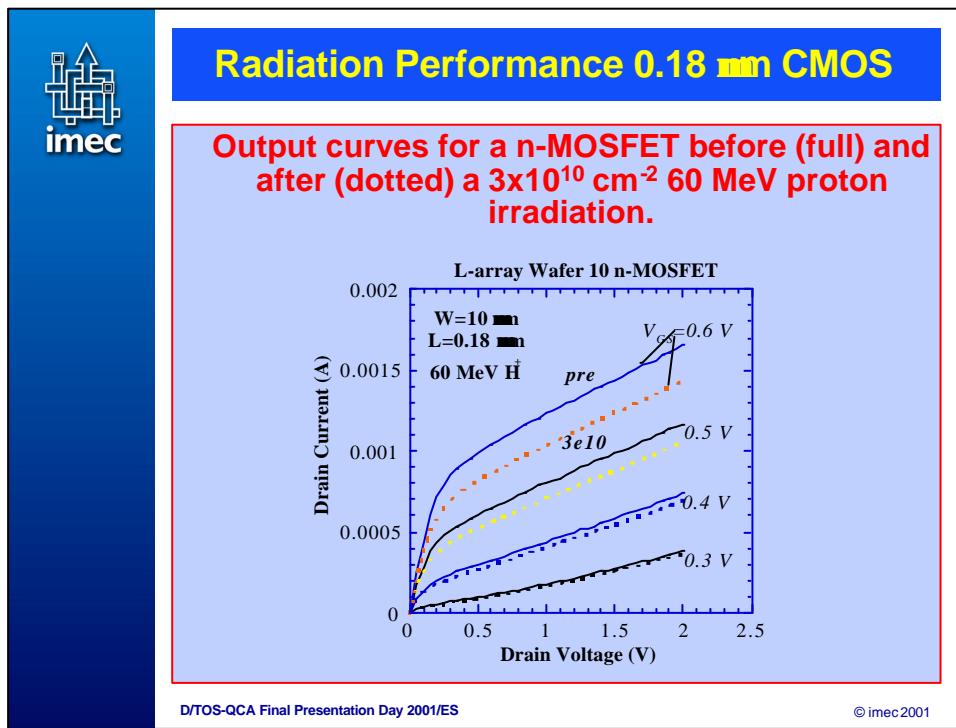
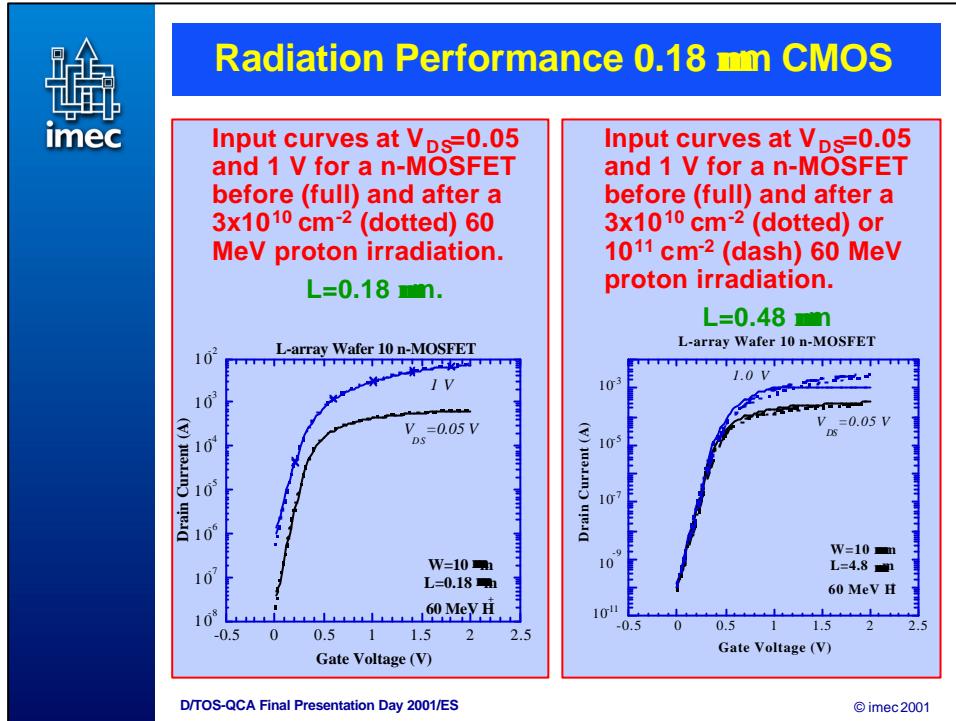


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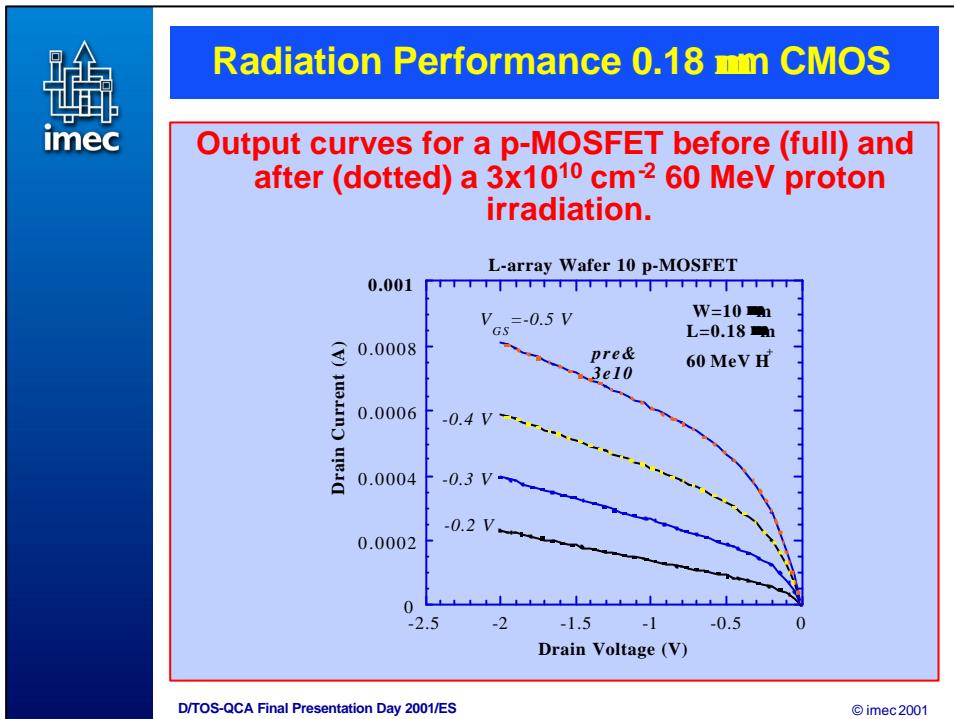
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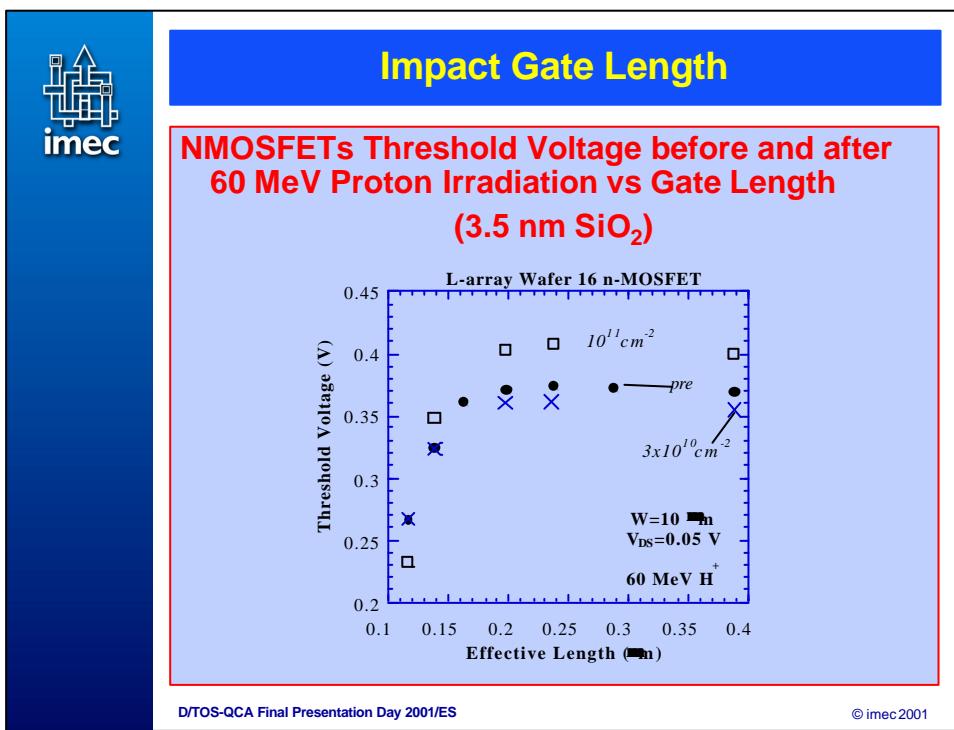
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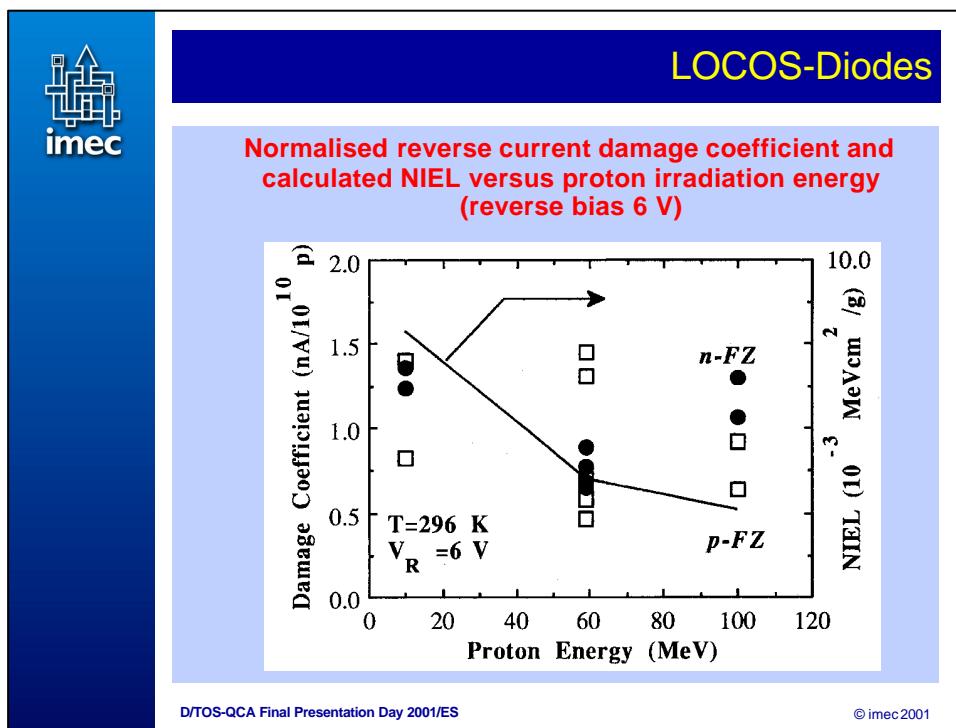
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Isolation Schemes

- **LOCal Oxidation of Silicon (LOCOS)**
Most commonly used technique
Useful down to 0.5 μm
- **Poly-Buffered and Poly Encapsulated LOCOS**
Useful down to 0.25 μm
- **Shallow Trench Isolation**
Required for 0.18 μm and smaller
Stress generation near the corners
Corner radius, transition angle, degree overfilling
Shaneyfelt et al. (IEEE Trans. NS, 45, 2584, 1998)
Claeys et al. (Nasda Conference, Tsukuba 2000)

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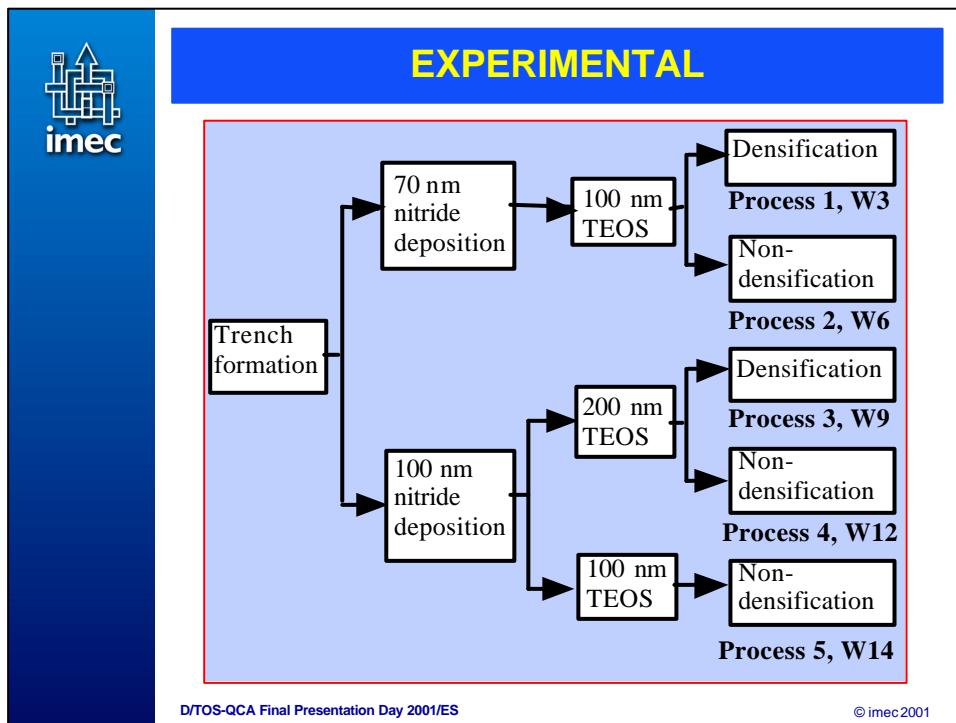
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EXPERIMENTAL

- Standard IMEC 0.18 μm CMOS process
- STI Module
 - Dry etching trenches
 - Oxidation of the trench sidewalls
 - TEOX filling step
 - CMP planarization
- Deep (200 keV) + shallow (55 keV) B I/I
 - 850C, 10 min anneal
- Junction formation
 - As, 70 keV, $4 \times 10^{15} \text{ cm}^{-2}$ + 10 s 1100C \downarrow 0.1 μm
- Co/Ti silicide + TEOS IMD + Al-Si-Cu

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EXPERIMENTAL

Shallow Trench Isolation

STI
SiO₂
n⁺
p-well
Al/Si
p-Sub

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EXPERIMENTAL

shallow contact
deep contact
poly Si
spacer
SiON
active area
PSG
Co silicide
Acc.V 1.20 kV Spot Magn 50000x Det TLD WD 2.5 500 nm
1.20 kV 2.0 50000x TLD 2.5 two K180019 X3 east CONTACT

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EXPERIMENTAL

- **Proton irradiation**
 - 8 MeV: Demokritos/Greece
 - 60 MeV: Cyclone/Belgium
 - 20 MeV: Takasaki JAERI/Japan
- **Electron irradiation**
 - 2 MeV: Takasaki JAERI/Japan
- **Neutron irradiation**
 - 1 MeV: Rikkyo University/Japan
- **TO holders for electrons and neutron**
- **No bias during irradiation**
- **I-V and C-V measurements**
 - Leakage current component: geometrical/physical
- **DLTS & TEM**
- **Damage coefficients & NIEL**

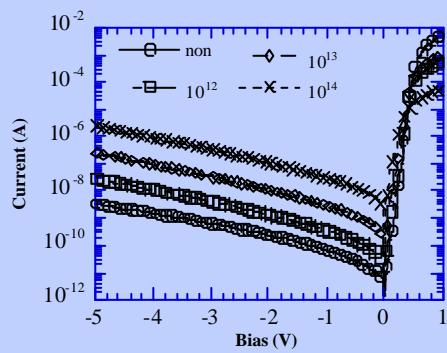
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Radiation of STI Diodes

I-V characteristic of 20 MeV proton irradiated SQ1 STI diodes in function of the fluence F . Curve non corresponds to a non exposed sample.



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RESULTS AND DISCUSSION

I/V characteristics before and after 1 MeV neutrons

The graph plots Current (A) on a logarithmic y-axis (from 10⁻¹¹ to 10⁻³) against Voltage (V) on the x-axis (from -1.0 to 1.0). It shows four curves: a solid line for 'Before' exposure and three dashed lines for '1-MeV Neutrons STI n-p diodes' at fluences of $1 \times 10^{12} \text{ n/cm}^2$ and $1 \times 10^{13} \text{ n/cm}^2$. The 'Before' curve shows a sharp increase in current starting around 0.5 V. The higher fluence curves show a significant decrease in reverse current compared to the 'Before' curve.

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RESULTS & DISCUSSION

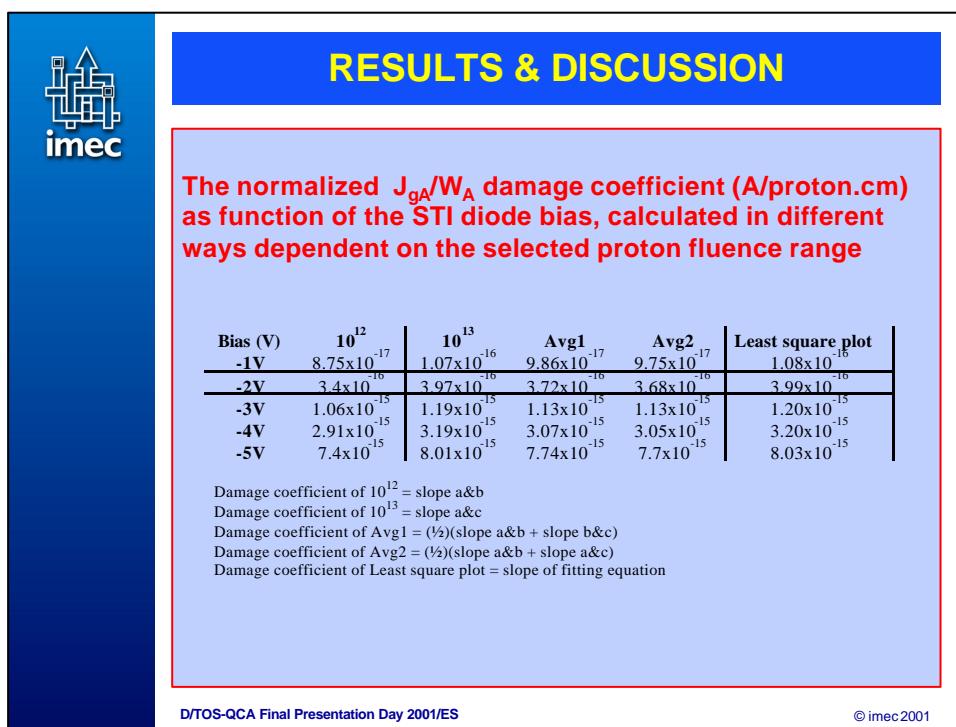
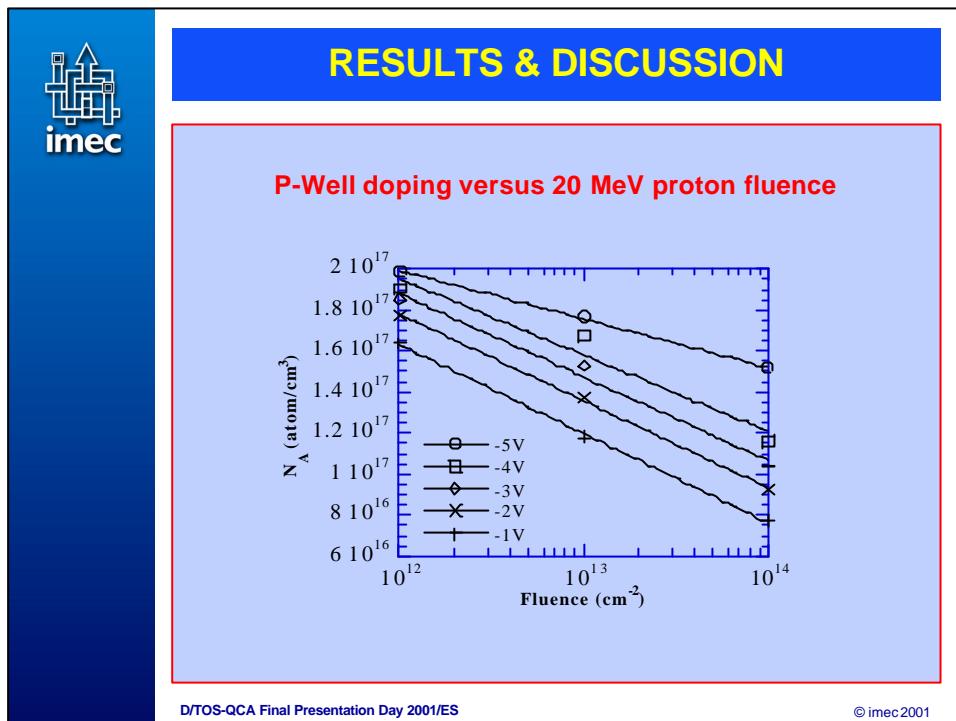
Generation current density vs 20 MeV proton fluence

The graph plots Generation current density J_{gA} (A/cm²) on the y-axis (from 0 to 2.5 $\times 10^{-5}$) against Fluence ($\times 10^{12} \text{ cm}^{-2}$) on the x-axis (from 0 to 120). Five curves are shown for different reverse voltages: -5V (open circle), -4V (open square), -3V (diamond), -2V (cross), and -1V (plus sign). The current density increases with both fluence and reverse voltage.

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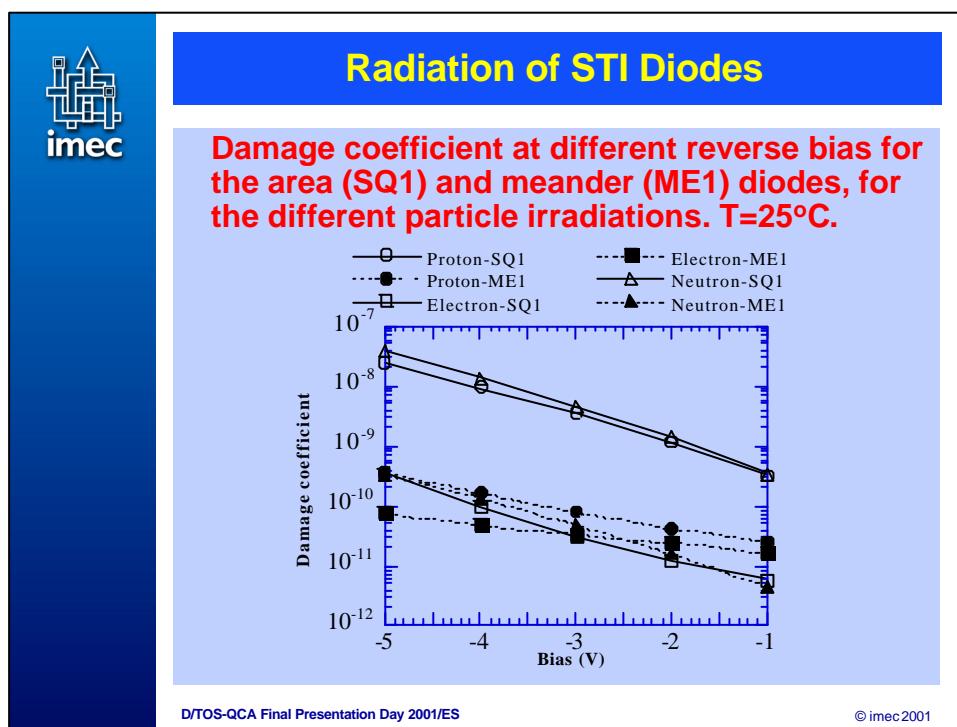
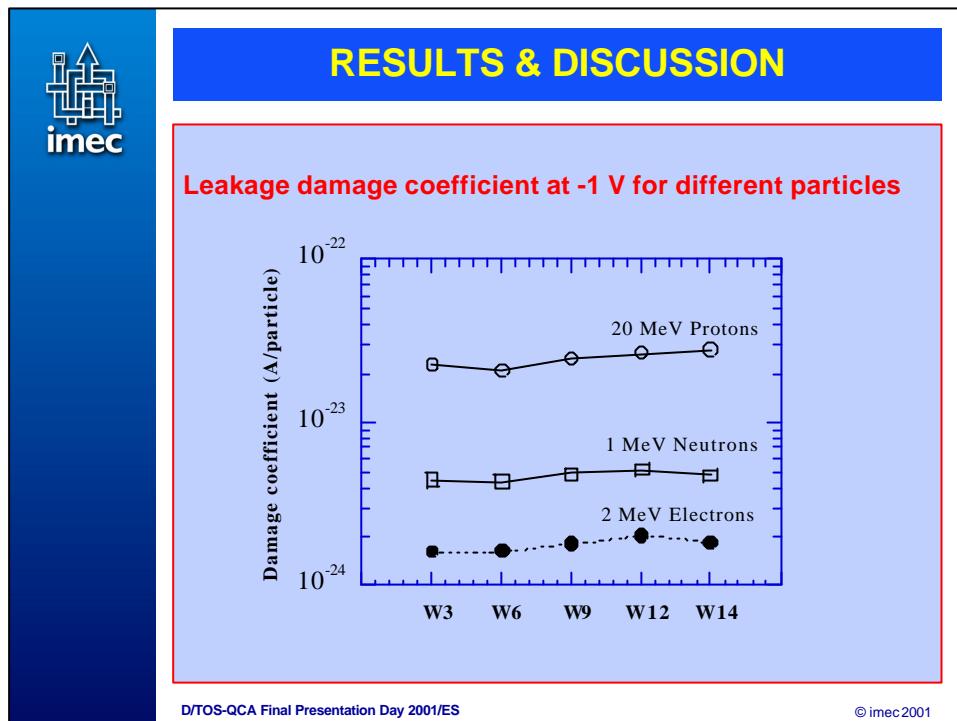
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CONCLUSIONS STI DIODES

- Leakage current increases with fluence
- No direct correlation with NIEL
ionization effects important
- Boron de-activation important for high
fluences
- Normalisation of the damage coefficient to
depletion width is not sufficient
electrical field effects

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CONCLUSIONS STI DIODES

- Highest damage coefficients are for protons, then neutrons and finally electrons
- The influence of the processing conditions are not very pronounced
further investigations needed

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Gate Dielectrics

- **Thin SiO₂ dielectrics have drawbacks**
 - Reproducibility and uniformity
 - Lower resistance to boron in-diffusion from the poly Si
 - Reliability limitations, especially at higher temperature
 - Reduced hot carrier immunity
 - Direct tunneling: exponential increase tunnel current
 - Quantum mechanical effects
- **High k-dielectrics are the solution**
 - Nitrided oxides (NO) or reoxidized nitrided oxides (RNO)
 - N in the oxide: barrier against B diffusion
 - mechanical stress
 - increase dielectric constant
 - More exotic materials are studied

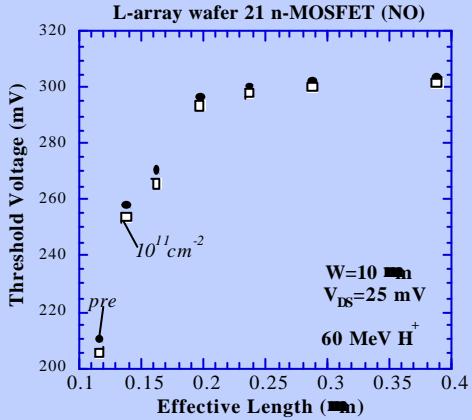
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Gate Dielectrics

NMOSFETs Threshold Voltage before and after 60 MeV Proton Irradiation vs Gate Length (3.5 nm NO)

L-array wafer 21 n-MOSFET (NO)



The graph plots Threshold Voltage (mV) on the y-axis (ranging from 200 to 320) against Effective Length (μm) on the x-axis (ranging from 0.1 to 0.4). Data points are shown for two conditions: 'pre' (before irradiation) and 'post' (after 60 MeV H⁺ irradiation). The 'pre' data points are open squares, and the 'post' data points are solid circles. The threshold voltage increases with effective length, reaching approximately 300 mV at 0.4 μm . The 'post' data points are consistently higher than the 'pre' points, indicating an increase in threshold voltage due to proton irradiation.

Effective Length (μm)	Threshold Voltage (mV) - pre	Threshold Voltage (mV) - post
0.12	205	215
0.15	250	265
0.20	295	305
0.25	300	308
0.30	305	312
0.35	310	315

Threshold Voltage (mV)

Effective Length (μm)

$10^{11} cm^{-2}$

$W=10 \mu m$

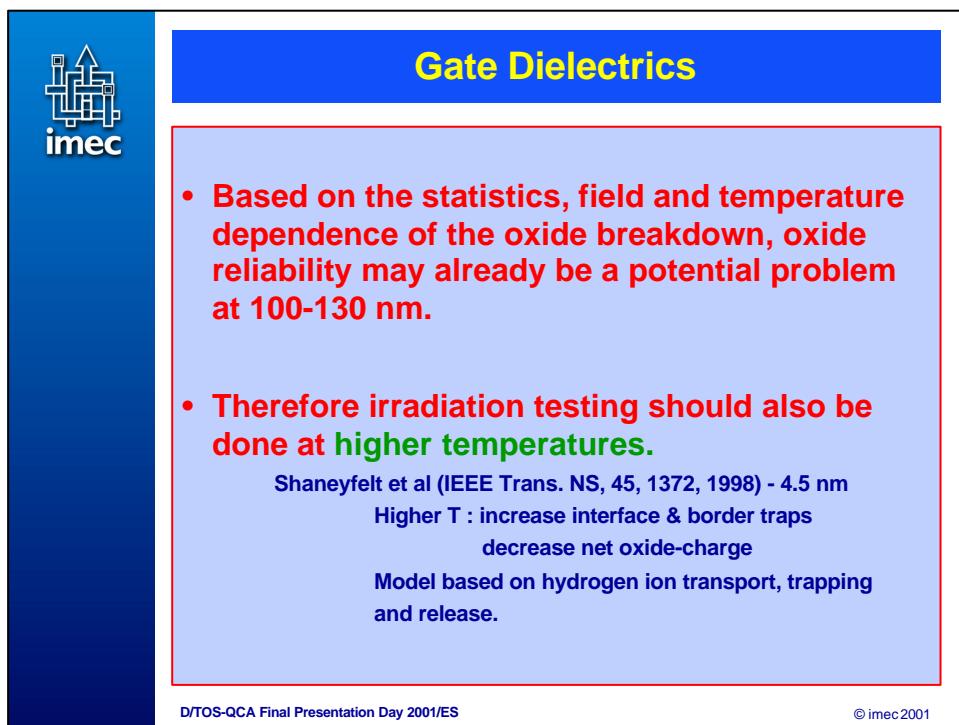
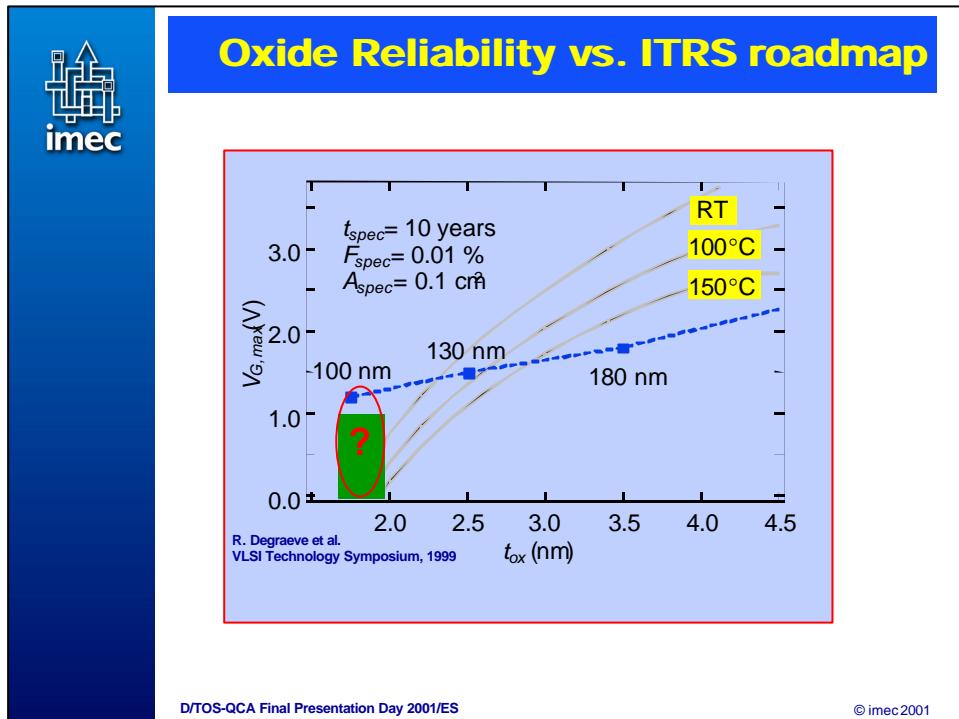
$V_{DS}=25 mV$

$60 \text{ MeV } H^+$

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Conclusions

- Deep submicron CMOS technologies for COTS components seems to be feasible
- Radiation testing of advanced process modules is a necessity
No good simulation models for these modules available
- Below 100 nm new or alternative radiation phenomena may be observed
- Technologies such as SiGe, BiCMOS and SOI are also gaining in importance.

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ACKNOWLEDGMENTS

The CMOS group at IMEC for supplying the 0.18 μm CMOS devices and stimulating discussions on process technology.

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