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MEMO

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To	PCB-SMT WG, PCB manufacturers, ESA projects	**Copy**	

Subject: High resistance electrical test for PCBs

1 SCOPE

The scope of the present memo is to define an improved electrical test method on PCBs to mitigate the risk of latent short circuits caused by imperfections in the dielectric material.

The test method and its scope has been agreed between members of the PCB/SMT WG, including Systronic, Printca, TESAT, Invotec, Astrium, TAS, RUAG, CNES and ESA.

The high resistance test is recommended to be performed on PCBs with a voltage ≥ 30 V. In case this test cannot be performed due to lack of test capability, an intermediate alternative test method may be acceptable provided that a planning is made for the implementation of the new high resistance test. In case the test method cannot be performed for other unforeseen reasons, it is recommended to submit any deviations of the test method for review to the final customer and qualification authority.

2 CLEANLINESS

PCBs have failed due to latent short circuits in various projects. The root cause for these failures has not been conclusively identified. However, it has been widely acknowledged that random contamination inside the dielectrical PCB material is of high concern. Contamination can comprise of fibers in laminate or on prepreg layers and may originate from the PCB manufacturing processes or from the base material supply chain. The presence of fiber contamination is the suspected root cause for latent short circuits in PCBs. The importance of cleanliness of base materials has been addressed to the PCB manufacturers [QT/2013/730/SH] and to the base material supply chain.

3 ELECTRICAL TEST REQUIREMENTS

3.1 Previous flying probe net list testing

Typical electrical testing applied on PCBs by a flying probe equipment, is specified in IPC-9252 and is based on an insulation threshold of 10 MΩ, corresponding to level C for IPC class 3. The objective of this test method is to verify electrical design, i.e. the absence of unintended connections in the circuit. For IPC class 3/A this test method is amended in IPC-6012 to 100 MΩ under 250 V bias.

3.2 New electrical test rationale

The purpose of the new high resistance electrical test method is to determine the quality of the insulation and possible imperfections in the dielectric material. The rationale is that contamination between nets can provide a high-Ohmic path that can be detected under high voltage bias and therefore fails this test. On PCBs that failed the high insulation requirement it has been demonstrated by DPA that the high-Ohmic path was caused by contamination in the dielectric material.

ECSS-Q-ST-70-10C requires typical insulation resistances of >1 GΩ (and orders of magnitude higher) for interlayer, intralayer and via-to-plane on dedicated test patterns. The requirement for high insulation is further substantiated by the typical volume resistivity of dielectric materials in the order of 10^8 MΩ-cm, determined at humid conditions of 90% RH in accordance with IPC-TM-650 2.5.17.1.

It is not the purpose of the high resistance test method to stress the dielectric material by screening for the operational voltage with a specified margin. For operational voltages higher than the test voltage (of 250V), a specific test may be needed such as a dielectric withstanding voltage test. This is not within the scope of the present memo. The high test voltage of 250 V is applied because it is necessary to generate a leakage current that can be detected by the test equipment and that corresponds to a high insulation threshold of 1 GΩ.

Application of the test voltage of 250V on the smallest insulation distance of 70 µm in Z-direction required in ECSS-Q-ST-70-10C results in a worst-case electrical field of 3.6 kV/mm. This is acceptable for the purpose of this high resistance test, because of the heritage with this test voltage on PCBs, the electrical strength specified in datasheets in the order of >30 kV/mm and the short duration of the sustain time.

Precautions (such as dehumidification of air) may be necessary to prevent discharge due to ionisation of air, which has a breakdown strength of 1.5-3.0 kV/mm depending on humidity. This is important for surface conductors spaced approximately 170 µm or closer.

The high resistance test is made applicable for PCBs with operational voltage ≥ 30 V. For lower voltage a similar test method is deemed necessary but more complex to define due to the possibility of HDI layers and fine pitch circuit. Lower voltage PCBs are therefore not within the scope of this memo.

3.3 **High resistance test method**

PCBs procured in accordance with ECSS-Q-ST-70-11C are recommended to be submitted to the electrical test method specified below. Deviations to these requirements due to specific properties of material, design, operational voltage or available test equipment, are recommended to be submitted for review to the final customer and qualification authority.

title	high resistance test
test vehicle	PCBs with worst-case peak operational voltage of ≥ 30 V
test voltage	≥ 250 V
insulation threshold	≥ 1 GΩ
sustain time	≥ 5 ms Lack of voltage stability within this time is recorded as test failure.
voltage monitoring	During the ramp up from 0 to 250 V, the test voltage shall be monitored and a significant drop of the voltage (typically 5%) shall be recorder as a failure of the test.
horizontal adjacency distance	≥ 1,27 mm (in-plane). See figure 1.
vertical adjacency distance	≥ 1,27 mm (in-plane) on 1 layer above and below the specified net. See figure 1.
resistive isolation testing	Direct resistive isolation testing shall be performed. Indirect isolation testing by signature comparison shall not be performed.
retest	• It is recommended to dehumidify the PCB by baking prior to testing. In case the test fails because dehumidification is not deemed to be sufficient, one further bake and retest may be performed. High temperature during baking may affect the quality of the surface finish, which needs to be verified. • Retesting may be performed in case high capacitance is caused by large plane layers requiring adjustment of test parameters.

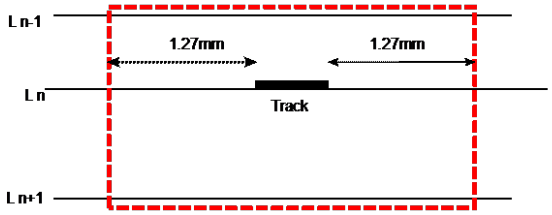

Figure 1: Nets within the volume defined by horizontal and vertical adjacency distance are included in the high resistance test.