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15 November 2008

Space product assurance

Qualification of printed circuit boards

ECSS Secretariat
ESA-ESTEC
Requirements & Standards Division
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Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering and product assurance in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards. Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

This Standard has been prepared by the ECSS Executive Secretariat, endorsed by the Document and Discipline Focal Points, and approved by the ECSS Technical Authority.

Disclaimer

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1
Scope

This Standard defines the requirements for evaluation, qualification and maintenance of qualification of PCB manufacturers for different types of PCBs.

This Standard is applicable to the following type of PCBs:

- Rigid PCBs (single-sided, double-sided, multilayer, sequential-laminated multilayer, metal core)
- Flexible PCB (single-sided and double-sided)
- Rigid-flex PCBs (multilayer and sequential-laminated multilayer)
- High frequency PCBs
- Special PCBs.

PCBs are used for the mounting of components in order to produce PCB assemblies performing complex electrical functions. The PCBs are subjected to thermal and mechanical shocks during their assembly such as mounting of components by soldering, rework and repair under normal terrestrial conditions, and in addition the complex PCB assembly are subjected to the environment imposed by launch and space flights.

This standard may be tailored for the specific characteristics and constraints of a space project in conformance with ECSS-S-ST-00.

2
Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revision of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the more recent editions of the normative documents indicated below. For undated references, the latest edition of the publication referred to applies.

ECSS-S-ST-00-01	ECSS system — Glossary of terms
ECSS-Q-ST-10-09	Space product assurance — Nonconformance control system
ECSS-Q-ST-20	Space product assurance — Quality assurance
ECSS-Q-ST-70	Space product assurance — Material, mechanical parts and processes
ECSS-Q-ST-70-02	Space product assurance — Thermal vacuum outgassing test for the screening of space materials
ECSS-Q-ST-70-08	Space product assurance — Manual soldering of high-reliability electrical connections
ECSS-Q-ST-70-11	Space product assurance — Procurement of printed circuit boards
ECSS-Q-ST-70-21	Space product assurance — Flammability testing for the screening of space materials
ECSS-Q-ST-70-22	Space product assurance — Control of limited shelf-life materials
ECSS-Q-ST-70-29	Space product assurance — Determination of offgassing products from materials and assembled articles to be used in a manned space vehicle crew compartment
IEC 60068-2-3 (1969-01)	Environmental testing. Part 2: Tests. Test Ca: Damp heat, steady state
IEC 60068-2-14-am 1 (1986-01)	Environmental testing. Part 2: Tests. Test N: Change of temperature
IEC 60068-2-20-am 2 (1987-01)	Environmental testing. Part 2: Tests. Test T: Soldering

IEC 60249-1-am 4 (1993-05)	Base materials for printed circuits. Part 1: Test methods
IEC 60326-2-am 1 (1992-06)	Printed boards. Part 2: Test methods
IEC 60326-5-am 1 (1989-10)	Printed boards. Part 5: Specification for single and double sided printed boards with plated-through holes
IEC 60326-8 (1981-01)	Printed boards. Part 8: Specification for single and double sided flexible printed boards with through connections
IEC 60326-11 (1991-03)	Printed boards. Part 11: Specification for flex-rigid multilayer printed boards with through connections
IEC 62326-4 (1996-12)	Printed boards. Part 4: Rigid multilayer printed boards with interlayer connections - Sectional specification
IPC-4101	Specification for base materials for rigid and multilayer printed boards
MIL-P-50884C	Printed wiring, flexible and rigid-flex

3
Terms, definitions and abbreviated terms

3.1 Terms from other standards

For the purpose of this Standard, the terms and definitions from ECSS-S-ST-00-01 apply.

3.2 Terms specific to the present standard

3.2.1 associated test coupon

small piece of PCB designated to have a limited specific set of tests performed

NOTE The associated test coupon is manufactured as part of a PCB and at the final manufacturing stage it is separated from it. The associated test coupon is thus associated with the PCB, with which it was simultaneously manufactured.

3.2.2 blister

delamination in the form of a localized swelling and separation between any of the layers of a lamination base material, or between base material and conductive foil or protective coating

[IEC 60194 (1999-04)]

3.2.3 cover layer (flexible circuit)

layer of insulating material that is applied covering totally or partially over a conductive pattern on the outer surfaces of a PCB

[IEC 60194 (1999-04)]

3.2.4 crazing

internal condition that occurs in reinforced base material whereby glass fibres are separated from the resin at the weave intersections

NOTE 1 This condition manifests itself in the form of connected white spots or crosses that are below the surface of the base material. It is usually related to mechanically induced stress.

NOTE 2 See also “measling”.

[IEC 60194 (1999-04)]

3.2.5 delamination

separation between plies within a base material, between base material and a conductive foil, or any other planar separation with a PCB

NOTE See also "blister".

[IEC 60194 (1999-04)]

3.2.6 dewetting

condition that results when molten solder coats a surface and then recedes to leave irregularly-shaped mounds of solder that are separated by areas that are covered with a thin film of solder and with the basis metal not exposed

[IEC 60194 (1999-04)]

3.2.7 flexible PCB

PCB either single, double sided or multilayer consisting of a printed circuit or printed wiring using flexible base materials only

[IEC 60194 (1999-04)]

3.2.8 haloing

mechanically-induced fracturing or delamination, on or below the surface of a base material, that is usually exhibited by a light area around holes or other machined features

[IEC 60194 (1999-04)]

3.2.9 high frequency PCB

PCB used for high frequency applications, that has specific requirements to the dielectric properties of the base laminates as well as special dimensional requirements to the lay-out for electrical purposes

3.2.10 inclusions

foreign particles, metallic or non-metallic, that may be entrapped in an insulating material, conductive layer, plating, base material or solder connection

[IEC 60194 (1999-04)]

3.2.11 key personnel

personnel with specialist knowledge responsible for defined production or product assurance areas

3.2.12 measling

condition that occurs in laminated base material in which internal glass fibres are separated from the resin at the weave intersection

NOTE 1 This condition manifests itself in the form of discrete white spots or "crosses" that are below the surface of the base material. It is usually related to thermally-induced stress.

NOTE 2 See also "crazing".

[IEC 60194 (1999-04)]

3.2.13 metal core PCB

PCB using a metal core base material

[IEC 60194 (1999-04)]

3.2.14 multilayer PCB

PCB that consist of rigid or flexible insulation materials and three or more alternate printed wiring and/or printed circuit layers that have been bonded together and electrically interconnected

[IEC 60194 (1999-04)]

3.2.15 prepreg

sheet of material that has been impregnated with a resin and cured to an intermediate stage

NOTE B-staged resin.

[IEC 60194 (1999-04)]

3.2.16 printed circuit board (PCB)

printed board that provides both point-to-point connections and printed components in a predetermined arrangement on a common base

NOTE This includes single-sided, double sided and multilayer PCBs with rigid, flexible, and rigid-flex base materials.

[IEC 60194 (1999-04)]

3.2.17 rigid double-sided PCB

double-sided PCB, either printed circuit or printed wiring, using rigid base materials only

[IEC 60194 (1999-04)]

3.2.18 rigid-flex PCB

PCB with both rigid and flexible base materials

[IEC 60194 (1999-04)]

3.2.19 rigid-flex double-sided PCB

double-sided PCB, either printed circuit or printed wiring, using combinations of rigid and flexible base materials

[IEC 60194 (1999-04)]

3.2.20 rigid-flex multilayer PCB

multilayer PCB, either printed circuit or printed wiring, using combinations of rigid multilayer and flexible single and double-sided base materials

3.2.21 rigid PCB

PCB using rigid base materials only

[IEC 60194 (1999-04)]

3.2.22 rigid single-sided PCB

single-sided PCB, either printed circuit or printed wiring, using rigid base materials only

[IEC 60194 (1999-04)]

3.2.23 rigid multilayer PCB

multilayer PCB, either printed circuit or printed wiring, using rigid base materials only

[IEC 60194 (1999-04)]

3.2.24 scratch

narrow furrow or grove in a surface

NOTE It is usually shallow and caused by the marking or rasping of the surface with a pointed or sharp object.

[IEC 60194 (1999-04)]

3.2.25 sequentially laminated multilayer PCB

multilayer PCB that is formed by laminating together through hole plated double-sided or multilayer PCBs

NOTE Thus, some of its conductive layers are interconnected with blind or buried vias.

[IEC 60194 (1999-04)]

3.2.26 test pattern

part of the PCB that refers to the copper pattern on and within the PCB substrate for a specific test

3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
CAD	computer aided design
CAM	computer aided manufacturing
M	major nonconformance
m	minor nonconformance
n.a.	not applicable
NRB	nonconformance review board
PCB	printed circuit board
PID	process identification document
PTH	plated-through hole

PTFE	polytetrafluoroethylene
r.m.s.	root-mean-square
TBD	to be defined

4
Principles

4.1 General

This Standard details the steps to obtain from the PCB manufacturer the qualification for supplying PCBs of an identified technology.

These steps are:

a. Evaluation (see clause 5);

b. Qualification (see clause 6):

— Test and inspections (see clause 7),

— Qualification approval (see clause 6.6);

c. Maintenance of qualification (see clause 6.7).

4.2 Roles

For the need of this Standard the roles "PCB manufacturer", "supplier", "customer" and "qualification authority" have been explicitly introduced to allow proper allocation of requirements:

a. The "PCB manufacturer" is the entity that manufactures the PCB.

b. The "supplier" is the entity that uses the PCB for an instrument, for instance a subcontractor that delivers an electronics box. The supplier procures the PCB from the PCB manufacturer.

c. The "customer" is the entity that uses the supplier's product for a project, for instance a prime contractor that integrates an electronics box into a spacecraft payload. The role of supplier can coincide with the one of customer. The term customer does not refer to being the customer of the PCB manufacturer but refers to being the (prime) contractor of a space organisation initiating a space project.

d. The "qualification authority" is the entity that reviews and accepts the qualification programme, evaluates the test results and grants the final approval. The role of customer can coincide with the one of qualification authority.

4.3 Specification of test requirements

Clause 7 describes the tests within the qualification programme in which the following three levels of requirement specifications are used:

a. The requirement specifications that are generic for all types of PCBs are listed in clause 7.

b. The requirement specifications that are specific to a particular type of PCB are listed in clause 9 and are referred to with the term "requirement" in clause 7.

c. The requirement specifications that are determined by the supplier are referred to with the term "supplier's specification" in clause 7.

5 Evaluation

5.1 General

a. The PCB manufacturer who applies for the qualification of his PCB manufacturing line shall:

1. request for an evaluation in conformance with clause 5.2;
2. supply evaluation PCBs in conformance with clause 5.3;
3. have a manufacturing line audit performed in conformance with clause 5.4.

NOTE If the result is satisfactory, the qualification authority can authorize the go-ahead of the qualification programme for each of the technologies that have been accepted.

b. The PCB manufacturer and the qualification authority shall agree on the evaluation tests to be performed.

NOTE The evaluation tests can be an appropriate subset of the tests performed within the qualification programme.

5.2 Request for evaluation

a. The PCB manufacturer's request for evaluation shall contain:

1. a description of the technology for which the PCB manufacturer wishes to be evaluated;
2. a description of the manufacturing line;
3. past experience.

b. Applications shall be signed by the person responsible for production and product assurance.

c. Applications shall be addressed to the qualification authority.

5.3 Evaluation PCBs

a. The PCB manufacturer shall produce three evaluation PCBs of each type with the materials, processes and equipment that are intended for use in subsequent production.

b. The evaluation PCBs shall be representative in terms of technology for which the PCB manufacturer applies for qualification.

NOTE The term technology refers, among others, to:

- Dimensions of the boards, vias, pads and tracks
- Number of layers
- Pattern design.

c. The evaluation PCBs shall represent the highest technological capability for which the PCB manufacturer applies for qualification.

d. The PCB manufacturer shall perform the evaluation test and document it in conformance with Annex A.

NOTE The evaluation PCBs can be inspected at an independent certified test house.

e. The evaluation PCBs shall be provided with associated test coupons.

5.4 Line audit

a. Provided that the evaluation PCBs are accepted, the qualification authority shall audit the manufacturing line when PCB production is in progress.

b. Before or during the audit, the PCB manufacturer shall make the following documents available to the customer:

1. Company organigram related to PCB production and control, including names and functions of all key personnel involved.
2. Identification of the parameters of the technologies that they wish to qualify.

NOTE See note in requirement 5.3b.

3. List of materials and equipment (including types and names of companies) used for production of PCBs.
4. List of process and control specifications with number, issue number, and date of issue.
5. Production flow-chart, including quality-assurance inspection point and relevant process specification.
6. Outline of test capabilities.

NOTE 1 Examples of test capabilities are metallographic examination, chemical analysis, failure analysis, mechanical and electrical test including functional testing of PCBs.

NOTE 2 These six documents can be gathered in a preliminary process identification document (PID).

6 Qualification

6.1 General

a. A qualification programme shall be initiated in the following cases:

1. Initial qualification.
2. When previous qualification is more than two years ago and maintenance of qualification was not assured.
3. Interruption of the manufacturing of the type of PCBs for more than two years.
4. New technology.
5. Change in the manufacturing line.

NOTE For example, any changes in material, chemical products, mechanical processing parameters, equipments.

6. The manufacturing line was moved to another location.
7. Changes in key personnel.

6.2 Qualification programme definition and approval

a. After successful evaluation, the PCB manufacturer shall submit a qualification programme to the qualification authority for approval, after which the programme shall be initiated.

b. The qualification programme shall identify:

1. the key personnel involved;
2. the test houses;
3. the test procedure and test sequence;
4. the proposed schedule of testing.

c. Each test house shall have the approval of the qualification authority prior to commencement of the programme.

d. The PCB manufacturer shall agree with the qualification authority on the monitoring during the qualification programme.

6.3 Nonconformance criteria

a. The nonconformances shall be dispositioned in conformance with ECSS-Q-ST-10-09.

b. Major nonconformances (M) shall be dispositioned at a nonconformance review board (NRB) established by the qualification authority and the PCB manufacturer.

NOTE This is because any major nonconformance (M) can result in the failure of qualification.

c. Minor nonconformances (m) shall be:

1. processed through an internal NRB of the PCB manufacturer to determine the causes and consequences;
2. reported in the qualification test report in conformance with Annex B;
3. assessed by the qualification authority;

d. Nonconformance criteria ranked "m/M" shall be further classified by the PCB manufacturer, the supplier and the qualification authority.

6.4 Qualification programme implementation

a. The qualification programme shall be performed by the PCB manufacturer or one or more independent test houses.

b. The qualification programme shall be performed on six qualification PCBs.

c. One additional qualification PCB shall be made for reference.

d. The qualification programme shall be performed in conformance with the test sequence specified in Figure 6-1 and the test specification in Table 6-1 and explained in detailed in clause 7.

e. A qualification test report shall be prepared in conformance with Annex B and submitted to the qualification authority for review and approval together with all prepared microsections.

NOTE The qualification authority can request the delivery of the inspected qualification PCBs.

f. If the PCBs are used for manned space programmes the customer shall assure the PCB base material is tested for the following items:

1. Flammability in conformance with ECSS-Q-ST-70-21.
2. Offgassing (toxicity) and odour according to ECSS-Q-ST-70-29.

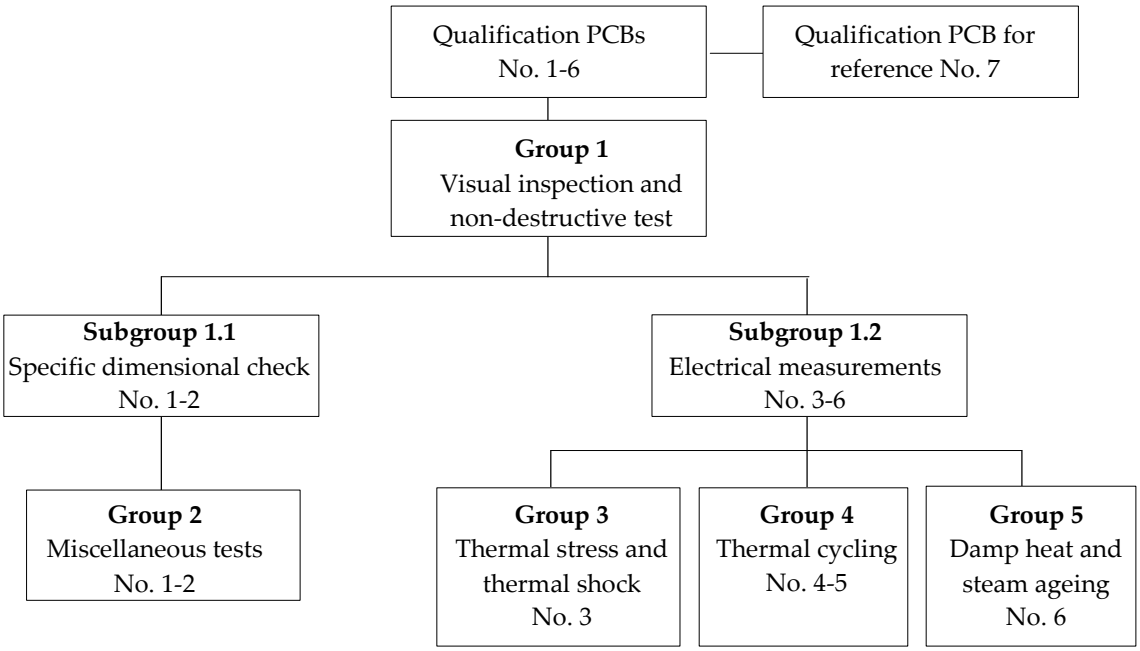


Figure 6-1: Test sequence

Table 6-1: Test specification

(Part 1 of 2)

Group	Tests	Clause	PCB no. Test pattern no.
Group 1	**Visual inspection and non-destructive tests**: - Verification of marking - Visual aspects - External dimensions - Warp - Twist	7.2 7.2.2 7.2.3 7.2.4 7.2.5 7.2.6	PCBs 1-6
Subgroup 1.1	Specific dimensional check	7.2.7	PCBs 1-2
Subgroup 1.2	Electrical measurements: - Intralayer[a] insulation resistance - Interlayer[b] insulation resistance - Dielectric withstanding voltage: • intralayer • interlayer - Continuity - Interconnection resistance - Impedance test - Dielectric constant and loss tangent for high frequency materials	7.2.8 7.2.8.2 7.2.8.3 7.2.8.4 7.2.8.5 7.2.8.6 7.2.8.7 7.2.8.8	PCBs 3-6 Test pattern A Test pattern H Test pattern A Test pattern H Test pattern D Test pattern E Test pattern Y Test pattern W
Group 2	**Miscellaneous tests**	7.3	PCBs 1-2
Subgroup 2.1	Solderability test: - Wettability - Microsectioning (option)	7.3.2 7.3.2 7.3.4.3	 Test pattern J Test pattern J
Subgroup 2.2	Mechanical tests: - Peel strength - Pull-off strength - Flexural fatigue (only for double sided flexible PCB) - Bending test (only for rigid-flex)	7.3.3 7.3.3.1 7.3.3.2 7.3.3.3 7.3.3.4	 Test pattern B Test pattern B Test pattern X
Subgroup 2.3	Coating tests: - Coating adhesion of non-fused SnPb finishes - Analysis of SnPb coating - Microsectioning	7.3.4 7.3.4.1 7.3.4.2 7.3.4.3	 Test pattern G Test pattern G Test pattern F
Subgroup 2.4	Electrical tests: - Current overload: • Short-time overload • Long-time overload - Internal short circuit	7.3.5 7.3.5.1 7.3.5.1.2 7.3.5.1.3 7.3.5.2	 Test pattern E Test pattern C
Subgroup 2.5	Physical tests: - Water absorption - Outgassing	7.3.6 7.3.6.1 7.3.6.2	Test pattern K

Table 6-1: Test specification

(Part 2 of 2)

Group 3	**Thermal stress**	7.4	PCB 3
	Solder bath float and vapour phase reflow simulation	7.4.2	PCB (without test pattern F) PCB
	- Substrate aspect test	7.2.3	Test pattern B
	- Peel strength	7.3.3.1	Test pattern D
	- Continuity	7.2.8.5	Test pattern E
	- Interconnection resistance	7.2.8.6	Test pattern J
	- Microsectioning	7.3.4.3	Test pattern F
	Rework simulation (thermal shock, hand soldering)	7.4.3	Test pattern F
	- Microsectioning	7.3.4.3	
Group 4	**Thermal cycling**	7.5	PCBs 4-5
	- Substrate aspect test	7.2.3	PCBs
	- Peel strength	7.3.3.1	Test pattern B
	- Continuity	7.2.8.5	Test pattern D
	- Interconnection resistance	7.2.8.6	Test pattern E
	- Intralayer[a] insulation resistance	7.2.8.2	Test pattern A
	- Interlayer[b] insulation resistance	7.2.8.3	Test pattern H
	- Dielectric withstanding voltage:	7.2.8.4	
	• intralayer		Test pattern A
	• interlayer		Test pattern H
	- Microsectioning	7.3.4.3	Test pattern F
Group 5	**Damp heat — Steam ageing**	7.6	PCB 6
	Damp heat	7.6.2	PCB (without test pattern F)
	- Peel strength	7.3.3.1	Test pattern B
	- Intralayer[a] insulation resistance	7.2.8.2	Test pattern A
	- Interlayer[b] insulation resistance	7.2.8.3	Test pattern H
	- Dielectric withstanding voltage:	7.2.8.4	
	• intralayer		Test pattern A
	• interlayer		Test pattern H
	- Microsectioning (if required)	7.3.4.3	Test pattern F
	Steam ageing	7.6.3	Test pattern F
	- Solderability test:		
	• Wettability	7.3.2	Test pattern F
	- Microsectioning (if required)	7.3.4.3	Test pattern F

a. i.e.: in the same layer.
b. i.e.: between opposite layers.

6.5 Qualification PCBs

6.5.1 General

a. The qualification PCBs shall have test patterns that enable evaluation of the specific characteristics, summarised in Table 6-1 and described in detail in clause 7.

b. The qualification PCB shall represent the highest technological capability for which the PCB manufacturer applies for qualification.

c. The qualification PCB shall consist of a test pattern demonstrating the technological capability (test pattern L) together with the other test patterns.

NOTE The pattern drawing on layer 1 of the individual test patterns given below and shown as an example in Figure 6-2 can be used.

d. The PCB manufacturer and the qualification authority shall agree on the layout of the capability pattern.

NOTE The capability pattern can be an actual PCB circuit to be used in the space project.

e. The test pattern layout and design shall be in conformance with the referenced IEC specification if applicable:

1. Single and double sided PCBs with plated-through holes: IEC 60326-5.
2. Rigid multilayer PCBs with interlayer connections: IEC 62326-4.
3. Single and double sided flexible PCBs with through connections: IEC 60326-8.
4. Flex-rigid multilayer PCBs with through connections: IEC 60326-11.

f. The test pattern layout and design for sequentially laminated multilayer PCBs and special PCBs shall be agreed between PCB manufacturer, supplier and qualification authority.

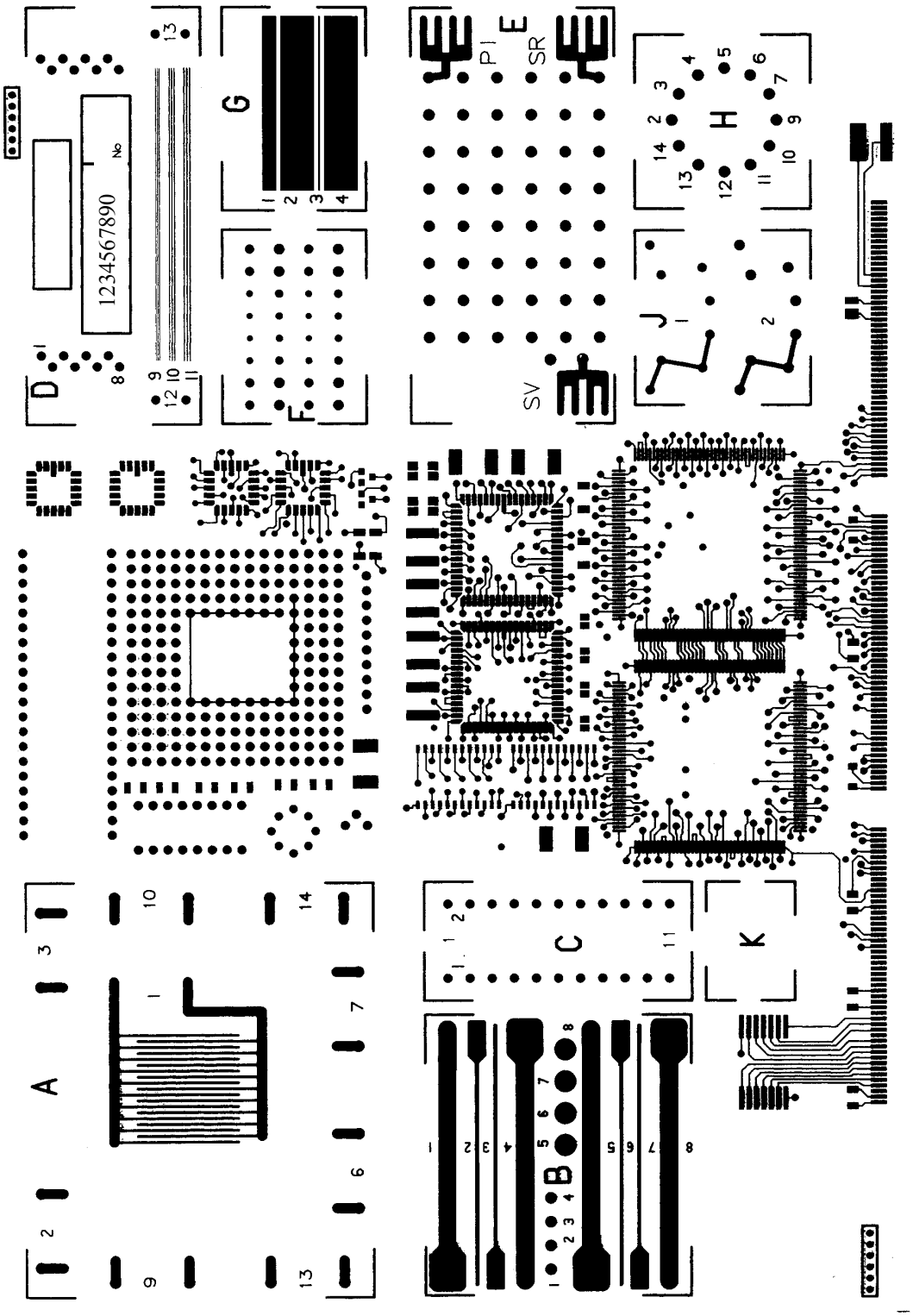


Figure 6-2: Example of a qualification PCB layout with patterns for testing and a pattern for demonstration of the technological capability

6.5.2 Test pattern A: Electrical test

a. The following measurements shall be performed on test pattern A:

1. Intralayer insulation resistance.
2. Dielectric withstanding voltage.

NOTE See example in Figure 6-3.

b. The conductor width and spacing within each layer shall represent the minimum dimensions to be qualified.

NOTE The comb pattern can provide a useful tool for evaluating cleanliness.

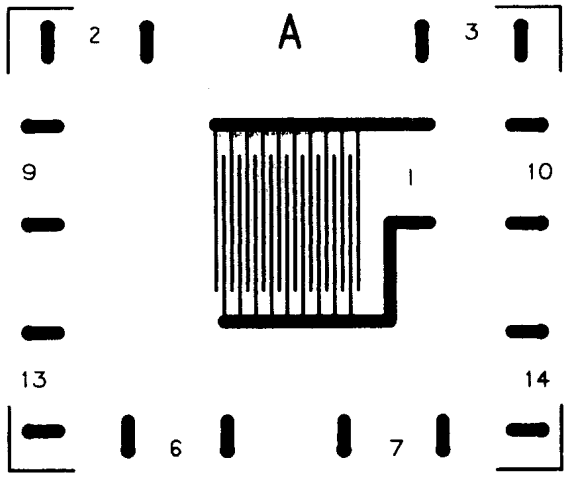


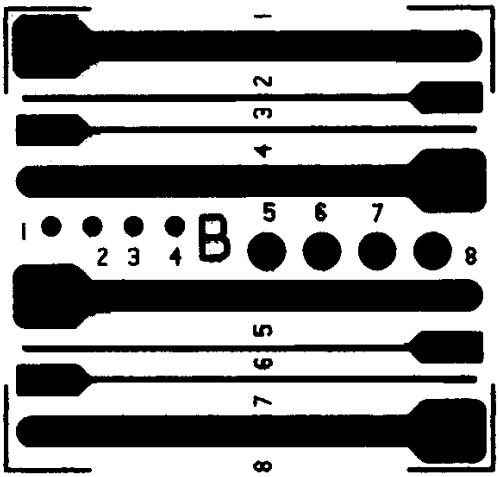
Figure 6-3: Example of test pattern for intralayer insulation resistance and dielectric withstanding voltage testing

6.5.3 Test pattern B: Mechanical test

a. The following measurements shall be performed on test pattern B:

1. Peel strength of copper track on laminate.
2. Pull-off strength of surface mount pads.
3. Surface solderability.

NOTE See example in Figure 6-4.



NOTE This is a surface pattern only and all holes are non-plated-through.

Figure 6-4: Example of test pattern for testing peel strength of conductors and pull-off strength of pads

6.5.4 Test pattern C: Electrical test

a. The internal short circuit shall be measured on test pattern C.

NOTE 1 This consists in verifying the insulation between plated-through holes in daisy chain through all layers and ground plane.

NOTE 2 See example in Figure 6-5.

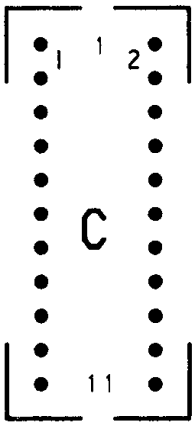


Figure 6-5: Example of test pattern for internal short circuit testing

6.5.5 Test pattern D: Electrical test and visual aspect

a. The following measurements shall be performed on test pattern D:

1. Marking.
2. Etching definition.

3. Continuity between plated-through holes in daisy chain through all layers.

4. Visual aspect.

NOTE See example in Figure 6-6.

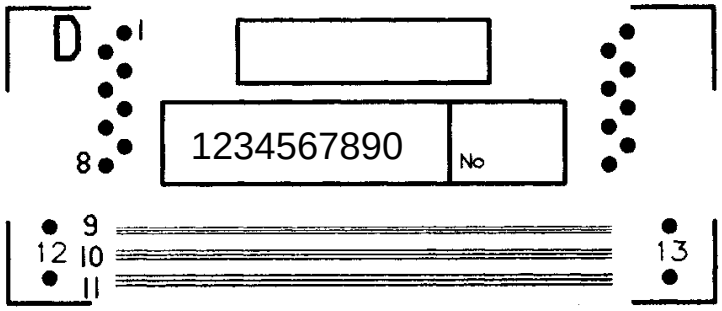


Figure 6-6: Example of test pattern for etching definition evaluation and continuity testing

6.5.6 Test pattern E: Electrical test

a. The following measurements shall be performed on test pattern E:

1. Interconnection resistance between plated-through holes in daisy chain through all layers before and after thermal cycling and thermal stress.

2. Current overload between plated-through holes in daisy chain through all layers for short and long duration.

NOTE See example in Figure 6-7.

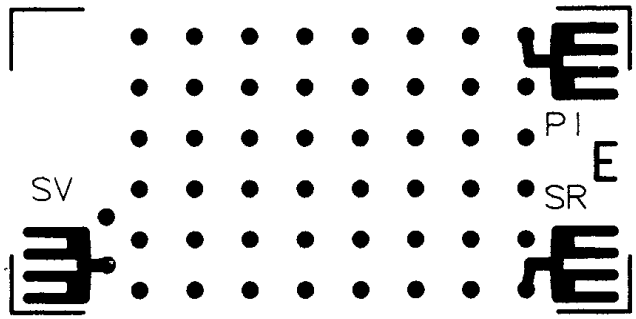


Figure 6-7: Example of test pattern for interconnection resistance and current overload testing

6.5.7 Test pattern F: Metal-plating test

a. The following measurements shall be performed on test pattern F:

1. Microsectioning to evaluate and determinate metal plating thickness.
2. Microsectioning after thermal cycling, thermal stress and damp heat (optional).

NOTE See example in Figure 6-8.

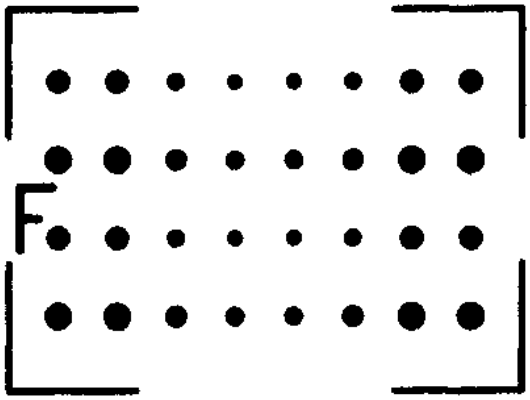


Figure 6-8: Example of test pattern for microsectioning and metal plating evaluation

6.5.8 Test pattern G: Metal-plating/coating test

a. The following measurements shall be performed on test pattern G:

1. Tape test for evaluation of adhesion of plated coating on copper track.
2. Analysis of SnPb composition after reflow.

NOTE See example in Figure 6-9.

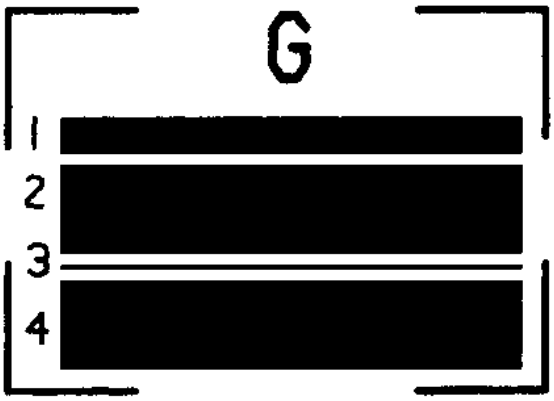


Figure 6-9: Example of test pattern for plating adhesion testing and analysis of SnPb coating composition after reflow

6.5.9 Test pattern H: Electrical test

a. The following measurements shall be performed on test pattern H:

1. Interlayer insulation resistance and dielectric withstanding voltage before and after thermal cycling and, optionally, after damp heat.
2. Interlayer insulation resistance and withstanding voltage measured between plated-through holes and a central ground plane.

NOTE See example in Figure 6-10.

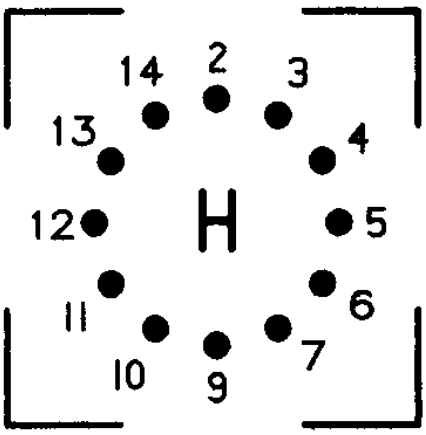


Figure 6-10: Example of test pattern for interlayer insulation resistance and dielectric withstanding voltage testing

6.5.10 Test pattern J: Solderability test

a. The following measurements shall be performed on test pattern J:

1. Solder wettability of pads and plated-through holes.
2. Rework simulation on plated-through holes.

NOTE See example in Figure 6-11.

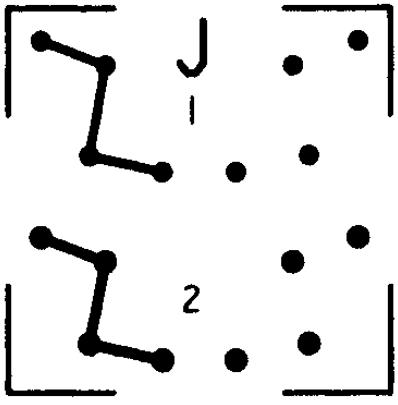


Figure 6-11: Example of test pattern for solder wettability and rework simulation testing

6.5.11 Test pattern K: Physical test

a. The following measurements shall be performed on test pattern K:

1. Water absorption (optional).
2. Outgassing tests on base laminate material according to ECSS-Q-ST-70-02.

NOTE See example in Figure 6-12.

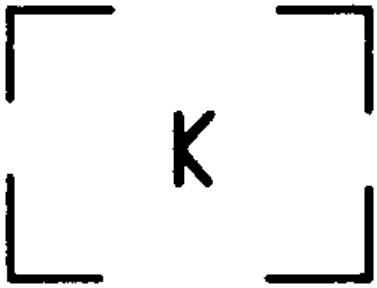


Figure 6-12: Example of test pattern for water absorption and outgassing testing

6.5.12 Test pattern L: Demonstration of technological capability

a. The following measurements shall be performed on test pattern L:

1. Minimum conductor width.
2. Minimum spacing.
3. Minimum hole diameter.
4. Other features that characterise the level of technological capability of the PCB design in terms of dimensional outline, build-up, non-standard use of materials.

NOTE See example in Figure 6-13.

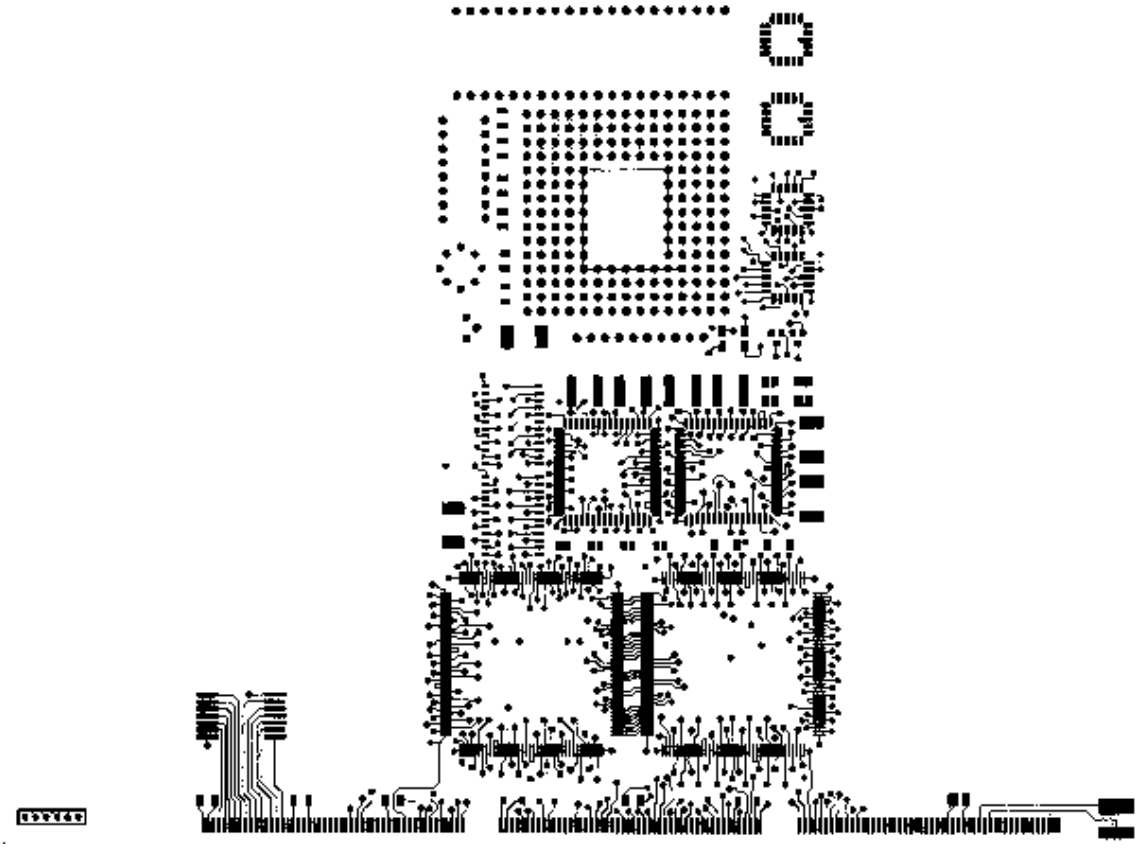


Figure 6-13: Example of test pattern for evaluation of the technological capability

6.5.13 Test pattern M: CAD/CAM criteria (on request by the qualification authority)

a. The CAD/CAM capability of the PCB manufacturer shall be evaluated on test pattern M by visual inspection.

NOTE See example Figure 6-14.

b. For this purpose the layout of the test pattern shall:

1. be divided up into 3 zones with identical surfaces.
2. have various pads in each zone (circular, oblong, square, rectangular).
3. have a thermal shunt for internal layers.

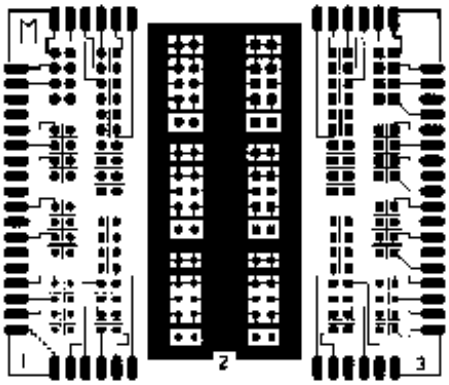


Figure 6-14: Example of test pattern for evaluation of CAD/CAM capability

6.5.14 Test pattern X: Resistance to bending cycles (for flexible parts only)

a. The following measurements shall be performed on test pattern X:

1. Evaluation of continuity of conductors after exposing the pattern to bending cycles.
2. Evaluation of adhesion between conductors and insulating material after exposing the pattern to bending cycles.

NOTE See example in Figure 6-15.

Figure 6-15: Example of test pattern for testing resistance to bending cycles

6.5.15 Test pattern Y: Electrical test (on request by the supplier)

a. An impedance test shall be performed on test pattern Y.

NOTE See example Figure 6-16.

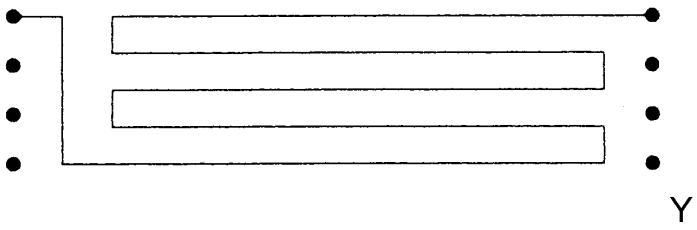


Figure 6-16: Example of test pattern for controlled impedance testing

6.5.16 Test pattern W: Electrical test for high frequency circuits (on request by the supplier)

a. The following measurements shall be performed on test pattern W:

   1. Dielectric constant.

   2. Loss tangent.

b. The resonator for dielectric constant and loss tangent measurements shall be defined between PCB manufacturer and supplier.

   NOTE This depends on the dielectric parameters of the material.

c. If the PCBs are used for manned space programmes the customer shall assure the PCB base material is tested for the following items:

   1. Flammability in conformance with ECSS-Q-ST-70-21.

   2. Offgassing (toxicity) and odour according to ECSS-Q-ST-70-29.

6.6 Qualification approval

a. The qualification authority shall grant qualification approval to the PCB manufacturer based on the examination and acceptance of the qualification programme.

b. The manufacturing process of the PCBs shall be established and documented in a PID in conformance with Annex C.

c. The qualification approval shall be valid for a period of two years.

6.7 Maintenance of qualification

a. During the period in which the qualification approval is valid the PCB manufacturer shall notify the qualification authority in case any problem arises that is related to the manufacturing of PCBs.

b. To maintain qualification status, the PCB manufacturer shall send, two months before the expiry date of the qualification period, the following items to the qualification authority:

   1. A qualification status report in conformance with Annex D.

   2. One recently manufactured high reliability PCB sample for technical assessment.

c. Based upon the information received, the result of the technological examination and an investigation of the experiences regarding delivery times and quality of PCBs supplied for space projects, the qualification authority shall decide upon one of the following:

   1. In case there are no nonconformances, to extend the qualification period by two years and eventually to arrange a control visit to the PCB manufacturer's plant.

2. In case there are nonconformances, the necessary corrective action is negotiated with the PCB manufacturer in order to enable maintenance of qualification status.

   NOTE This can include additional testing to be agreed between PCB manufacturer and qualification authority and submittal of a new PCB sample.

d. The PCB manufacturer shall arrange for an audit by the qualification authority every second year.

e. The qualification shall be withdrawn if the:

   1. submitted PCB specimen for qualification renewal is rejected;
   2. results of an audit at the manufacturing facility are unsatisfactory;
   3. materials or manufacturing processes are modified without prior authorization by the qualification authority;
   4. supplier has met major nonconformances regarding delivery time and manufacturing defects.

7
Tests

7.1 General

a. Unless otherwise specified, all tests shall be carried out under the below specified normal atmospheric conditions in conformance with test 18a of IEC 60326-2-am 1 (1992-06):

   1. Room temperature: (22 ± 3) °C.
   2. Relative humidity: (55 ± 10) %.
   3. Atmospheric pressure.

b. Before testing is started, the PCBs shall be subjected for 48 h to ambient conditions.

c. During a sequence of measurements, the atmospheric conditions in the test area shall not undergo significant or rapid changes.

d. The PCBs to be tested shall not be covered with a protective varnish.

e. During the testing period, the following precautions shall be taken:

   1. Keep the boards flat against a plane surface.
   2. Protect boards used for electrical tests from any contamination and hold them only by their edges during the tests.
   3. Before environmental exposure, soldering operation, electrical and mechanical testing, clean the boards in conformance with ECSS-Q-ST-70-08.

7.2 Group 1 — Visual inspection and non-destructive test

7.2.1 General

a. The PCBs number 1-6 shall be used for the tests.

7.2.2 Verification of marking

a. Each board shall be inspected with the naked eye for correct marking.

b. The marking shall be legible and resistant to test stresses.

c. The nonconformance criteria shall be as follows:

1. Identification impossible ..... **M**
2. Marking not conforming to supplier's specification ..... **M**
3. Defects not affecting identifications ..... **m**

7.2.3 Visual aspects

a. Each board shall be inspected by magnification ≥ ×10 with suitable lighting conditions to verify that construction and workmanship meet the requirements.

b. In case of any irregularity, the area shall be examined under ×20 - ×40 magnification.

c. The nonconformance criteria for the general cleanliness and contamination shall be as follows:

1. Contamination visible to the naked eye and not removable by cleaning according to ECSS-Q-ST-70-08..... **M**
2. Contamination visible to the naked eye and removable by cleaning according to ECSS-Q-ST-70-08 ..... **m**

d. The nonconformance criteria for the substrate shall be as follows:

1. Not in conformance with PCB manufacturer's trademark and required quality..... **M**
2. Scratches cutting glass fibre or leaving marks in the dielectric laminate that are affecting reliability..... **M**
3. Scratches not affecting reliability ..... **m**
4. Dents, crazing and haloing:
   (a) Visible to the naked eye ..... **M**
   (b) Only visible with magnification aids ..... **m**
5. Non-homogeneity regarding colouring and opacity ..... **m/M**
6. Discoloured copper oxide layer on internal layer is acceptable;
7. Inclusion of foreign matter, blistering or air bubbles:
   (a) Visible to the naked eye ..... **M**
   (b) Only visible with magnification aids ..... **m**
8. Delamination..... **M**
9. Measling:
   (a) General measling spread over the whole PCB surface..... **M**
   (b) Local measling that causes reduction of the insulation distance in the outer layer to below the requirement..... **M**

(c) Local measling that does not cause reduction of the insulation distance in the outer layer to below the requirement ..... **m**

10. Fungus growth ..... **M**

11. Delamination of cover layer (only for flexible PCB)..... **m/M**

e. The nonconformance criteria for non-plated-through holes shall be as follows:

1. Holes plated unintentionally ..... **m/M**

2. Incompletely drilled holes, missing or additional holes..... **m/M**

f. The nonconformance criteria for the routing shall be as follows:

1. Incomplete routing of board, such that dimensional or mechanical requirements are not met ..... **M**

2. Arbitrary cutting defects that remain acceptable within the dimensional requirements ..... **m**

g. The nonconformance criteria for the surface metallization shall be as follows:

1. Conductors or pads not conforming to supplier's specification ..... **M**

2. Terminal pads or conductors partially or completely missing..... **M**

3. Terminal pads or conductors that are cut ..... **M**

4. Terminal pads or conductors forming a short circuit..... **M**

5. Lifting/delamination of conductive pattern from substrate.... **M**

6. Scratches in the SnPb metallisation exposing the underlaying copper plating ..... **M**

7. Copper or nickel visible on top surface plated areas ..... **M**

NOTE Exposed copper can be accepted on the side of tracks or on the side of soldering pads.

8. Large number of superficial scratches not attributed to a manufacturing process evidencing bad workmanship..... **M**

9. Dewetting of fused tin lead finish on solder pads..... **M**

10. Granular surface structure of fused tin lead finish on solder pads ..... **m/M**

11. Corrosion of exposed copper..... **M**

12. Migration of underlaying copper through gold coating..... **M**

h. The nonconformance criteria for plated-through holes shall be as follows:

1. Incompletely drilled, additional or missing holes ..... **M**

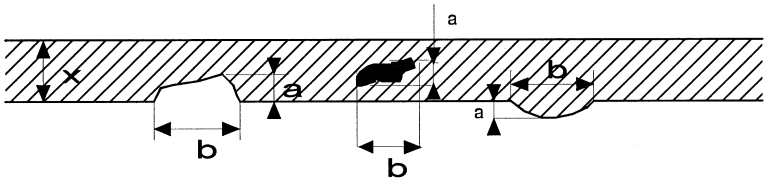
2. Partially or completely missing metallization..... **M**

3. Component holes ≥ 0,6 mm filled or partially filled with solder resulting in a diameter smaller than the requirement.. **m/M**

i. The nonconformance criteria for arbitrary defects of conductors and terminal pads shall be as follows:

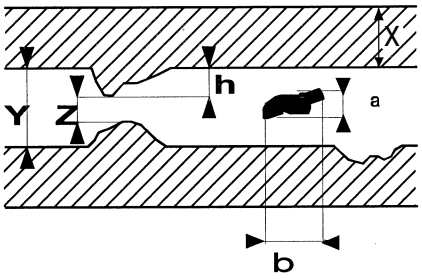
1. a ≤ 20 % of x
   and minimum conductor width > requirement ..... **m**
2. a > 20 % of x ..... **M**
3. minimum conductor width < requirement ..... **M**
4. b ≤ x ..... **m**
5. b > x ..... **M**
6. Opposite peaks: if z < 80 % of y ..... **M**
7. Isolated peaks or valleys: h > 20 % of x
   and z < requirement ..... **M**
8. Conducting island: a + h > 20 % of y
   and the isolation spacing < requirement ..... **M**
9. Minimum remaining spacing y - a < requirement ..... **M**
10. a > 20 % of y ..... **M**
11. b > y ..... **M**
12. Cover layer (flexible PCBs) covering part of solder pad
    (see Figure 7-3) ..... **M**

NOTE Intermittent and irregular metallisation defects on conductors are edge roughness (peak or valley), pits, pin holes, voids, protrusions or indentations, as shown in Figure 7-1, Figure 7-2 and Figure 7-3.



x: nominal conductor width

Figure 7-1: Arbitrary defects on conductors



y: nominal spacing between conductors

Figure 7-2: Arbitrary defects on spacing between conductors

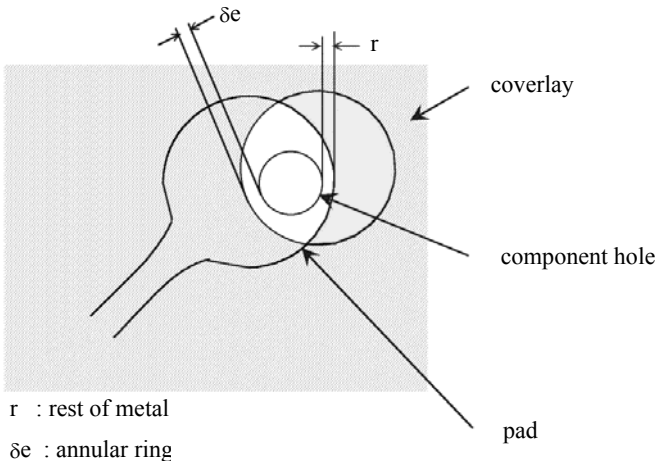


Figure 7-3 Misalignment of cover layer (for flexible PCBs)

7.2.4 External dimensions

a. Each board shall be measured by means of suitable standard measuring equipment to verify that the physical dimensions, including board thickness and external dimensions meet the supplier's specification.

b. The nonconformance criteria for the thickness of base laminate (average of 4 measurements on the board) shall be as follows:

   1. Thickness not conforming to tolerance limits of the supplier's specification ..... **M**

c. The nonconformance criteria for the length and width of board (average of 2 measurements on the board) shall be as follows:

   1. Length or width not conforming to tolerance limits of the supplier's specification ..... **M**

7.2.5 Warp

a. The PCBs shall be placed unrestrained on a plane horizontal surface with the convex side upward.

b. The warp shall be expressed in percentage terms.

c. The maximum bow between the plane horizontal surface and the PCB shall be measured as defined in Figure 7-4.

d. The length of the PCB shall be measured.

e. The warp percentage shall be calculated as defined in equation [7-1]:

$$Warp\ (\%) = \frac{Max.\ blow\ (mm)}{Length\ of\ the\ PCB\ (mm)} \times 100 \qquad [7\text{-}1]$$

f. The nonconformance criteria shall be as follows:

   1. Warp > requirement..... **M**

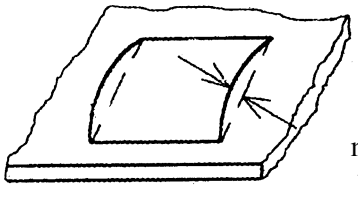


Figure 7-4: Warp

7.2.6 Twist

a. The PCB shall be placed on a plane horizontal surface so that it rests on three corners.

b. The twist shall be expressed in percentage terms.

c. The distance between the plane horizontal surface and the fourth corner of the PCB shall be measured as defined in Figure 7-5.

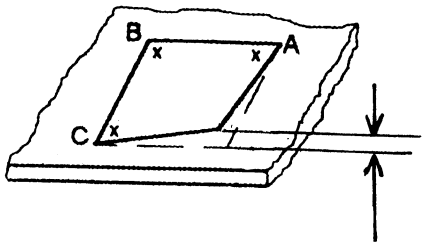
d. The length of the diagonal shall be measured.

e. The twist percentage shall be calculated as defined in equation [7-2].

$$Twist\ (\%) = \frac{Max.\ twist\ (mm)}{Length\ of\ the\ diagonal\ (mm)} \times 100 \qquad [7\text{-}2]$$

f. The nonconformance criteria shall be as follows:

1. Twist > requirement..... **M**



A, B and C are touching base

Figure 7-5: Twist

7.2.7 Subgroup 1.1 — Specific dimensional check

a. The PCBs number 1-2 shall be used for the tests.

b. The points to be measured on associated test coupons and PCB shall be decided between PCB manufacturer and qualification authority.

NOTE This can include for example:

- Minimum and maximum plated-through holes diameter and soldering pads diameter.
- Minimum and maximum conductor width.
- Minimum and maximum distance between conductors.

c. The measurements shall be presented in tabular form.

NOTE An example is given in Figure 7-6.

d. The measurements of dimensional parameters relating to metal plating shall be taken at the copper/board base interface or for high frequency circuits as required by the supplier (see clause 7.3.4, Figure 7-8).

NOTE 1 Examples for dimensional parameters relating to metal plating are width of conductors, spacing, minimum annular ring.

NOTE 2 Hole diameters can be measured with measuring gauges or a measuring microscope.

Plated-through holes					
Measuring point	Associated test coupon	∅ pad		∅ hole	
		Measured	Deviation	Measured	Deviation

Conductor's widths			
Measuring point	Test or coupon	Measured dimension	Deviation

Spacing between conductors			
Measuring point	Test or coupon	Measured dimension	Deviation

Figure 7-6 Example of a presentation of measurements in tabular form

e. The nonconformance criteria shall be as follows:

1. Dimensions not conforming to the circuit definition document and acceptable tolerance limits of the supplier's specification ..... **M**

NOTE Example of such dimensions are diameter of holes, width of conductors and diameter of terminal pads.

2. Diameter of non-soldering holes not conforming to tolerance limits of the supplier's specification ..... **m**

7.2.8 Subgroup 1.2 — Electrical measurements

7.2.8.1 General

a. The PCBs number 3-6 shall be used for the tests.

7.2.8.2 Intralayer insulation resistance on test pattern A

a. The test shall be carried out in conformance with tests 6a and 6b of IEC 60326-2-am 1 (1992-06).

b. A direct voltage of (500 ± 50) V shall be applied between the two closest conductors that are not electrically connected.

c. The insulation resistance (R) shall be measured 1 min after the voltage has been applied.

d. The nonconformance criteria shall be as follows:

1. R < requirement ..... **M**

7.2.8.3 Interlayer insulation resistance on test pattern H

a. The test shall be carried out in conformance with test 6c of IEC 60326-2-am 1 (1992-06).

b. The test shall be carried out in conformance with clause 7.2.8.2.

c. The voltage shall be applied between two ground planes or between one ground plane and one conductor that are superimposed, i.e. on two separate adjacent layers.

d. The nonconformance criteria shall be as follows:

1. R < requirement ..... **M**

7.2.8.4 Dielectric withstanding voltage intralayer on test pattern A and interlayer on test pattern H

a. The test shall be carried out in conformance with tests 7a and 7b of IEC 60326-2-am 1 (1992-06).

b. For interlayer measurements the test voltage shall be applied between two superimposed conductors (i.e. between layers).

c. For intralayer measurements the test voltage shall be applied between two adjoining, but not electrically connected conductors within the same layer.

d. The AC voltage at 50 Hz shall be gradually applied progressing from 200 V r.m.s. per second up to 1 500 V r.m.s. per mm of spacing between two conductors.

e. This voltage shall be kept steady for one minute.

f. The current shall be limited to 100 µA.

g. The final evaluation shall be visual aspect and measurements of the continuity.

h. The nonconformance criteria shall be as follows:

1. Evidence of breakdown, flashover or sparking ..... **M**

7.2.8.5 Continuity on test pattern D

a. The test shall be carried out in conformance with test 3a of IEC 60326-2-am 1 (1992-06).

b. Conductor continuity shall be tested by measuring the interconnection resistance on test pattern D.

c. The measurement shall be performed using a method ensuring an error no greater than 5 % (four wire method).

d. The current shall be limited to 0,1 A.

e. The measuring voltage shall not exceed 5 V.

f. The post-test measurements taken on each sample shall be compared with pre-test measurements.

g. The nonconformance criteria shall be as follows:

1. Discontinuity..... **M**

2. Dispersion greater than ±10 % with respect to the mean of values measured on the test patterns ..... **m/M**

7.2.8.6 Interconnection resistance on test pattern E

a. The test shall be carried out in conformance with test 3b of IEC 60326-2-am 1 (1992-06).

b. The test conditions shall be the same as for continuity testing.

c. The nonconformance criteria shall be as follows:

1. Discontinuity..... **M**

2. Dispersion greater than ±10 % with respect to the mean of values measured on the test pattern..... **M**

7.2.8.7 Impedance test on test pattern Y

a. The test shall be carried out in conformance with test 9a of IEC 60326-2-am 1 (1992-06).

b. The measuring method shall be specified by the supplier.

7.2.8.8 Dielectric constant and loss tangent for high frequency materials on test pattern W

a. The measuring method shall be specified by the supplier:

   1. Annular ring;

   2. Closed cavity or other method.

7.3 Group 2 — Miscellaneous tests

7.3.1 General

a. The PCBs number 1-2 shall be used for the tests.

7.3.2 Subgroup 2.1 — Solderability test — Wettability on test pattern J

a. The test shall be carried out in conformance with test 14a of IEC 60326-2-am 1 (1992-06) and IEC 60068-2-20-am 2 (1987-01), test TC.

b. Non-activated rosin-based flux shall be used as specified in ECSS-Q-ST-70-08.

c. The solder shall be tin-lead 60/40 or 63/37 as specified in ECSS-Q-ST-70-08.

d. The test machine shall be a rotary dip tester or similar equipment.

e. The specimens shall be fluxed by immersion.

f. Surplus flux shall be allowed to flow off the specimen by keeping it upright for 5 min.

g. The specimen shall be arranged on the soldering machine and brought into contact with the surface of the solder bath that is kept at the temperature of (235 ± 5) °C for the below specified period:

   1. For evaluation of wetting: 3 s.

   2. For evaluation of dewetting: 10 s.

h. A visual inspection shall be made with a ×10 magnification.

   NOTE A microsection can also be performed and a visual inspection made at a magnification greater than ×100.

i. The nonconformance criteria shall be as follows:

   1. Poor wettability of solder pads and plated-through holes: see Figure 7-7 ..... **M**

   2. Microsectioning: broken metallization..... **M**

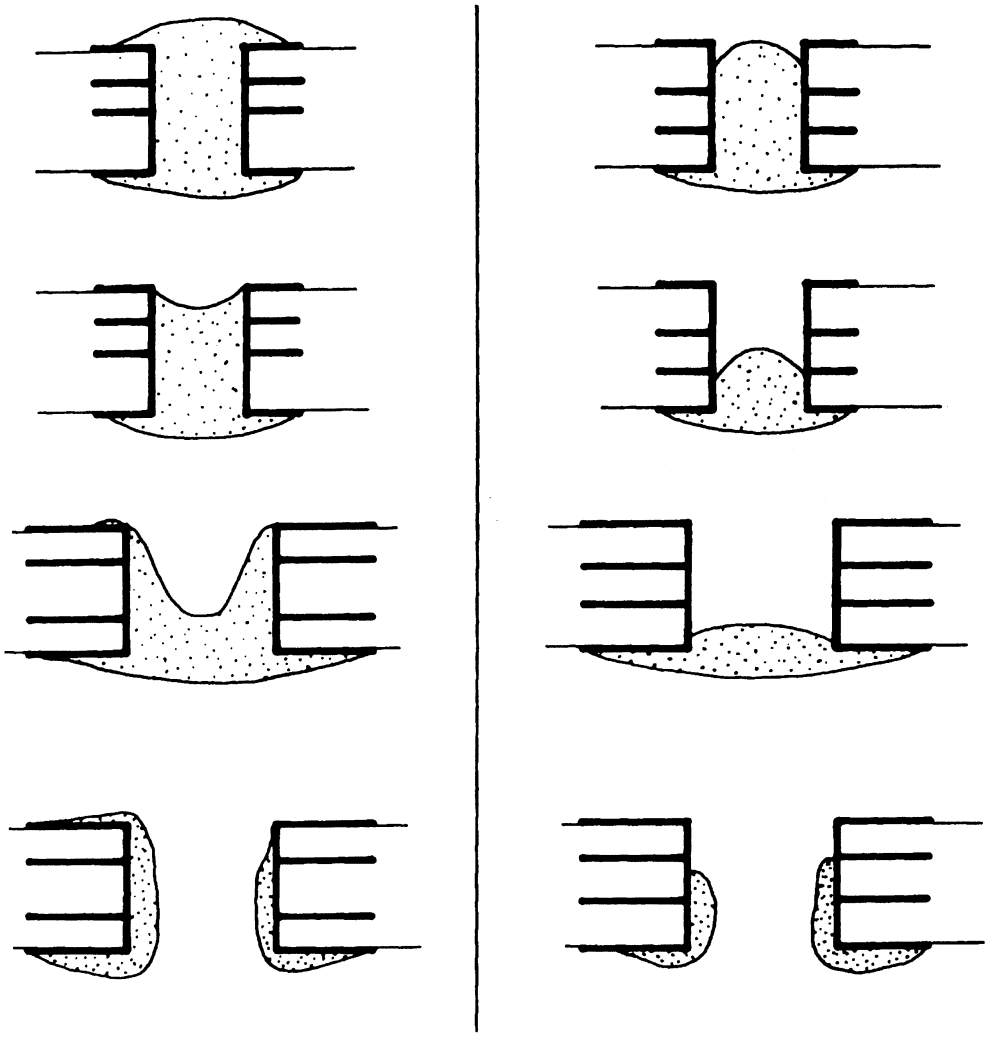


Figure 7-7: Wettability of terminal pads and plated-through holes

7.3.3 Subgroup 2.2 — Mechanical tests

7.3.3.1 Peel strength on test pattern B

a. The test shall be carried out in conformance with test 10a of IEC 60326-2-am 2 (1992-06).

b. The conductor selected shall be peeled back at one end for a length of about 10 mm.

c. The detached end of the conductor shall be firmly gripped over its whole width.

d. Traction shall be applied in a direction perpendicular to the plane of the PCB until the copper starts to peel away.

e. The rate of traction shall be kept constant at 50 mm/min.

f. The traction direction shall be kept perpendicular to the plane of the PCB.

g. Machine inertia shall have no effect on the measurement.

h. The conductor width to be taken into account shall be the actual width over which the conductor is adhered to the substrate.

i. The nonconformance criteria for the peel strength shall be as follows:

1. Peel strength < requirement..... **M**

7.3.3.2 Pull-off strength on test pattern B

a. The test shall be carried out in conformance with test 11a of IEC 60326-2-am 1 (1992-06).

b. Temperature of iron shall be (270 ± 10) °C.

c. The solder shall be tin-lead 60/40 or 63/37 alloy with non-corrosive resin core as specified in ECSS-Q-ST-70-08.

d. After application of the soldering flux specified in IEC 60068-2-20-am 2 (1987-01), test TC, the pads shall be tinned for (4 ± 1) s.

e. A tinned copper wire with a diameter of 0,3 mm less than the hole diameter and with a length of approximately 150 mm shall be soldered onto the pad.

f. Soldering shall be between 2 s and 3 s.

g. After 5 min ambient reconditioning the soldering operations shall be repeated (second soldering).

h. The ambient reconditioning time before final measurement shall be more than 10 min.

i. For the measurement of the pull-off strength the following steps shall be carried out:

1. Force is applied on the wire by using a traction machine.

2. This force increases with a constant rate of between 5 N/s and 50 N/s until the terminal pad separates from the board base material.

NOTE The preferred rate is 10 N/s.

j. The nonconformance criteria for the pull-off strength for terminal pads shall be as follows:

1. Pull-off strength < requirement..... **M**

7.3.3.3 Flexural fatigue on test pattern X (only for double sided flexible PCB)

a. The test shall be carried out in conformance with test 21a of IEC 60326-2-am 1 (1992-06).

b. The equipment shall be similar to that described in IEC 60249-1-am 4 (1993-05) clause 3.12-2 and Figure 6-13.

c. Short insulated wires shall be connected to the ends of the conductive patterns (frontside and backside in series).

d. The specimen shall be mounted on the device such that the interior diameter of the loop is (9,6 ± 0,4) mm.

e. The alternating movement shall be such that the loop moves at least 25 mm and that the specimen is not curved at either end.

f. The pace of the alternating movement shall not exceed ten cycles per minute.

g. For the test the alternating movement shall be continued until an electrical discontinuity appears or until 500 cycles are completed without defect.

h. The nonconformance criteria shall be as follows:

1. Discontinuity occuring before 250 cycles..... **M**
2. Discontinuity occuring between 250 cycles and 500 cycles..... **m**
3. Lifting of insulation coating from conductors..... **m/M**
4. Lifting of conductors from board base material ..... **m/M**
5. Lifting of insulation coating from board base material..... **m/M**

7.3.3.4 Bending test (only for rigid-flex)

a. The test shall be carried out in conformance with MIL-P-50884C clause 3.6.5 and 4.8.4.5.

b. A 25 cycle folding test shall be carried out as described in MIL-P-50884C clause 4.8.4.5.

c. There shall be no electrical defect or degradations.

d. The nonconformance criteria shall be as follows:

1. Any degradation of continuity..... **M**

7.3.4 Subgroup 2.3 — Coatings tests

7.3.4.1 Coating adhesion of non-fused SnPb finishes on test pattern G

a. The test shall be carried out in conformance with test 13a of IEC 60326-2-am 1 (1992-06).

b. The test shall be carried out on SnPb finished boards before reflow of test board.

c. After cleaning, an adhesive tape, at least 50 mm long, shall be applied to the test surface and pressed down to eliminate all air bubbles.

d. After 10 s, the tape shall be quickly pulled off perpendicular to the coating surface.

e. The surface area to be tested shall be 1 cm^2 of conductor

NOTE Example of tape, which can be used: TESA 4104 width 19 mm.

f. The nonconformance criteria shall be as follows:

1. If part of SnPb coating is sticking to tape or test surface shows scaling ..... **M**

7.3.4.2 Analysis of SnPb coating on test pattern G

a. The tin-lead alloy shall be chemically dissolved.

b. The relative quantities of tin and lead shall be determined by atomic absorption spectrometry.

NOTE This is the proposed method for SnPb. Any other method resulting in the same degree of precision can be used.

c. The nonconformance criteria shall be as follows:

1. If the content of tin and lead is not conforming to the tolerance limits of the requirement ..... **M**

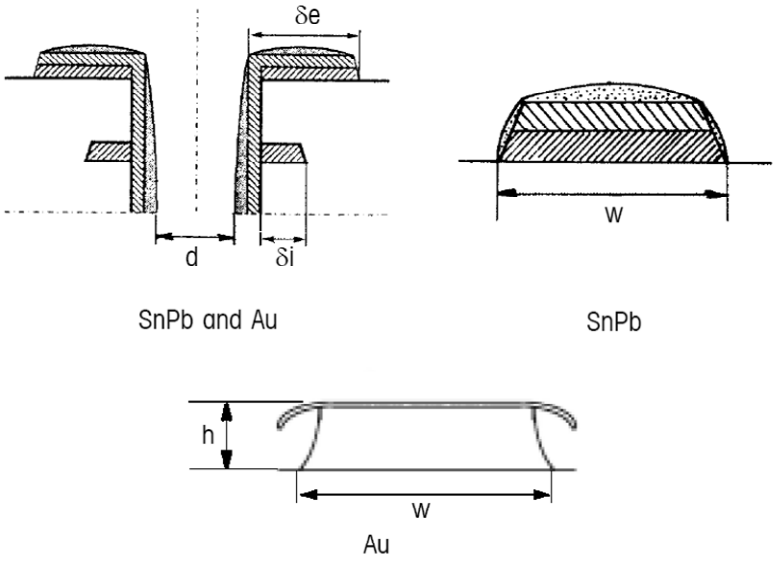
7.3.4.3 Microsectioning on test pattern F

7.3.4.3.1 General

a. The test shall be carried out in conformance with tests 1c and 15b of IEC 60326-2-am 1 (1992-06).

b. For high frequency conductors the customer shall specify at which height of the conductor the width shall be measured (see Figure 7-8).

NOTE Microsection with typical defects in PTH is shown in Annex F.



w width of conductor
δe minimum annular erring on external layer
δe minimum annular erring on internal layer
d diameter of plated-through hole
h height of conductor

Figure 7-8: Dimensional parameters to be measured

7.3.4.3.2 Thickness of metal-plating

a. The test shall be carried out on a microsection.

b. Observations shall be made with magnification greater than or equal to ×250.

c. The nonconformance criteria for the thickness of copper plating on external layers shall be as follows:

1. Basic copper:

(a) Thickness not conforming to the supplier's specification ..... **M**

2. Basic copper plus electrolytic copper on non-soldering areas:

(a) Thickness < requirement ..... **M**

3. Basic copper plus electrolytic copper soldering pads (see Figure 7-9 number 2):

(a) Thickness < 40 µm ..... **M**

d. The nonconformance criteria for the thickness of copper in plated-through holes that are component holes shall be as follows:

1. Average thickness based on 3 measurements taken on the hole walls (see Figure 7-9 number 1):

(a) Thickness < requirement ..... **M**

e. The nonconformance criteria for the thickness of copper layer on internal layers shall be as follows:

1. Thickness not conforming to supplier's specification ..... **M**

f. The nonconformance criteria for the thickness of copper in plated-through holes that are vias, buried vias or blind vias shall be as follows:

1. Thickness < requirement ..... **M**

g. The nonconformance criteria for the thickness of tin-lead alloy on surface, measured along the conductor longitudinal axis, shall be as follows:

1. 5 µm < thickness < 8 µm ..... **m**
2. Thickness < 5 µm ..... **M**

h. The nonconformance criteria for the thickness of tin-lead alloy in holes shall be as follows:

1. In highest part of half of the hole wall height (see Figure 7-9 number 3): thickness < 8 µm ..... **M**
2. On angle of hole corner (see Figure 7-9 number 4): 1 µm < thickness < 2 µm ..... **m**
3. On angle of hole corner (see Figure 7-9 number 4): thickness < 1 µm ..... **M**

i. The nonconformance criteria for the thickness of electrolytic Au or Au/Ni on surface and in holes (measured along the conductor longitudinal axis) shall be as follows:

1. Au for manual soldering on nickel:
   (a) Thickness < 1 µm ..... **M**
   (b) Thickness > 7 µm ..... **M**
2. Au for manual soldering on copper:
   (a) Thickness < 3 µm ..... **M**
   (b) Thickness > 7 µm ..... **M**
3. Au for high frequency circuits or other assembly methods - as specified by customer:
   (a) Thickness not conforming to tolerance limits of supplier's specification ..... **M**
4. Ni:
   (a) Thickness < 2 µm ..... **M**
   (b) Thickness > 10 µm ..... **M**

j. The nonconformance criteria for the distance between SnPb and Au overlap and the termination pad designated for soldering shall be as follows:

1. Distance < 200 µm ..... **M**

k. The nonconformance criteria for the etch undercut on external and internal layers for fused SnPb (see Figure 7-10) shall be as follows:

1. Undercut (u) > total copper thickness (h) ..... **M**

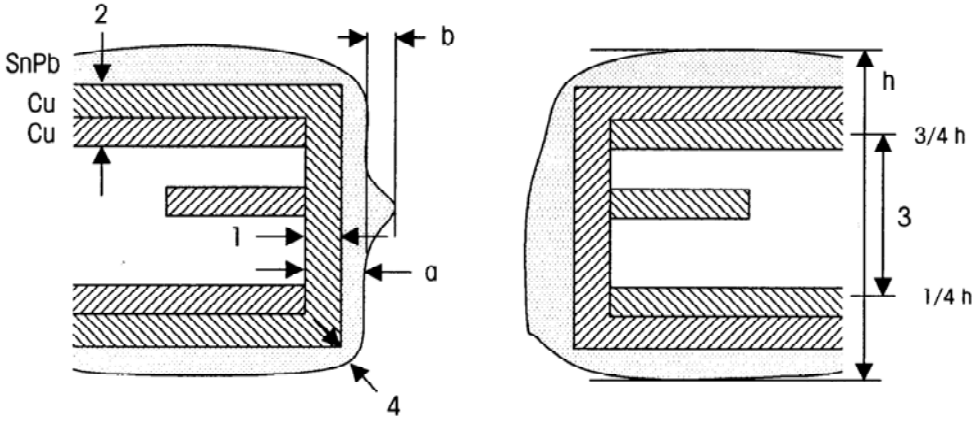
l. The nonconformance criteria for the etch undercut on external and internal layers for Au plating with or without Ni finish (see Figure 7-11) shall be as follows:

1. If undercut (d) > 30 µm..... **M**

m. The nonconformance criteria for the etch overhang on external layers for Au plating with or without Ni finish (see Figure 7-12) shall be as follows:

1. If overhang (D) > 2× thickness of total copper ..... **M**

NOTE For high frequency application overhang is normally undesirable and can be removed mechanically.



Key
1 = Cu in PTH
2 = Cu at surface pattern
3 = SnPB in hole
4 = SnPb in angle area
internal buging b < a

Figure 7-9: Microsection of a PTH

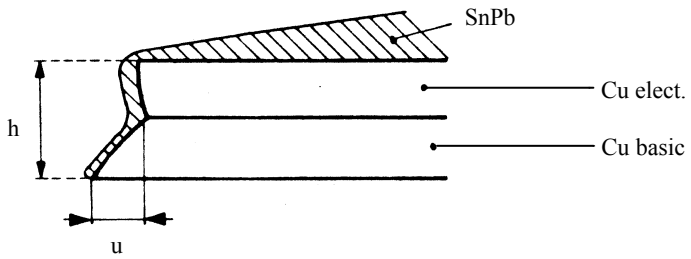


Figure 7-10: Undercut for PCBs with fused SnPb finish

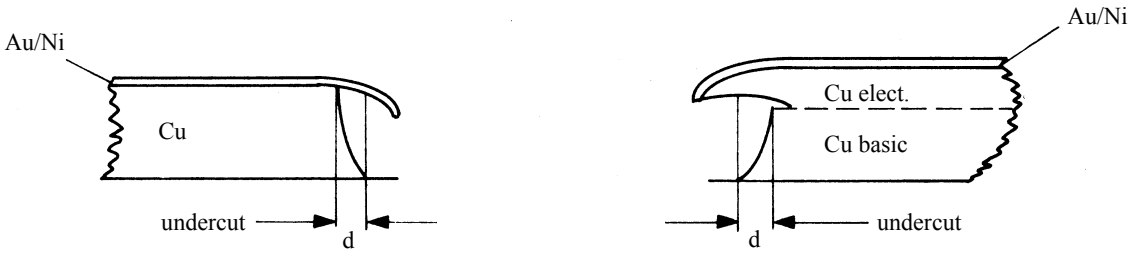


Figure 7-11: Undercut for PCBs with Au/Ni or Au finish

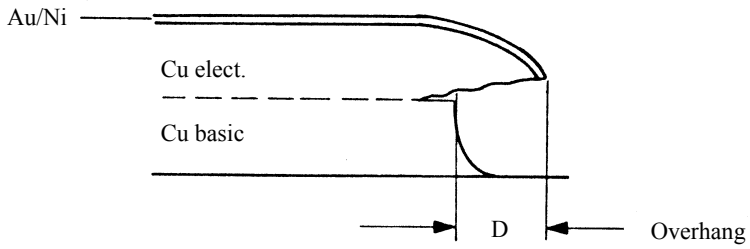


Figure 7-12: Overhang for PCBs with Au/Ni or Au finish

7.3.4.3.3 Aspect of plated-through holes

a. Sections of plated-through holes shall be observed with magnification greater than or equal to ×100.

b. Layer misregistration compared to the minimum annular ring on pads.

c. The nonconformance criteria for the layer misregistration on the external layer (see Figure 7-8) shall be as follows:

   1. δe < requirement ..... **M**

d. The nonconformance criteria for the layer misregistration on the internal layers (see Figure 7-8) shall be as follows:

   1. δi < requirement ..... **M**
   2. Minimum insulation between layers < requirement ..... **M**

e. The nonconformance criteria for irregular drilling (see Figure 7-13) shall be as follows:

   1. Infiltration of metal into base laminate:
      (a) 40 µm < infiltration < 80 µm ..... **m**
      (b) Infiltration> 80 µm ..... **M**
   2. Presence of adhesive on basic copper not leading to rupture during fusing process or thermal shock ..... **m**
   3. Adhesion defects between metal-plating and basic copper .... **M**
   4. Adhesion defects between metal-plating and inner layers ..... **M**
   5. Resin smear on the interface between internal conductor and plated copper greater than 15 % of conductor thickness . **M**

6. Void in resin greater than 50 % of basic copper thickness..... **M**

f. The nonconformance criteria for voids in PCB base laminate substrate and resin recession in holes (see Figure 7-14) shall be as follows:

1. Voids in the PCB base laminate substrate:

(a) Lc > 80 µm ..... **M**

2. At edge of metal-plating:

(a) Sum of resin recession h_c > 20 % sum h_i..... **M**

3. Resin recession in hole before or after test:

(a) Resin recession between 10 % and 20 % of height of hole ..... **m**

(b) If resin recession > 20 % of height of hole..... **M**

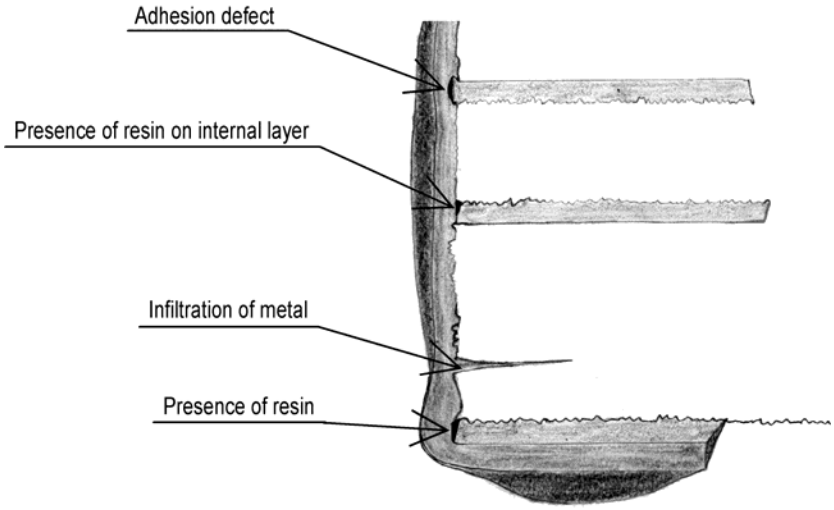
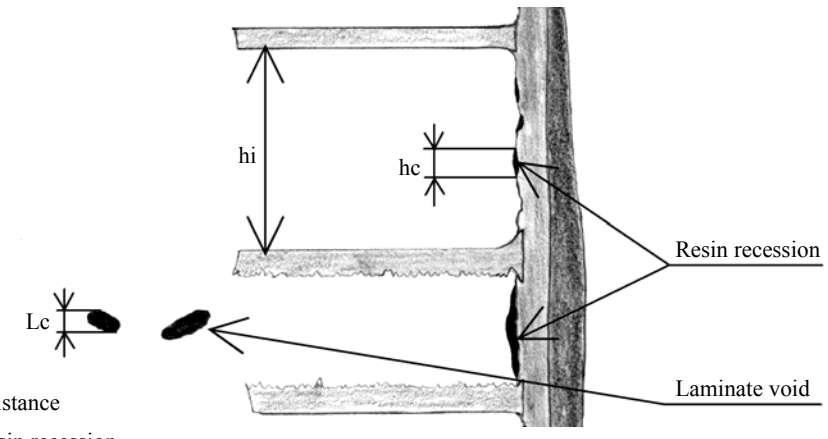


Figure 7-13: Microsection in PTH: Possible defects



hi = insulation distance

hc = height of resin recession

Lc = size of the void

Figure 7-14: Microsection of PTH: Possible defects

g. The nonconformance criteria for the copper plating inside buried, blind, via and component holes shall be as follows:

1. Void in copper plating in holes ..... **M**

h. The nonconformance criteria for the resin inside buried vias shall be in conformance with Figure 7-15.

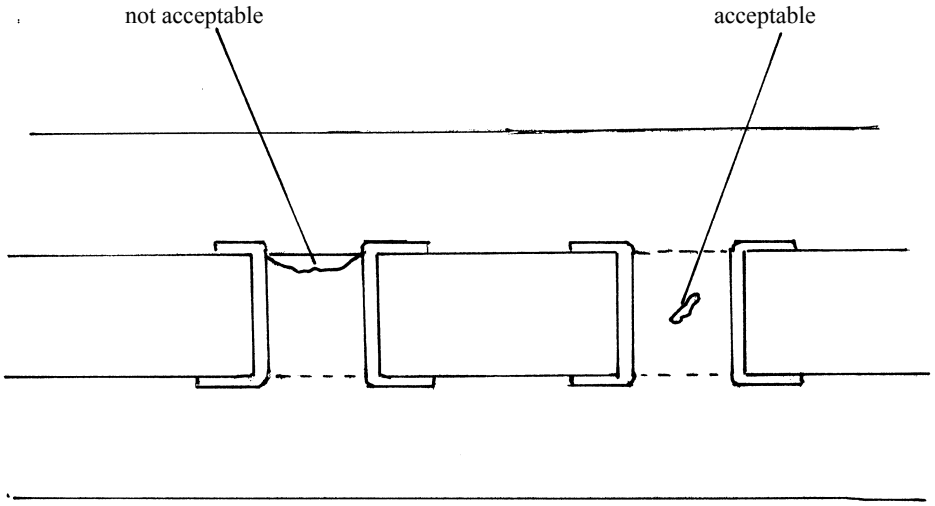


Figure 7-15: Voids in resin inside buried vias

7.3.5 Subgroup 2.4 — Electrical tests

7.3.5.1 Current overload on test pattern E

7.3.5.1.1 General

a. The test shall be carried out in conformance with test 5 of IEC 60326-2-am 1 (1992-06).

7.3.5.1.2 Short-time overload

a. The test shall be carried out on a pattern including holes (50 holes minimum) connected in series by conductors.

b. Two connecting wires shall be soldered to both ends of the circuit being tested.

c. A measurement shall be taken of the interconnection resistance between the ends.

d. Voltage shall be applied between ends in such a way that current flow into the circuit is:

1. 7 A for 35 μm thick basic copper.

2. 14 A for 70 μm thick basic copper.

e. This voltage shall be maintained for (4 ± 1) s.

f. After ambient reconditioning for 2 h, circuit continuity shall be checked by measuring the interconnection resistance.

g. The nonconformance criteria shall be as follows:

1. Electrical discontinuity ..... **M**
2. Blistering visible to the naked eye ..... **M**
3. Variation in interconnection resistance increased by more than +10 %..... **M**

7.3.5.1.3 Long-time overload

a. Same initial conditions as in clause 7.3.5.1.2 with application of a voltage to the circuit terminals such that the current varies by successive steps:

1. I_0 = 2 A for 3 min.
2. I_1 = 4 A for 3 min;
3. Further increments of 2 A every 3 min until destruction (open circuit) or if for I = 18 A circuit discontinuity is not achieved.

b. The nonconformance criteria shall be as follows:

1. destructive current < requirement ..... **M**

7.3.5.2 Internal short circuit on test pattern C

a. The test shall be carried out in conformance with test 4a of IEC 60326-2-am 1 (1992-06).

b. The test shall be carried out in an insulation area in conformance with Figure 7-16.

c. A polarized voltage of 100 V DC shall be applied between the ground plane connected to earth and the plated-through hole passing through the access opening for 1 min (see Figure 7-16).

d. The insulation resistance shall be measured.

e. The nonconformance criteria shall be as follows:

1. Insulation resistance < requirement..... **M**

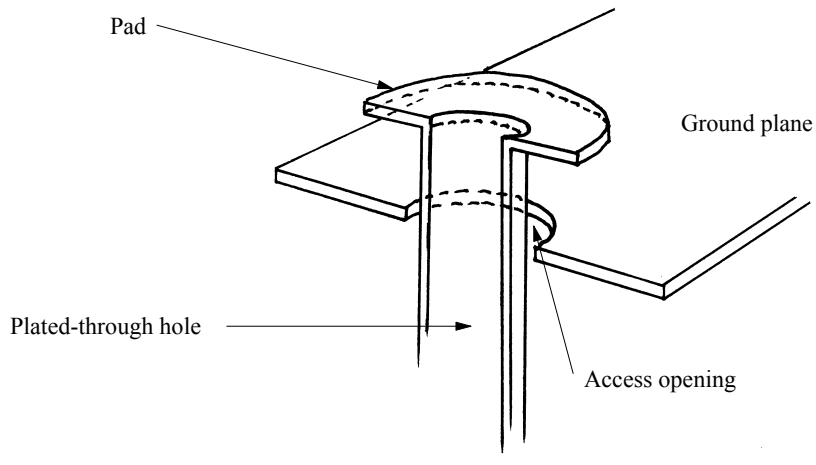


Figure 7-16: Test for internal short circuit

7.3.6 Subgroup 2.5 — Physical tests on test pattern K

7.3.6.1 Water absorption (optional)

a. The specimen, completely devoid of copper, shall be dried in an oven for (24 ± 1) h at a temperature between 50 °C and 55 °C.

b. It shall be cooled in a container with a siccative until the temperature is (23 ± 1) °C.

c. At this stage it shall be weighed to the nearest milligram.

d. It shall be placed in a de-ionized water bath maintained at (23 ± 0,5) °C.

e. It shall be placed on the edge, remain completely submerged and not in contact with the edges of the bath.

f. After (24 ± 1) h, it shall be withdrawn from the water and dried with a dry fluff-free cloth or filter paper.

g. It shall be weighed to the nearest milligram in the minute following its removal from the water.

h. The nonconformance criteria for the percentage of absorbed water (Δm) in various types of substrates shall be as follows:

1. Glass fibre-epoxy base laminate: Δm > 0,2 % ..... **M**
2. Glass fibre-polyimide base laminate: Δm > 0,8 % ..... **M**
3. Random glass reinforced PTFE resin: Δm > 0,2 % ..... **M**
4. Ceramic filled woven-glass reinforced PTFE resin: Δm > 0,1 % ..... **M**
5. Ceramic filled PTFE resin: Δm > 0,1 % ..... **M**
6. Ceramic filled cross-linked hydrocarbon/thermoset polymer: Δm > 0,1 % ..... **M**
7. Quartz filled polyimide: Δm > 0,8 %..... **M**
8. Polyimide: Δm > 0,8 % ..... **M**

7.3.6.2 Outgassing

a. The test shall be carried out in conformance with ECSS-Q-ST-70-02.

b. The test shall be carried out on a specimen entirely devoid of copper in order to determine the volume of included gas constituents, which threaten to contaminate a space environment.

c. The outgassing shall be determined after measurement of the difference in weight of the specimen before and after the test.

d. The nonconformance criteria shall be as follows:

1. TML or RML > 1 % (see ECSS-Q-ST-70-02 clause 7.2.3) and CVCM > 0,1 % ..... **M**

7.4 Group 3 — Thermal stress and thermal shock (on PCB)

7.4.1 General

a. The PCB number 3 shall be used for the tests.

b. PCB manufacturer and the qualification authority shall agree on omission of any of these tests.

NOTE The solder bath test is to simulate solder wave assembly of PCBs and is followed by the vapour phase solder test to simulate solder reflow assembly of PCBs. The rework test simulates hand solder assembly, rework and repair of PCBs.

7.4.2 Solder bath float and vapour phase reflow simulation (on board without test pattern F)

7.4.2.1 Solder bath floating test

a. The test shall be carried out in conformance with test 19c of IEC 60326-2-am 1 (1992-06).

b. The thermal shock shall be applied to one side of the test board by floating it in a solder bath.

c. After conditioning for 6 h at (140 ± 2) °C, the board shall be floated in a 63/37 solder bath maintained at (287 ± 6) °C.

d. The duration of the test shall be 10 s.

e. Ambient reconditioning shall be more than 1 h, after which a visual inspection shall be performed to evaluate the substrate visual aspect.

7.4.2.2 Vapour phase simulation test

a. The test shall be carried out in conformance with test 19g of IEC 60326-2-am 1 (1992-06).

b. A thermal shock shall be applied to the whole board of the test board by immersion in the vapour phase of a fluorinated chemical bath.

c. Depending on the time passed after the first thermal shock (during the solder bath float test), the board shall be conditioned for 1 h to 6 h at (140 ± 2) °C.

d. The other side compared to the procedure in 10.2.1.2a of the same test board shall be coated with flux or a solder paste with flux and baked.

e. The test board shall be lowered into the vapour phase at a temperature of (215 ± 2) °C.

f. The duration of the exposure shall be 10 s.

g. Ambient reconditioning shall be more than 1 h, after which the following final measurements shall be performed:

1. Substrate visual aspect;
2. Peel strength on test pattern B;
3. Continuity on test pattern D;
4. Interconnection resistance on test pattern E;
5. Microsectioning on test pattern J.

h. The nonconformance criteria shall be as follows:

1. Peel strength < requirement ..... **M**
2. Delamination ..... **M**
3. Localized/generalized measling ..... **m/M**
4. General occurrence of terminal pads that show first signs of pad lifting ..... **M**
5. Any terminal pad that show pad lifting ..... **M**
6. Increase in interconnection resistance > +10 % ..... **M**
7. Microsectioning: broken metallization ..... **M**

7.4.3 Rework simulation (thermal shock, hand soldering) on test pattern F

a. The test shall be carried out in conformance with test 19d of IEC 60326-2-am 1 (1992-06).

b. A thermal shock shall be applied to the test pattern F by soldering and unsoldering a wire five times.

c. Copper wires shall be of diameter:

1. 0,51 mm for holes of ∅ = 0,8 mm (∅ of land = 2 mm).
2. 1,02 mm for holes of ∅ = 1,6 mm (∅ of land = 4 mm).

d. A sufficient wire length to fit the gripping mechanism of the tensile tester shall be prepared for each hole.

e. The wires shall be inserted in the holes and soldered to the terminal areas using a conventional soldering iron, operating at a tip temperature of (270 ± 10) °C.

f. The wires shall not be clinched on the other side of the PCB.

g. They shall be soldered and then unsoldered and removed from the hole.

h. This cycle shall be repeated five times, using a new wire for each soldering operation.

i. During the soldering/unsoldering cycles, the soldering iron shall be applied to the wire and not to the terminal pads.

j. After the fifth cycle, the wires shall be soldered into the holes and the PCB shall be left to cool for 30 min minimum.

k. A microsection shall be performed on the soldered holes to evaluate possible cracking of the copper of the through-hole plating.

l. The nonconformance criteria shall be as follows:

1. Cracked copper ..... **M**

7.5 Group 4 — Thermal cycling (on PCB)

a. The PCBs number 4-5 shall be used for the tests.

b. The test shall be carried out in conformance with test Nb of IEC 60068-2-14-am 1 (1986-01).

c. The test is performed on an entire PCB.

d. The temperature range ΔT shall be 200 °C with the highest temperature not exceeding the glass transition temperature of the substrate.

NOTE The lower temperature can be (-70 ± 15) °C.

e. The number of cycles shall be 200.

f. The temperature change rate shall be approximately 10 °C/min.

g. The conditioning time at the extreme temperatures within a cycle shall be 15 min.

h. After ambient reconditioning for at least 2 h, the following final measurements shall be performed:

1. Substrate visual aspect.
2. Peel strength on test pattern B.
3. Continuity on test pattern D and interconnection resistance on test pattern E.
4. Intra- and interlayer insulation resistance on test pattern A and H.
5. Withstanding voltage on test patterns A and H.
6. Microsectioning on test pattern F.

i. The nonconformance criteria shall be as follows:

1. Peel strength < requirement ..... **M**
2. Increase in resistance > +10 % ..... **M**
3. Intralayer insulation resistance < 10^3 MΩ ..... **M**
4. Interlayer insulation resistance < 10^4 MΩ ..... **M**
5. Evidence of flashover, breakdown, sparking ..... **M**
6. Microsectioning: broken metallization ..... **M**
7. Technological and functional defects ..... **M**

7.6 Group 5 — Damp heat — Steam ageing (on PCB)

7.6.1 General

a. The PCB number 6 shall be used for the tests.

7.6.2 Damp heat (on entire PCB excluding test pattern F)

a. The test shall be carried out in conformance with test Ca of IEC 60068-2-3 (1969-01).

b. The test conditions shall be:

1. Temperature: (40 ± 2) °C.
2. Relative humidity: 93 % (+2 %, -3 %).
3. Duration of test: 10 days.
4. No operation during test.

c. The sample shall be reconditioned to normal atmospheric conditions for a period of at least 1 h and not more than 2 h, after which the following final measurements shall be taken:

1. Peel strength on test pattern B.
2. Intra- and interlayer insulation resistance on test patterns A and H.
3. Withstanding voltage on test patterns A and H.
4. Microsectioning (if necessary) on test pattern F.
5. Corrosion of circuits for electrolytic Au finish.

d. The nonconformance criteria shall be as follows:

1. Peel strength < requirement ..... **M**
2. Intralayer insulation resistance < 10^3 MΩ ..... **M**
3. Interlayer insulation resistance < 10^4 MΩ ..... **M**
4. Evidence of flashover, breakdown, sparking ..... **M**
5. Microsectioning (if required): broken metallization ..... **M**
6. Evidence of corrosion ..... **M**

7.6.3 Steam ageing on test pattern F

a. The test shall be carried out in conformance with test 20a of IEC 60326-2-am 1 (1992-06).

NOTE This test is intended to give an indication of the effects of storage on the solderability of the PCBs.

b. The flux shall be non-activated, rosin-based flux as specified in ECSS-Q-ST-70-08.

c. The solder shall be tin-lead 60/40 or 63/37 alloy with non-corrosive resin core as specified in ECSS-Q-ST-70-08.

d. The test machine shall be a steam generator or similar equipment.

e. The specimens shall be fluxed by immersion.

f. Surplus flux shall be allowed to flow off the specimen by keeping it upright for 5 min.

g. The specimen shall be exposed in the steam generator machine for approximately 80 min.

h. After closing the generator, it shall be purged with nitrogen at a flow rate between 250 ml/min and 750 ml/min.

i. The specimen carrier shall rotate at a speed of 5 revolutions per minute to 50 revolutions per minute.

j. The temperature inside machine shall be (100 ± 2) °C and stabilized for (5 ± 1) min.

k. The nitrogen flow shall be switched off.

l. The 90 °C condensed steam rate in the chamber shall be controlled to (5 ± 0,5) l/min.

m. A mixture of pure oxygen 20 % and nitrogen 80 % with a flow rate of (100 ± 10) ml/min shall be switched on for (60 ± 5) min.

n. After removing the specimens from the steam generator machine, they shall be dried.

o. A solderability test shall be performed.

p. A visual inspection shall be performed with a ×10 magnification.

q. If the result of the visual inspection is deemed unsatisfactory, a microsection shall be performed. In this case a visual inspection shall be made with a magnification greater than ×100.

r. The nonconformance criteria shall be as follows:

1. Poor wettability of conductors, terminal pads and plated-through holes: see Figure 7-7 for terminal pads and plated-through holes..... **M**
2. Microsectioning (if necessary): broken metallization..... **M**
3. Evidence of corrosion ..... **M**

8
Quality assurance for manufacturing

8.1 General

a. The quality assurance requirements defined in ECSS-Q-ST-20 shall apply.

b. No repair shall be performed on finished bare PCBs.

8.2 Data

a. The supplier shall retain the quality records for at least ten years or in accordance with project business agreement requirements.

NOTE Example of such quality records are logbooks.

b. The quality records shall be composed of the following:

1. Documentation of the final inspection of manufactured PCBs.
2. Nonconformance reports and corrective actions in conformance with ECSS-Q-ST-10-09;
3. Copy of the test results (including evaluation and qualification test report) in conformance with Annex A and Annex B.

8.3 Incoming inspection of raw materials

a. Raw materials and semi-finished products shall be selected, inspected and tested (e.g. chemical and physical tests) in conformance with the production flow chart.

b. The PCB manufacturer shall separate and, and prevent the use of, raw materials and semi-finished products that are awaiting completion of test results.

8.4 Traceability

a. The PCB manufacturer's control system shall make it possible to determine, in respect of any lot of PCBs, the history of all raw materials and semi-finished products listed in the production flow chart and the individual process steps mentioned herein, and to verify that the items originate from one production lot.

b. In the case of materials with limited shelf-life, the PCB manufacturer's control system shall provide for means to verify the validity of the relevant material for use.

c. The verification and re-certification procedure shall be in accordance with ECSS-Q-ST-70-22.

8.5 Calibration

a. The PCB manufacturer shall calibrate any electrical and mechanical manufacturing equipment to traceable reference standards.

b. The PCB manufacturer shall record any suspected or actual equipment failure as a nonconformance report according to ECSS-Q-ST-20.

NOTE This is to ensure that previous manufacturing results are examined to ascertain whether or not a re-inspection or re-testing is necessary.

8.6 Workmanship standards

a. Visual standards consisting of photos or drawings of microsections or other visual aids that clearly illustrate the quality characteristics required shall be available to each inspector.

8.7 Inspection

a. During all stages of the manufacturing the inspection points shall be observed. Quality conformance inspection shall be performed using quality test specimen and microsections.

8.8 Operator and inspector training

a. All operators and inspectors shall be suitably trained for their task and for the understanding of the necessary quality assurance requirements.

8.9 Quality test specimen

a. The PCB manufacturer shall produce with each panel quality test specimens for in-house quality control purposes and one to be supplied to the qualification authority in accordance with ECSS-Q-ST-70-11 clause 5.5.1.

8.10 Microsection

a. The PCB manufacturer shall produce with each panel microsections for in-house quality control purposes and one to be supplied to the qualification authority in accordance with ECSS-Q-ST-70-11 clause 5.5.2.

8.11 Final inspection and tests

a. The PCB manufacturer shall have an in-house procedure for final inspection of PCBs; this shall include visual inspection according to clause 7.2 and specific dimensional check according to clause 7.2.7 and the qualification authority's requirements.

b. Electrical testing shall be agreed between PCB manufacturer and the qualification authority in accordance with ECSS-Q-ST-70-11 clause 5.5.2.

c. The quality test specimen representative of the PCB and produced on the same panel shall be subjected to continuity test, solderability test and thermal stress test.

NOTE Other specific test can be agreed with the customer.

d. Microsectioning of holes as received and after thermal stress tests (rework simulation) shall be performed.

e. The PCBs shall be cleaned and dried before packaging according to ECSS-Q-ST-70-11 clause 5.4.2.

f. The cleanliness values shall be in accordance with ECSS-Q-ST-70-08 clause 11.3.

8.12 Delivery

a. The PCB manufacturer shall have suitable packaging facilities in conformance with ECSS-Q-ST-70-11 clause 5.4.

b. The documentation shall be done in conformance with ECSS-Q-ST-70-11 clause 5.3.3.

9
Requirements for PCBs

9.1 Rigid single-sided and double-sided PCBs

a. The base materials shall be in conformance with ECSS-Q-ST-70, IEC specifications and IPC-4101 and shall be one of the following:

   1. Woven-glass-reinforced epoxy resin FR4;
   2. Woven-glass-reinforced polyimide resin.

b. The limits for the dimensional characteristics shall be as follows:

   1. External dimension tolerance: ±0,2 mm;
   2. Thickness tolerance: ±10 %;
   3. Active board size, maximum: supplier's specification;
   4. Board thickness maximum: 3,2 mm;
   5. Positioning tolerance between registration mark and edge of circuit: ±0,2 mm;
   6. Conductor width: 200 µm minimum (for fine pitch 120 µm width is tolerated if less than 5 mm from component pad);
   7. Spacing between conductors: 300 µm minimum (for fine pitch 150 µm spacing is tolerated if less than 5 mm from component pad);
   8. Conductor tolerance (minimum/maximum):
      supplier's specification, ±20 % maximum;
   9. Tolerance on diameter of terminal pads:
      supplier's specification, ±20 % maximum;
   10. Minimum hole diameter:
      (a) Component hole: in conformance with ECSS-Q-ST-70-08;
      (b) Via hole: 0,25 mm minimum
      and maximum aspect ratio t/d = 6;
   11. Tolerance on diameter of plated-through holes:
      (a) Nominal $\varnothing \geq 0{,}7$ mm:
      Δ maximum 0,15 mm for component hole;
      (b) Nominal $\varnothing < 0{,}7$ mm: Δ maximum 0,20 mm;

12. Tolerance on diameter of non-plated-through holes:
Δ maximum 0,20 mm;

13. Positioning tolerance of holes with respect to reference mark: ±0,1 mm;

14. Relative misregistration pad/hole: ≤ 0,15 mm;

15. Misalignment determined by measuring minimum annular ring:

(a) Solder side: 0,20 mm;

(b) Component side (reduced pads): 0,10 mm;

(c) Non-soldering hole: 0,10 mm.

c. The limits for the electrolytic coatings shall be as follows:

1. Electrolytic copper plating:

(a) Minimum purity: 99,5 %;

(b) Thickness of surface pattern: ≥ 25 µm;

(c) Thickness of plated-through holes: ≥ 25 µm;

(d) Thickness of via holes: ≥ 20 µm;

2. Tin lead plating after reflow:

(a) Tin content of alloy: (63 ± 8) %;

(b) Thickness on surface: 8 µm in highest part;

(c) Thickness in plated-through holes: 8 µm in highest part (minimum half height of hole wall);

(d) Thickness on corner angle: 2 µm;

3. Electrolytic gold plating:

(a) Minimum purity: 99,8 % (not more than 0,2 % silver);

(b) Thickness on nickel: (4 ± 3) µm;

(c) Thickness on copper: (5 ± 2) µm;

4. Electrolytic nickel plating:

(a) Thickness: 2 µm to 10 µm.

NOTE It is optional under gold.

d. The limits for the mechanical characteristics shall be as follows:

1. Warp and twist:
≤ 1,1 % for board thickness ≥ 1,6 mm,
≤ 1,5 % for board thickness < 1,6 mm;

2. Conductor adhesion/peel strength:

(a) On epoxy: ≥ 16 N/cm;

(b) On polyimide: ≥ 12 N/cm;

3. Pull strength:

(a) For terminal pads 4 mm ∅ on epoxy: ≥ 140 N;

(b) For terminal pads 4 mm ∅ on polyimide: ≥ 80 N;

(c) For terminal pads 2 mm ∅ on epoxy: ≥ 35 N;

(d) For terminal pads 2 mm ∅ on polyimide: ≥ 20 N.

e. The limits for the electrical characteristics shall be as follows:

1. Insulation resistance:

(a) Intralayer (i.e. in the same layer): > 10^4 MΩ;

(b) Interlayer (i.e. between opposite layers): > 10^5 MΩ;

2. Withstanding voltage per mm spacing between conductors:

(a) Intralayer and interlayer: 1 000 V r.m.s;

3. Short time overload:

(a) 0,035 mm copper thickness: 7 A for 4 s;

(b) 0,070 mm copper thickness: 14 A for 4 s;

4. Long time overload, destructive current:

(a) 0,035 mm copper thickness: I ≥ 8 A;

(b) 0,070 mm copper thickness: I ≥ 16 A.

9.2 Rigid single-sided and double-sided PCBs for high frequency application

a. The base materials shall be in conformance with ECSS-Q-ST-70, IEC specifications and IPC-4101 and shall be on of the following:

1. Random-glass-reinforced PTFE resin with or without Al backing;

2. Woven-glass-reinforced PTFE resin;

3. Ceramic filled woven-glass-reinforced PTFE resin;

4. Ceramic filled PTFE resin with or without Al backing;

5. Ceramic filled cross-linked hydrocarbon/thermoset polymer;

6. Woven-glass-reinforced epoxy resin FR4;

7. Quartz filled polyimide resin.

b. The limits for the dimensional characteristics shall be as follows:

1. External dimension tolerance: ±0,2 mm;

2. Thickness tolerance: ±10 %;

3. Active board size, maximum: supplier's specification;

4. Board thickness (minimum/maximum): customer's and supplier's specification according to electrical performance;

5. Positioning tolerance between registration mark and edge of circuit: ±0,2 mm;

6. Conductor width/spacing: customer's and supplier's specification according to electrical performance;

7. Tolerance on conductor (minimum/maximum): supplier's specification;
8. Tolerance on diameter of terminal pads: customer's and supplier's specification according to electrical performance;
9. Minimum hole diameter:
   (a) Component hole: in conformance with ECSS-Q-ST-70-08;
   (b) Via hole: 0,25 mm minimum
   and maximum aspect ratio t/d = 6;
10. Tolerance on diameter of plated-through holes:
   (a) Nominal ∅ ≥ 0,7: Δ maximum 0,15 mm for component hole;
   (b) Nominal ∅ < 0,7: Δ maximum 0,20 mm;
11. Tolerance on diameter of non-plated-through holes:
Δ maximum 0,20 mm;
12. Positioning tolerance of holes with respect to reference mark: ±0,1 mm;
13. Relative misregistration pad/hole: ≤ 0,15 mm;
14. Misalignment determined by measuring minimum annular ring:
   (a) Solder side: 0,2 mm;
   (b) Component side (reduced pads): 0,1 mm;
   (c) Non-soldering hole: 0,1 mm.

c. The limits for the electrolytic coatings shall be as follows:
1. Electrolytic copper plating:
   (a) Minimum purity: 99,5 %;
   (b) Thickness of surface pattern for soldering pads: ≥ 25 µm (total thickness of basic plus electrolytic copper ≥ 40 µm);
   (c) Thickness of plated-through holes: ≥ 25 µm;
   (d) Thickness of via hole: ≥ 20 µm;
2. Tin lead plating after reflow:
   (a) Tin content of alloy: (63 ± 8) %;
   (b) Thickness on surface: ≥ 8 µm in highest part;
   (c) Thickness in plated-through holes: ≥ 8 µm in highest part (minimum half height of hole wall);
   (d) On corner angle: ≥ 2 µm;
3. Electrolytic gold plating:
   (a) Minimum purity: 99,8 %
   (b) Not containing more than 0,2 % silver;
   (c) Thickness on nickel: 1 µm to 7 µm;

4. Electrolytic nickel plating:
   (a) Thickness: 2 µm to 10 µm;

   NOTE It is optional under gold.

d. The limits for the mechanical characteristics shall be as follows:
   1. Warp and twist:
      (a) Random-glass-reinforced PTFE resin: n.a.;
      (b) Woven-glass-reinforced PTFE resin: n.a.;
      (c) Ceramic filled PTFE resin: ≤ 1,1 %;
      (d) Ceramic filled x-linked hydrocarbon/thermoset polymer: ≤ 1,1 %;
      (e) Woven-glass-reinforced epoxy resin FR4:
      ≤ 1,1 % for board thickness ≥ 1,6 mm,
      ≤ 1,5 % for board thickness < 1,6 mm;
      (f) Quartz filled polyimide:
      ≤ 1,1 % for board thickness ≥ 1,6 mm,
      ≤ 1,5 % for board thickness < 1,6 mm;
   2. Conductor adhesion/peel strength:
      (a) On PTFE reinforced/ceramic filled or non-filled: ≥ 8 N/cm;
      (b) Cross-linked hydrocarbon: ≥ 8 N/cm;
      (c) On epoxy: ≥ 16 N/cm;
      (d) On polyimide quartz: ≥ 12 N/cm;
   3. Pull strength:
      (a) For terminal pads 4 mm ∅ on PTFE reinforced/ceramic filled or non-filled: ≥ 60 N;
      (b) For terminal pads 4 mm ∅ cross-linked hydrocarbon: ≥ 60 N;
      (c) For terminal pads 4 mm ∅ on epoxy: ≥ 140 N;
      (d) For terminal pads 4 mm ∅ on polyimide quartz: ≥ 60 N;
      (e) For terminal pads 2 mm ∅ on PTFE reinforced /ceramic filled or non-filled: ≥ 12 N;
      (f) For terminal pads 2 mm ∅ cross-linked hydrocarbon: ≥ 12 N;
      (g) For terminal pads 2 mm ∅ on epoxy: ≥ 35 N;
      (h) For terminal pads 2 mm ∅ on polyimide quartz: ≥ 20 N.

e. The limits for the electrical characteristics shall be as follows:
   1. Insulation resistance:
      (a) Intralayer: > 10^4 MΩ;
      (b) Interlayer: > 10^5 MΩ;

2. Withstanding voltage per mm spacing between conductors:
   (a) Intralayer and interlayer: 1 000 V r.m.s.;
3. Short time overload:
   (a) 0,009 mm copper thickness: n.a.;
   (b) 0,017 mm copper thickness: n.a.;
   (c) 0,035 mm copper thickness: 7 A for 4 s;
   (d) 0,070 mm copper thickness: 14 A for 4 s;
4. Long time overload, destructive current:
   (a) 0,009 mm copper thickness: n.a.;
   (b) 0,017 mm copper thickness: n.a.;
   (c) 0,035 mm copper thickness: $I \geq 8$ A;
   (d) 0,070 mm copper thickness: $I \geq 16$ A;
5. Permittivity: customer's and supplier's specification according to electrical performance;
6. Loss angle Tg δ: customer's and supplier's specification according to electrical performance.

9.3 Flexible PCBs

a. The base materials shall be in conformance with ECSS-Q-ST-70, IEC specifications and IPC-4101 and shall be the following:
   1. Flexible copper-clad polyimide film.

b. The limits for the dimensional characteristics shall be as follows:
   1. External dimension tolerance: ±0,4 mm;
   2. Thickness tolerance: ±20 %;
   3. Active board size, maximum: supplier's specification;
   4. Board thickness maximum: 0,4 mm;
   5. Positioning between registration mark and edge of circuit: ±0,4 mm;
   6. Conductor width/spacing: (250 µm/250 µm) minimum;
   7. Conductor tolerance (minimum/maximum): supplier's specification;
   8. Tolerance on diameter of terminal pads: supplier's specification;
   9. Minimum diameter of plated-through holes: 0,25 mm;
   10. Tolerance on diameter of plated-through holes for components:
      (a) Nominal $\varnothing \geq 0{,}7$: Δ maximum 0,15 mm;
      (b) Nominal $\varnothing < 0{,}7$: Δ maximum 0,20 mm;

11. Tolerance on diameter of non-plated-through holes: Δ maximum 0,20 mm;
12. Positioning of holes with respect to reference mark: ±0,10 mm;
13. Relative misregistration pad/hole: ±0,15 mm;
14. Registration of sides: ±0,10 mm;
15. Cutting of insulation coating tolerance:
    (a) Internal cutting: ±0,50 mm;
16. Misalignment determined by measuring minimum annular ring:
    (a) Solder side: 0,25 mm;
    (b) Reduced terminal pads (oblong): 0,10 mm;
    (c) Non-soldering holes: 0,10 mm;
17. Misalignment of insulation coating determined by measuring rest of metal:
    (a) Plated-through holes: 0,15 mm;
    (b) Non-plated-through holes: 0,25 mm;
18. Number of layers: 2.

c. The limits for the electrolytic coatings shall be as follows:
    1. Electrolytic copper plating:
        (a) Minimum purity: 99,5 %;
        (b) Thickness of surface pattern: ≥ 25 µm;
        (c) Thickness of plated-through holes: ≥ 25 µm;
    2. Tin lead plating after reflow:
        (a) Tin content of alloy: (63 ± 8) %;
        (b) Thickness on surface: ≥ 8 µm in highest part;
        (c) Thickness in plated-through holes: ≥ 8 µm in highest part (minimum half height of hole wall);
        (d) On corner angle: ≥ 2 µm.

d. The limits for the mechanical characteristics shall be as follows:
    1. Conductor adhesion/peel strength: ≥ 10 N/cm;
    2. Pull strength:
        (a) For terminal pads 4 mm ∅: ≥ 60 N;
        (b) For terminal pads 2 mm ∅: ≥ 12 N;
    3. Resistance to bending cycles: ≥ 250 cycles;
    4. Bending test for rigid-flex boards: ≥ 25 cycles.

e. The limits for the electrical characteristics shall be as follows:
    1. Insulation resistance:
        (a) Intralayer: ≥ 10^4 MΩ;

(b) Interlayer: ≥ 10^5 MΩ;

(c) With temperature at 80 °C: ≥ 10^2 MΩ;

2. Withstanding voltage per mm spacing between conductors: 1 000 V r.m.s.;

3. Short time overload: 7 A for 4 s;

4. Long time overload, destructive current: ≥ 8 A.

9.4 Rigid-flex PCBs

a. The requirements for rigid-flex PCBs shall be in conformance with clause 9.3 for the flexible part and clause 9.5 for the rigid part.

b. For the construction of multilayer rigid-flex the flexible copper clad polyimide film shall be without adhesive

9.5 Rigid multilayer PCBs

a. The base materials shall be in conformance with ECSS-Q-ST-70, IEC specifications and IPC-4101 and shall be one of the following:

1. Woven-glass-reinforced epoxy resin;

2. Woven-glass-reinforced polyimide resin;

3. Woven-glass-reinforced bismaleimide/trazine modified epoxy (HTg) resin;

4. Non-woven aramide-reinforced polyimide resin.

b. The limits for the dimensional characteristics shall be as follows:

1. External dimension tolerance ±0,2 mm;

2. Thickness tolerance: ±10 %;

3. Maximum active board size: supplier's specification;

4. Maximum board thickness: 3,2 mm;

5. Positioning between registration mark and edge of circuit: ±0,2 mm;

6. Conductor width:

(a) Internal: 120 µm minimum;

(b) External: 200 µm minimum (for fine pitch 120 µm width is tolerated if less than 5 mm from component pad);

7. Conductor spacing:

(a) Internal: 150 µm minimum;

(b) External: 300 µm minimum (for fine pitch 150 µm spacing is tolerated if less than 5 mm from component pad);

8. Conductor tolerance (minimum/maximum): supplier's specification;

9. Tolerance on diameter of terminal pads: supplier's specification;

10. Minimum drilled hole diameter:
    (a) Component hole: in conformance with ECSS-Q-ST-70-08;
    (b) Via hole: 0,25 mm minimum
    and maximum aspect ratio t/d = 6;
11. Tolerance on diameter of plated-through holes:
    (a) Nominal ∅ ≥ 0,7: Δ maximum 0,15 mm for component hole;
    (b) Nominal ∅ < 0,7: Δ maximum 0,20 mm;
12. Tolerance on diameter of non-plated-through holes:
    Δ maximum 0,20 mm;
13. Positioning of holes with respect to reference mark: ±0,1 mm;
14. Relative misregistration pad/hole: ≤ 0,15 mm;
15. Misalignment determined by measuring minimum annular ring:
    (a) External layers: solder side: 0,20 mm
    (b) External layers: component side (reduced pads): 0,10 mm
    (c) External layers: non-soldering hole: 0,10 mm
    (d) Internal layers: 50 µm;
16. Layer to layer registration: ±100 µm;
17. Number of layers: 18 maximum.

c. The limits for the electrolytic coatings shall be as follows:
1. Electrolytic copper plating:
    (a) Minimum purity: 99,5 %;
    (b) Thickness of surface pattern: ≥ 25 µm;
    (c) Thickness of plated-through holes: ≥ 25 µm;
    (d) Thickness of via holes: ≥ 20 µm;
2. Tin lead plating after reflow:
    (a) Tin content of alloy: (63 ± 8) %;
    (b) Thickness on surface: ≥ 8 µm in highest part;
    (c) Thickness in plated-through holes: ≥ 8 µm in highest part (minimum half height of hole wall);
    (d) On corner angle: ≥ 2 µm;
3. Electrolytic gold plating:
    (a) Minimum purity: 99,8 %
    (b) Not containing more than 0,2 % silver;
    (c) Thickness on nickel: (4 ± 3) µm;
    (d) Thickness on copper: (5 ± 2) µm;
4. Electrolytic nickel plating:
    (a) Thickness: 2 µm to 10 µm;
    NOTE It is optional under gold.
5. Insulation between layers: 70 µm minimum.

d. The limits for the mechanical characteristics shall be as follows:

1. Warp and twist:
≤ 1,1 % for board thickness ≥ 1,6 mm,
≤ 1,5 % for board thickness < 1,6 mm;

2. Conductor adhesion/peel strength:
   (a) On epoxy with Tg < 160 °C: ≥ 16 N/cm;
   (b) On epoxy with Tg > 180 °C: ≥ 12 N/cm;
   (c) On polyimide: ≥ 12 N/cm;
   (d) On bismaleimide/trazine modified epoxy HTg: ≥ 12 N/cm;
   (e) Aramide/polyimide: ≥ 6 N/cm;

3. Bond strength/pull strength:
   (a) For terminal pads 4 mm ∅ on epoxy Tg < 160 °C: ≥ 140 N;
   (b) For terminal pads 4 mm ∅ on epoxy Tg > 180 °C: ≥ 80 N;
   (c) For terminal pads 4 mm ∅ on polyimide: ≥ 80 N;
   (d) For terminal pads 4 mm ∅ on bismaleimide/trazine modified epoxy HTg: ≥ 60 N;
   (e) For terminal pads 4 mm ∅ on aramide/polyimide: ≥ 60 N;
   (f) For terminal pads 2 mm ∅ on epoxy Tg < 160 °C: ≥ 35 N;
   (g) For terminal pads 2 mm ∅ on epoxy Tg > 180 °C: ≥ 20 N;
   (h) For terminal pads 2 mm ∅ on polyimide: ≥ 20 N;
   (i) For terminal pads 2 mm ∅ on bismaleimide/trazine modified epoxy HTg: ≥ 12 N;
   (j) For terminal pads 2 mm ∅ on aramide/polyimide: ≥ 12 N.

e. The limits for the electrical characteristics shall be as follows:

1. Insulation resistance:
   (a) Intralayer: > 10^4 MΩ;
   (b) Interlayer: > 10^5 MΩ;

2. Withstanding voltage per mm spacing between conductors:
   (a) Intralayer and interlayer: 1 000 V r.m.s.;

3. Short time overload:
   (a) 35 µm copper thickness: 7 A for 4 s;
   (b) 70 µm copper thickness: 14 A for 4 s;

4. Long time overload, destructive current:
   (a) 35 µm copper thickness: I ≥ 8 A;
   (b) 70 µm copper thickness: I ≥ 16 A;

5. Internal short circuit:
   (a) Insulation resistance: ≥ 10^3 MΩ.

9.6 Sequential rigid multilayer PCBs

a. The base materials shall be in conformance with ECSS-Q-ST-70, IEC specifications and IPC-4101 and shall be one of the following:

1. Woven-glass-reinforced epoxy resin;
2. Woven-glass-reinforced polyimide resin;
3. Woven-glass-reinforced bismaleimide/trazine modified epoxy (HTg) resin;
4. Non-woven-aramide-reinforced polyimide resin.

b. The limits for the dimensional characteristics shall be as follows:

1. External dimension tolerance: ±0,2 mm;
2. Thickness tolerance: ±10 %;
3. Maximum active board size: supplier's specification;
4. Maximum board thickness: 3,2 mm;
5. Positioning between registration mark and edge of circuit: Δ maximum 0,20 mm;
6. Conductor width:
   (a) Internal: 120 µm minimum;
   (b) External: 200 µm minimum (for fine pitch 120 µm width is tolerated if less than 5 mm from component pad);
7. Conductor spacing:
   (a) Internal: 150 µm minimum;
   (b) External: 300 µm minimum (for fine pitch 150 µm spacing is tolerated if less than 5 mm from component pad);
8. Conductor tolerance (minimum/maximum): supplier's specification;
9. Tolerance on diameter of terminal pads: supplier's specification;
10. Minimum drilled hole diameter:
    (a) Component hole: in conformance with ECSS-Q-ST-70-08;
    (b) Via hole: 0,25 mm minimum and maximum aspect ratio t/d = 6;
    (c) Buried via: supplier's specification and maximum aspect ratio t/d = 6;
    (d) Blind via produced sequentially: supplier's specification and maximum aspect ratio t/d = 6;
11. Tolerance on diameter of plated-through holes:
    (a) Nominal ∅ ≥ 0,7: Δ maximum 0,15 mm for component hole;
    (b) Nominal ∅ < 0,7: Δ maximum 0,20 mm;
12. Tolerance on diameter of non-plated-through holes: Δ maximum 0,20 mm;

13. Positioning of holes with respect to reference mark: ±0,10 mm;
14. Relative misregistration pad/hole: ≤ 0,15 mm;
15. Misalignment determined by measuring minimum annular ring:
    (a) External layers: solder side: 0,20 mm;
    (b) External layers: component side (reduced pads): 0,10 mm;
    (c) External layers: non-soldering hole: 0,10 mm;
    (d) Internal layers: 0,05 mm;
16. Layer to layer registration: ±100 µm;
17. Number of layers: 18 maximum.

c. The limits for the electrolytic coatings shall be as follows:

1. Electrolytic copper plating:
    (a) Minimum purity: 99,5 %;
    (b) Thickness of surface pattern: ≥ 25 µm;
    (c) Thickness of plated-through holes: ≥ 25 µm;
    (d) Thickness of via holes: ≥ 20 µm;
    (e) Thickness of buried via holes: ≥ 18 µm;
    (f) Thickness of blind via holes: ≥ 18 µm;
2. Tin lead plating after reflow:
    (a) Tin content of alloy: (63 ± 8) %;
    (b) Thickness on surface: ≥ 8 µm in highest part;
    (c) Thickness in plated-through holes: ≥ 8 µm highest part (minimum half height of hole wall);
    (d) On corner angle: ≥ 2 µm;
3. Electrolytic gold plating:
    (a) Minimum purity: 99,8 %
    (b) Not containing more than 0,2 % silver;
    (c) Thickness on nickel: (4 ± 3) µm;
    (d) Thickness on copper: (5 ± 2) µm;
4. Electrolytic nickel plating:
    (a) Thickness: 2 µm to 10 µm;

    NOTE It is optional under gold.
5. Resin fill in buried vias: see 7.3.4.3.3h;
6. Insulation between layers: 70 µm minimum.

d. The limits for the mechanical characteristics shall be as follows:

1. Warp and twist:
    ≤ 1,1 % for board thickness ≥ 1,6 mm,
    ≤ 1,5 % for board thickness < 1,6 mm;

2. Conductor adhesion/peel strength:
   (a) On epoxy with Tg < 160 °C: ≥ 16 N/cm;
   (b) On epoxy with Tg > 180 °C: ≥ 12 N/cm;
   (c) On polyimide: ≥ 12 N/cm;
   (d) On bismaleimide/trazine modified epoxy HTg: ≥ 12 N/cm;
   (e) Aramide/polyimide: ≥ 6 N/cm;
3. Bond strength/pull strength:
   (a) For terminal pads 4 mm ∅ on epoxy Tg < 160 °C: ≥ 140 N;
   (b) For terminal pads 4 mm ∅ on epoxy Tg > 180 °C: ≥ 80 N;
   (c) For terminal pads 4 mm ∅ on polyimide: ≥ 80 N;
   (d) For terminal pads 4 mm ∅ on bismaleimide/trazine modified epoxy HTg: ≥ 60 N;
   (e) For terminal pads 4 mm ∅ on aramide/polyimide: ≥ 60 N;
   (f) For terminal pads 2 mm ∅ on epoxy Tg < 160 °C: ≥ 35 N;
   (g) For terminal pads 2 mm ∅ on epoxy Tg > 180 °C: ≥ 20 N;
   (h) For terminal pads 2 mm ∅ on polyimide: ≥ 20 N;
   (i) For terminal pads 2 mm ∅ on bismaleimide/trazine modified epoxy HTg: ≥ 12 N;
   (j) For terminal pads 2 mm ∅ aramide/polyimide: ≥ 12 N.

e. The limits for the electrical characteristics shall be as follows:
1. Insulation resistance:
   (a) Intralayer: > 10^4 MΩ;
   (b) Interlayer: > 10^5 MΩ;
2. Withstanding voltage per mm spacing between conductors:
   (a) Intralayer and interlayer: 1 000 V r.m.s.;
3. Short time overload:
   (a) 0,035 mm copper thickness: 7 A for 4 s;
   (b) 0,070 mm copper thickness: 14 A for 4 s;
4. Long time overload, destructive current:
   (a) 0,035 mm copper thickness: I ≥ 8 A;
   (b) 0,070 mm copper thickness: I ≥ 16 A;
5. Internal short circuit:
   (a) Insulation resistance: ≥ 10^3 MΩ.

Annex A (normative)
Evaluation test report – DRD

A.1 DRD identification

A.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-10, requirements 5.3d and 8.2b.3.

A.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the evaluation test report.

A.2 Expected response

A.2.1 Scope and content

<1> Description and history of sample

a. The report shall contain the description and history of the sample.

<2> Visual inspection parameters

a. The report shall contain the visual inspection parameters.

<3> Test condition

a. The report shall contain the measurements of the atmospheric conditions (room temperature, relative humidity and atmospheric pressure).

<4> Results of the evaluation test

a. The report shall contain the results of the evaluation test.

<5> Microsection

a. The report shall contain the results of the measurements on the microsection.

A.2.2 Special remarks

The evaluation tests are a subset of the qualification tests. The example test report in Figure A-1 can be used.

METALLIC MATERIALS AND PROCESSES SECTION — **MATERIAUX & PROCEDES METALLURGIQUES**

METALLURGICAL INSPECTION OF PRINTED CIRCUIT BOARD REPORT No:

Description and History of Sample:

Project and Cost Code:

date: **Originator:** **Telephone:**

VISUAL INSPECTION PARAMETERS. MINOR DEFECTS (m) AND MAJOR DEFECTS (M) ARE CIRCLED IF FOUND

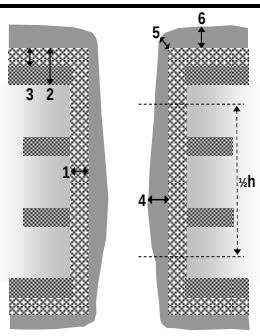
1.	**CONDUCTIVE PATTERN**	
1.1	SHORT CIRCUITS	M
1.4	SCRATCHES EXPOSING COPPER PLATING	M
1.5	SUPERFICIAL SCRATCHES	m
1.7	DEWETTING ON SOLDERABLE ZONES	M
1.8	DEWETTING ON EDGES OF MASS ZONES	m
1.9	UNDERCUT EXCEEDING 0.025 mm PER EDGE	M
2.	**BASE LAMINATE**	
2.1	EMBEDDED FOREIGN PARTICLE	M
2.2	DELAMINATION	M
2.3	CRACKS VISIBLE TO NAKED EYE	M
2.4	PITS AND DENTS	M
2.5	CHIPPING	M
3.	**HOLES**	
3.1	OPEN CIRCUITS, CRACKS	M
3.2	HOLE POSITIONS ± 0.01 mm	
3.3	ECCENTRICITY	m
3.4	DIRT, NOT REMOVABLE	M
4.	**MARKING DEFECTS**	
4.1	IDENTIFICATION IMPOSSIBLE	M

REMARKS:

-
-
-

OK / m / M

5. Annular ring internal layer (≥ 50 µm)	**OK / M**
6. Peel strength (≥ xx N/cm)	N/cm
7. Contamination (≤ 1.56 µg/cm^2)	µg/cm^2
8. Board thickness over laminate (±0.2 mm, ≤ 3.2 mm)	mm
9. Solderability	**OK / M**
10a. Rework simulation on PTH	**OK / M**
10b. Rework simulation on SMD pad	**OK / M**
11. Solder bath floating test	**OK / M**
12. Microsection mount numbers	



	REQUIRED	MEASURED	REMARKS
1. Cu in PTH	**≥ 25 µm**		**OK / M**
2. Total Cu on surface pattern	**≥ 40 µm**		**OK / M**
3. Plated Cu on surface pattern	**≥ 25 µm**		**OK / M**
4. SnPb on PTH wall	**≥ 8 µm**		**OK / M**
5. SnPb on corner	**≥ 2 µm**		**OK / M**
6. SnPb on surface	**≥ 8 µm**		**OK / M**
7. Cu in via holes	**≥ 20 µm**		**OK / M**
8. Cu in burried and blind via	**≥ 18 µm**		**OK / M**

CONCLUSION:

INSPECTED: **APPROVED:** **DISTRIBUTION:**

DATE: **DATE:**

Figure A-1: Example of a test report

Annex B (normative)
Qualification test report – DRD

B.1 DRD identification

B.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-10, requirements 6.3c.2, 6.4e and 8.2b.3.

B.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the qualification test report.

B.2 Expected response

B.2.1 Scope and content

<1> Description and history of sample

a. The report shall contain the description and history of the sample.

<2> Visual inspection parameters

a. The report shall contain the visual inspection parameters.

<3> Test condition

a. The report shall contain the measurements of the atmospheric conditions (room temperature, relative humidity and atmospheric pressure).

<4> Qualification programme

a. The report shall contain the results of the qualification programme.

<5> Microsection

a. The report shall contain the results of the measurements on the microsection.

B.2.2 Special remarks

The example test report in Figure A-1 can be used.

Annex C (normative) PCB manufacturing/assembly process identification document (PID) – DRD

C.1 DRD identification

C.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-10, requirement 6.6b.

C.1.2 Purpose and objective

The purpose of the PID is to describe the manufacturing process of the PCB.

C.2 Expected response

C.2.1 Scope and content

<1> Process and control specifications

a. The PID shall list all the process and control specifications with number, issue number and date for the full manufacturing flow for the qualified PCBs and the limits of approval.

C.2.2 Special remarks

None.

Annex D (normative)
Qualification status report – DRD

D.1 DRD identification

D.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-10, requirement 6.7b.1.

D.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the qualification status report.

D.2 Expected response

D.2.1 Scope and content

<1> Change report

a. The report shall contain the list of changes, if any, in manufacturing equipment and processes or materials used, in particular:

   1. Change of base materials.
   2. Change of chemical products.
   3. Change of process sequence.
   4. Change in process parameters.
   5. Change of equipment.

<2> PCBs

a. The report shall contain the list of PCBs supplied to this specification by the above mentioned plant during the last 24 months.

b. The evaluation test report of the delivered PCB shall be in conformance with Annex A.

D.2.2 Special remarks

None.

Annex E (informative)
Example of check-list

Figure E-1 shows an example that can be used as a check-list for double sided and multilayer PCBs.

Materials and Processes Division **Metallic Materials and Processes Section**	**Division Matériaux et Procédés** **Section Matériaux & Procédés Métalliques**

Check-list for double sided and multilayer printed circuit board fabrication facilities

Full name of company:	
Address of company:	
Town:	
Country:	
Phone:	
Fax:	
Full name of company:	
Address of company:	
Town:	

Date(s) of audit	
Name of auditor(s)	**Signature of auditor(s)**

Figure E-1: Example of Check-list for double sided and multilayer PCBs

(Part 1 of 3)

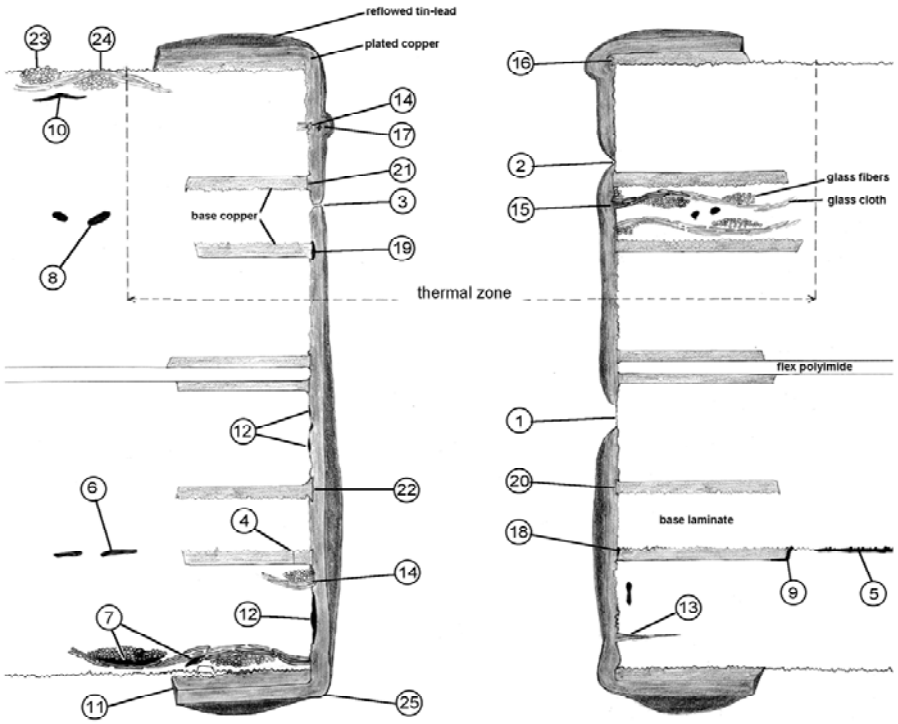
Check-list for double and multilayer printed circuit board fabrication facilities		
Process or inspection step	**Presented in documentation**	**Details and remarks**
1. Incoming inspection of laminates • Peel strength • Visual criteria • Solderability • Etchability • Warp and twist		
2. Prepreg controls (MLB) • Gel time • Resin flow • Resin content • Volatile content		
3. Inspection of artwork • Touch up • Control		
4. Photo-resist • Cleaning • Application • Exposure • Development		
5. Inspection		
6. Etching process		
7. Resist stripping process		
8. Inspect etching		
9. Pre-lamination cleaning (MLB)		
10. Cutting and laying of prepreg (MLB)		
11. Inspect pre-lamination (MLB)		
12. Laminate process (MLB)		
13. Inspect drill tools		
14. Drilling and cleaning		

Figure E-1: Example of Check-list for double sided and multilayer PCBs
(Part 2 of 3)

15. Inspect end item		
16. Etchback (MLB) – Desmear		
17. Inspect etchback		
18. Electroless copper plating and bath control		
19. Copper plate and bath control		
20. Microsection/Inspection		
21. Tin-lead plating and bath control		
22. Microsection and controls		
23. Additional platings Ni, Au, Rh, and controls		
24. Tin-lead fusing operation		
25. Routing of PCBs		
26. Final microsection		
27. Inspect end item		
28. Clean periodic test for ionic contamination		
29. Packaging		
30. Other comments		

Figure E-1: Example of Check-list for double sided and multilayer PCBs
(Part 3 of 3)

Annex F (informative)
Example of plated-through hole microsection



Cross section of a flex-rigid multilayer plated-through hole with typical features and defects

1 - plating void
2 - pinhole
3 - plating crack
4 - basic copper crack
5 - delamination
6 - delamination
7 - measling
8 - laminate void (out of thermal zone)
9 - resin recession innerlayer
10 - resin crack
11 - lifted land
12 – pull away
13 - wicking (copper)
14 - glass fibre protrusion
15 - rough drilling and wicking (copper)
16 - burr
17 - plating nodule
18 - smearing
19 - adhesion defect
20 - positive etch back (inner layer copper imbedded in plated copper)
21 - negative etch back
22 - nailheading
23 - weave exposure (fibres visible)
24 - weave texture (glass cloth shape visible)
25 - tin lead thickness < 1μ in angles

Figure F-1: Example of plated-through hole microsection

Bibliography

ECSS-S-ST-00	ECSS system – Description, implementation and general requirements
IEC 60194 (1999-04)	Printed board design, manufacture and assembly — Terms and definitions