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PPBI for OTP FPGAs

Final Report

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1 INTRODUCTION

1.1 Scope of the Document

This document describes the information and data gathered by the FPGA PPBI WG members during October 2012 through to May 2013 to compile all relevant and pertinent data on the MEC technology antifuses, to demonstrate that the reliability weaknesses applicable and inherent to the MEC technology antifuses is not applicable to the UMC technology antifuses and to compile all relevant and pertinent PPBI data and PPBI-related data on the UMC technology antifuse to justify the removal/modification or not of post-programming burn-in on one-time programmable FPGA devices.

1.2 Applicable and Reference Documents

1.2.1 Reference Documents (RDs)

RD-1: ESA Alert – ESA Alert EA-2004-EEE-07-B released in April 2005.

RD-2: ECSS-Q-ST-60-02C – Space Product Assurance ASIC and FPGA Development.

RD-3: FPGA Policy WG Report, Reference TEC-QQ/2005/10-351, Issue 1, Revision 0.

RD-4: Microsemi Reliability Report, Revision 10, November 2012.

RD-5: JESD85 (Methods for Calculating Failure Rates in Units of FITs) Standard.

RD-6: "*Post Programming Burn-in (PPBI) for RT54SX-S and A54SX-A Actel FPGAs*" by Minal Sawant, Dan Elftmann, John McCollum, Werner van den Abeelen, Solomon Wolday and Jonathan Alexander of Actel Corporation.

RD-7: "*Lifetest of Actel AX2000 Field Programmable Gate Array*", Aerospace Report No. TOR-2013(1459)-2.

RD-8: Space product assurance "*Electrical, electronic and electromechanical (EEE) components*" ECSS-Q-ST-60C Rev.1, 6 March 2009.

RD-9: Space product assurance "*Electrical, electronic and electromechanical (EEE) components*" ECSS-Q-ST-60C Rev.2, 21 October 2013.

RD-10: "*SCSB Decisions Regarding OTP FPGA PPBI (List of Heritage OTP FPGA Types Exempted from PPBI) and Best Practices for Programming*", ESCC REP 010, Issue 1 – October 2013.

RD-11: Department of Defense Test Method Standard Microcircuits, MIL-STD-883J.

1.3 Acronyms and abbreviations

The following acronyms and abbreviations are used in this WG report:

AC	:	Alternating Current
AFM	:	Antifuse Map
AITT	:	Actel Industry Tiger Team
ASIC	:	Application Specific Integrated Circuit
ATE	:	Automatic Test Equipment
BI	:	Burn-In
BIST	:	Built In Self-Test
CAE	:	Computer Aided Engineering
CMOS	:	Complementary Metal Oxide Semiconductor
CQFP	:	Ceramic Quad Flat Package
CTB	:	Component Technology Board
DBBI	:	Dynamic Blank Burn-in
DC	:	Direct Current
DLA	:	Defense Logistics Agency
DOD	:	Department of Defense
DSP	:	Digital Signal Processing
DUT	:	Device Under Test
EAQ	:	Enhanced Antifuse Qualification
ECSS	:	European Cooperation for Space Standardisation

EEE	:	Electrical, Electronic, Electromechanical
EEPROM	:	Electronically Erasable Programmable Read Only Memory
EIT	:	Enhanced Integrity Test
ELA	:	Enhanced Lot Acceptance
EM	:	Engineering Model
EOC	:	End of Channel
EOP	:	End Of Programming
EPA	:	ESD Protected Area
ESCC	:	European Space Components Coordination
ESD	:	Electrostatic Discharge
ESA	:	European Space Agency
FIT	:	Failures In Time
FM	:	Flight Model
FPGA	:	Field Programmable Gate Array
GSFC	:	Goddard Space Flight Centre
GSTP	:	General Support Technology Programme
HSB	:	High Single-B
HTOL	:	High Temperature Operating Life
HW	:	Hardware
IC	:	Integrated Circuit
JPL	:	Jet Propulsion Laboratory
LED	:	Light Emitting Diode
LTOL	:	Low Temperature Operating Life
LTPD	:	Lot Tolerance Percent Defective
LVGOX	:	Low Voltage Gate Oxide
M2M	:	Metal-To-Metal
MER	:	Mars Exploration Rover
MRO	:	Mars Reconnaissance Orbiter
MTTF	:	Mean Time to Failure
NASA	:	National Aeronautics and Space Administration

ONO	:	Oxide, Nitride, Oxide
OTP	:	One-Time Programmable
PAD	:	Parts Approval Document
PCB	:	Printed Circuit Board
PCN	:	Product Change Notification
PGA	:	Programmable Gate Array
PPBI	:	Post-Programming Burn-In
PROM	:	Programmable Read Only Memory
QA	:	Quality Assurance
QCI	:	Quality Conformance Inspections
QMS	:	Quality Management System
RAM	:	Random Access Memory
RD	:	Reference Document
RT	:	Radiation Tolerant
SBBI	:	Static Blank Burn-In
SEM	:	Scanning Electron Microscope
SEU	:	Single Event Upset
SMD	:	Standard Microcircuit Drawing
SRAM	:	Static Random Access Memory
SW	:	Software
TA	:	Technical Authority
TAS	:	Thales Alenia Space
TD	:	Technology Development
TM	:	Test Method
TOR	:	Terms Of Reference
TTL	:	Transistor-Transistor Logic
UMC	:	United Microelectronics Corporation
UPS	:	Uninterruptible Power Supply
VLSI	:	Very Large Scale IC
WG	:	Working Group

2 EXECUTIVE SUMMARY

The FPGA Policy Working Group (WG) has performed the tasks requested of it as defined in its Terms of Reference. These tasks were to:

1. Compile all relevant and pertinent historical information and data on the MEC technology antifuses highlighted in RD-1 released in April 2005.
2. Demonstrate that the reliability weaknesses applicable and inherent to the MEC technology antifuses is not applicable to the UMC technology antifuses.
3. Compile all relevant and pertinent PPBI data and PPBI-related data on the UMC technology antifuse to justify the removal/modification or not of post-programming burn-in on one-time programmable FPGA devices.
4. Review and consider previous studies and analysis available on the topic.
5. Propose an alternative to burn-in after programming, if and where applicable, in a manner that ensures the high level of assurance and quality control of one-time programmable FPGA devices.

FPGAs have been progressively introduced in space applications for the past number of years. Initially forbidden for use in mission critical applications, FPGAs have become for many space companies a viable alternative to other forms of system implementation including ASICs and are now frequently proposed for critical applications.

Antifuse based FPGAs from the US supplier Microsemi (formerly Actel) have been the preferred choice for space applications. It is expected that this trend continue to be the case in the near future. Although the review group findings are primarily based on Microsemi devices, these are independent of the antifuse technology itself and are similarly applicable to other US-FPGA suppliers. There is currently no European source for space qualified one-time programamble (OTP) FPGA devices.

In designing a testing and screening program, the driving issue is the reliability goal for a program in general and the FPGAs in particular. What increase in reliability of a device as a result of the proposed additional testing is needed and expected? Will the proposed testing and screening regime demonstrate the increased level of reliability and is the regime well designed? The majority of advocates of extensive third-party testing do not have quantitative or analytical answers to these questions. The up-screening is “justified” by a “that's what we have always done” or a “we want to

make it better" argument and is not based on a need for improvement or a defensible engineering analysis.

Based on the identified issues within this document, the Working Group made the following statements and conclusions:

1. The WG recognises that the Serma Technologies pseudo-static burn-in provides low test coverage & little or no activation of FPGA antifuses.
2. Microsemi already applies two categories of burn-in on all virgin blank parts, namely: static blank burn-in (SBBI) and dynamic blank burn-in (DBBI) using a high stress test design. It is noted that SBBI is applied to E-flow and V-flow/EV-flow RT FPGAs, while SBBI is not applied to B-flow RT FPGAs. DBBI is however, applied to all three screening flows.
3. From Microsemi ELA (Enhanced Lot Acceptance) testing no antifuse failures have been recorded to date.
4. From independent Aerospace Corporation testing a long-term test of the reliability of RTAX-S/SL FPGA antifuses has been performed. From RD-7 it is noted that 731 devices have been tested with 26,492,662 total devices hours and no antifuse failures were detected.
5. NASA GSFC commissioned reliability tests on RTAX250S & RTAX2000S. 164 devices were subjected to 3000 hours HTOL, 3000 hours LTOL with 984,000 total device hours and no antifuse failures were detected.
6. The full Serma Technologies PPBI data set from 2004 through to January 2013 covers 2095 Microsemi FPGAs and indicates that no electrical or functional failures have been observed on FPGAs which have been submitted to burn-in.
7. However, it is noted from the Serma Technologies & TAS data sets that a number of electrical parametric fails have been observed during the PPBI flow after electrical testing but always prior to the burn-in.
8. TAS highlights that a very strong improvement has been observed since migrating from the MEC technologies (global PPBI reject rate of 4.7%) to the UMC technologies (global PPBI reject 0.4%). The reject rate has decreased by an order of magnitude since switching to the UMC foundry.
9. TESAT Spacecom has detected no burn-in fails on 141 devices covering 20 designs over 6 Microsemi device types.
10. Thales CS detected 1 device fail prior to burn-in and no burn-in fails on 110 devices tested.

Based on the above conclusions, the FPGA PPBI WG recommendations were as follows:

1. To remove the post-programming burn-in requirement from RD-8 for UMC-based Microsemi FPGAs on technologies with a clear and defined heritage which is applicable to those part types listed in RD-10. The update of this RD-8 ECSS standard was published on October 21st, 2013 as RD-9.
2. For all Classes of UMC-based Microsemi FPGA components, PPBI shall remain mandatory in the case of a new family, a new technology, or major process, mask or foundry changes.
3. Agreement and consensus that the programming aspects for OTP Microsemi FPGAs shall need to be better documented. To this end RD-10 includes (although not necessarily limited to) some programming best practices for OTP Microsemi FPGAs.
4. To update RD-8 detailing that the programming software to be used should be the latest "qualified" software version with life-test/lot acceptance test data and not necessarily the latest version released by Microsemi. This has been captured in Section s 4.6.4f, 5.6.4f and 6.6.4f of RD-9.
5. Microsemi shall be actioned to not recommend the latest programming software version for space users but instead shall recommend the latest "qualified" software version with life-test/lot acceptance test data (as per the previous bullet).
6. No agreement or consensus was reached on whether or not to perform electrical testing after programming. As a result RD-8 has not been changed in this regard where it is now stated in RD-9 that the supplier shall prepare a post-programming procedure for customer's approval, depending on part types (including when necessary electrical tests, programming conditions and equipment, programming software version qualified by the supplier, burn-in conditions, additional screening tests and specific marking after programming).

   Each individual stakeholder feedback on electrical testing post-programming can be summarised as follows:

a): Alter Technology Position on Electrical Testing Post-Programming

- 3 temperature electrical testing post-programming shall be mandatory at component-level.
- This testing shall verify the programmed FPGA based on the manufacturer's electrical specification.
- It could also potentially identify basic design rule violations.
- It will put antifuse FPGAs at the same position of others devices such as SRAM-based and Flash-based FPGAs.

b): Astrium Position on Electrical Testing Post-Programming

- No specific test required to be performed at part-level.
- Final device acceptance shall be done by test, either at board or equipment level.
- Based on a purely industrial risk trade-off on a project basis, additional tests may be performed.

c): TAS Position on Electrical Testing Post-Programming

- Parametric measurements according to Table I of the SMD (at 3 temperatures, with supply voltage combinations, Read & Record) shall be performed as a quality health check at part-level.
- Functional test is a programmatic rather than a quality driven test. As a result, functional testing can be an industrial choice to perform it a board or equipment-level.

d): CNES Position on Electrical Testing Post-Programming

- Electrical parametric testing at part-level over 3 temperatures & 3 supply voltages and I(V) characterisation of all I/Os shall be performed. These tests shall verify the good health of the part after programming.
- Functional test at component-level must be considered for critical designs (high gates complexity, high frequency…). This test shall verify sufficient margins on design critical timings. However, its relevance shall be assessed during the project risk mitigation.
- Functional tests shall be performed at board-level. All mission functionalities and operating modes shall be tested over the full qualification temperature range.

e): DLR Position on Electrical Testing Post-Programming

- Recommendation from DLR for independent programming verification is to perform this at application-level and not with a dedicated component test procedure at part-level.
- This approach is considered acceptable only if the confidence level on correct programming is high.

f): ESA Position on Electrical Testing Post-Programming

- 3 temperature electrical parametric testing of programmed FPGA devices prior to mounting of parts at board-level should be maintained. ESA considers electrical parametric testing a necessary part-level health check prior to assembly.
- Functional testing of devices and final device acceptance can be performed at board-level.

A non-exhaustive list of advantages and disadvantages of component-level parametric testing versus application-level testing, looks as follows:

Component-Level Parametric Testing : Pros & Cons

Pros	Cons
i. Tests verify the programmed FPGA versus the manufacturer's electrical specification. ii. Tests can include worst case conditions. iii. Tests can be independent of the design. iv. Complete parametric measurements can be performed including characterisation of I/Os. v. Good health check of the device directly after programming can mean early detection of issues.	vi. Extra manipulation of FPGA devices increases the risk of failure from ESD or handling. vii. The test coverage can be considered quite low. viii. Testing does not verify the programming as it's not possible to read back antifuses. ix. The test conditions are not necessarily at full operating frequency. x. The flight functions are tested only at board-level.

Application-Level Testing : Pros & Cons

Pros	Cons
i. Low manipulation of FPGA devices and so reduced risk of failure from ESD or handling. ii. Lower cost. iii. Faster project schedules as all post-programming component-level testing is eliminated. iv. Board-level testing is at full operating frequency, under application conditions and a realistic environment.	v. Tests will not include worst case conditions. vi. No parametric testing of I/Os. vii. The flight functions are tested only at board-level. **viii.** Detection of issues is very late instead of detection at component-level.

7. As no consensus for post-programming electrical testing at component-level could be reached within the FPGA PPBI WG, the Q60 Working Group decided to leave the RD-8 text with respect to electrical testing as is.

3 WOKRING GROUP ACTIVITIES

The various members of the FPGA PPBI WG were as follows:

Title	Name	Company
Chairman	Ken HERNAN	ESA
Member	Joel LE MAUFF	Alter Technology
Member	Vincent LESTIENNE	Astrium
Member	David DANGLA	CNES
Member	Jerome CARRON	CNES
Member	Volker LUECK	DLR
Member	Ralf DE MARINO	ESA
Member	John MCCOLLUM	Microsemi
Member	Ken O'NEILL	Microsemi
Member	Maxence LEVEQUE	Serma Technologies
Member	Michel CARQUET	TAS-F
Member	Aurelien JANVRESSE	Thales TCS

FPGA PPBI WG teleconference calls were organised between Q4 2012 and Q4 2013 on the following dates & times:

Meeting #	Date	Time
1	October 2nd 2012	4:00 P.M. (C.E.T.)
2	October 22nd 2012	4:00 P.M. (C.E.T.)
3	November 13th 2012	4:00 P.M. (C.E.T.)
4	December 6th 2012	4:00 P.M. (C.E.T.)
5	January 24th 2013	4:00 P.M. (C.E.T.)

6	February 19th 2013	4:00 P.M. (C.E.T.)
7	March 5th 2013	4:00 P.M. (C.E.T.)
8	April 11th 2013	4:00 P.M. (C.E.T.)
9	May 23rd 2013	4:00 P.M. (C.E.T.)
10	June 24th 2013	4:00 P.M. (C.E.T.)
11	December 3rd, 2013	4:00 P.M. (C.E.T.)

4 BACKGROUND

4.1 Use of FPGAs in Space Applications

Different types of Field Programmable Gate Arrays (FPGA) are on the market. One of the main distinctions between these types is the programming element used. Antifuses are used in one-time programmable (OTP) FPGAs and require dedicated hardware and software for programming prior to their assembly in the intended application board. Antifuses are manufactured with high ohmic interconnections and are programmed by applying an external high voltage creating a breakdown in the antifuse insulation area and thereby transforming it into a low resistance path. This physical alteration of a large number of antifuses to create the application specific device configuration is irreversible and although it is performed by the user it is considered to be a final production step.

SRAM or EEPROM type memory cells are used for (in system) re-programmable FPGAs. For commercial applications SRAM based device types dominate in spite of the fact that they require a non-volatile memory component (e.g. PROM) to boot the FPGA configuration memory on power-up. The reason for this preference is the higher performance and flexibility provided by SRAM memory compared to other memory types.

For SRAM based FPGAs there continues to be considerable concern with respect to the SEU sensitivity of the configuration memory, where radiation induced bit-flips can cause a change in functionality of the device. This technical weakness, along with concerns around the lack of experience and effective QA controls in dealing with in system programmable components have slowed down the widespread adoption of SRAM based FPGAs in space applications. However, for a number of years Xilinx, worldwide the biggest commercial FPGA producer (also fab-less) is more

aggressively marketing its products to space users with more notable success among non-European space companies.

For all FPGAs as for ASICs, RD-2 defines the requirements for the design of user applications (not to be confused with the ASIC technology development or generic FPGA design performed by the foundry or vendor). This standard specifies all requirements pertaining to the planning and execution of the development activity including quality assurance and documentation up to and including the validation of prototypes.

The history of FPGA application experience (which mainly encompasses antifuse based device types from Actel) has shown that there are some inherent, but possibly unavoidable weaknesses in the formulation of generic microcircuit requirements in ECSS and ESCC documents, which may lead to conflicting interpretations in the case of antifuse FPGAs. As a result, in 2005 ESA deemed it necessary to assess the situation and propose a policy for the use of FPGAs in ESA projects. The policy adopted by ESA and the recommendations proposed are described in more detail in Section 4.8.

4.2 The Antifuse: A Technical Backgrounder

Through the years, the design of digital logic circuits has evolved from working with small-scale integrated circuits (ICs) containing discrete gates to use of large-scale and very-large-scale ICs (VLS1) containing many thousands of gates. A number of commonly-used functions became available in the form of high-density circuits. Yet designers still retained the need to use small-scale ICs, even discrete gates, to solve interface problems and to implement their unique designs. The advent of the FPGA encapsulated the design flexibility provided by small-scale lCs into a high-density circuit.

The applications for FPGAs are legion. Wherever a design uses a substantial amount of small and medium-scale ICs there exists the potential for an FPGA to provide a faster, more compact, more reliable solution. FPGAs also excel in new designs, where VLSI alternatives do not exist and the cost of custom ICs is prohibitive. Where complex designs must undergo minor updates to match changing market demands, where designs must be initiated without final specifications in hand, or where production volumes are too low to amortise a custom circuit’s setup costs, FPGAs have a home. The market for FPGAs is substantial and growing. Indeed, the market has attracted a number

of vendors, each touting its architecture and technology as the best solution to the needs of logic designers.

An antifuse, as its name implies, is like a fuse in reverse. The antifuse begins as a high-impedance (essentially open) circuit element and changes to a low-impedance connection when subjected to a programming voltage. The change is irreversible and highly reliable. The array comprises horizontal rows of logic blocks alternating with channels of pre-defined interconnect tracks segmented into varying lengths. The input and output ports of each logic block connect to vertical tracks that span several logic rows and interconnect channels. The vertical and horizontal tracks are insulated from one another but at each crossover lies an antifuse. When programmed, the antifuse connects the two tracks together. Selectively programming the antifuses will create a circuit path between one logic block and another as indicated in Figure 1 below.

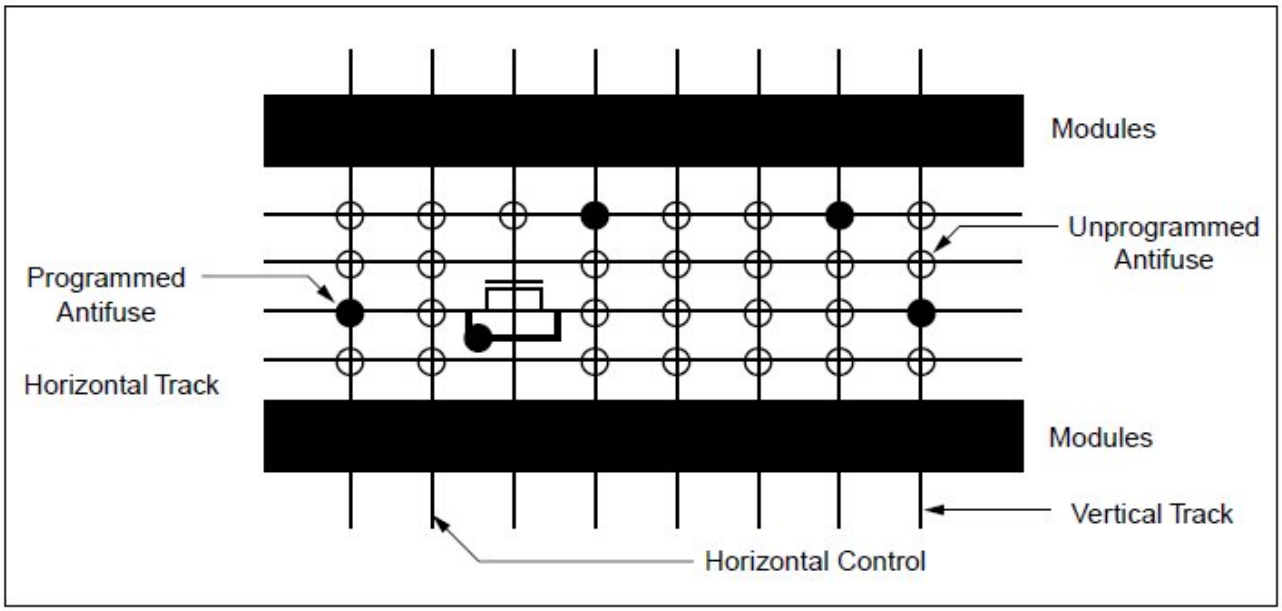


Figure 1: FPGA array architecture

The network of horizontal and vertical interconnect tracts allows arbitrary and flexible interconnections among logic blocks. All speed-critical interconnections can be accomplished programming only two antifuses. Most other connections in the design use two or three antifuses, but never more than four. The result is a device that lets designers utilise in excess of 80%, and in many applications, 100% of the available logic blocks before all available routing channels are taken. And that routing is flexible enough that CAE tools can achieve 100% automatic placement

and routing. These levels of utilisation and routability are comparable to conventional gate arrays of similar size.

The antifuses reside entirely within the interconnect channels and are smaller than the space from one track to the next. Thus, the antifuses interconnects occupy no additional die area. Further, they are small enough that improvements in process technology that shrink line spacing don't crowd the antifuses.

4.3 Antifuse vs Memory-Based Programmable Logic

When it was founded in 1985, Actel sought the best long-term solution to the needs of high-performance programmable logic. It considered a variety of alternatives, examining various antifuse structures. Actel chose to pair an antifuse interconnect scheme with a gate-array-like architecture in order to achieve the highest possible circuit density and, consequently, lowest cost on a per-gate basis.

Two kinds of gate array structures exist: channelled arrays and channel-less sea-of-gates arrays. The channelled array divides the silicon into strips of logic blocks interspersed with channels containing metal tracks. The sea-of-gates structure uses a myriad of small logic blocks (gates) that cover the silicon. In both cases a network of metal traces provides potential pathways for carrying signals to and from the logic blocks. In the channelled array, the traces within the channels can carry signals alongside the logic. A second layer of metal traces, insulated from the channels and logic blocks, can carry signals across the logic. The sea-of-gates array uses three insulated metal trace layers, two of which run at right angles and the third layer is used to connect the logic blocks. In either case a route from one logic element to another lies along a combination of traces within the two layers, but the traces aren't connected, yet.

A programmable gate array offers the user a means of selectively connecting trace segments in the two layers to form complete circuits between logic elements. The methods used to provide that connection include both memory-driven transistor switches and physical-change structures. With memory-driven interconnections, an EPROM or RAM cell provides a signal that controls a pass transistor. When turned on, the transistor provides a signal path between the trace segments it bridges. When off, it isolates the two. By programming the memory cells, the user establishes logic circuits.

Physical-change structures, on the other hand, use an interconnection element that will be physically altered during the programming process. The alteration is permanent, eliminating the need for a memory circuit. Two types of such interconnection elements are possible: the fuse and the antifuse.

The fuse is a familiar structure: a conducting metal filament that is destroyed when subjected to excessive heat or current, creating an open circuit. Fuses have been used for years as programming elements for memories and simple programmable logic. They are ill-suited to FPGAs, however, because of the many potential connections.
A fuse-based programmable gate array (PGA) would need to start out with all possible connections among the logic elements already made. The user then would remove all the unwanted connections in order to leave the pattern desired. Because a programmed gate array typically uses only 2% of its possible connections, this is rather like building a box by hollowing out a large block of wood—highly inefficient. Fuse-based PGAs can be implemented for factory programming, however, using a laser to cut the unwanted fuses.

In contrast to the fuse, the antifuse is a non-conducting circuit element that becomes conducting following application of a programming voltage and current across its terminals. Configuring an antifuse-based FPGA, therefore, requires programming only those connections that are desired, leaving the others alone. You only build the walls you need for your box.

Of all these structures, the antifuse represents the most efficient use of die area. The memory cells needed for memory-based interconnect occupy considerable silicon area. An SRAM cell, for example, needs at least 3 transistors in addition to the pass transistor for the connection. Further, the pass transistors have to be relatively large to get high performance. This multitude of large transistors occupies more space than the traces alone need. The result is either a relatively large die or limits to the number of interconnections per chip.

An antifuse structure is much more compact. Antifuses typically consist of a thin insulating layer between contact points that begins conducting under application of high voltage, typically 12–20V. Once the insulation starts conducting, the antifuse's terminals melt together and form a permanent conducting channel through the insulation. That channel is typically a tenth the size of the tracks being connected. Thus, the antifuse can occupy the space between metal traces, taking up no additional die area. This allows the antifuse to be placed at every potential connection point without affecting the die size.

The antifuse FPGA does lose some chip area because it needs on-chip high-voltage programming circuits. These circuits reside on the chip's edges, however, rather than at each interconnect junction. Thus the die area occupied by the high-voltage drive transistors does not restrict the interconnect density achievable in the rest of the chip, unlike the transistors in a memory-based FPGA. Further, as semiconductor processes scale to smaller feature sizes and allow higher gate capacity devices, the relative area occupied by the high-voltage circuits decreases.

In addition to the die area advantages, the antifuse provides a connection with lower resistance and capacitance than the pass transistors. Lower resistance and capacitance translates into smaller propagation delays, resulting in faster overall circuits.

4.4 Antifuse Technology

The antifuse concept dates back to at least 1951, when it was considered for use in memories. The basic antifuse is a thin insulating layer between conductors that gets altered (programmed) by the application of high voltage. The alteration is non-volatile, i.e., it remains after removal of the voltage. Once the change has occurred, a low-resistance path exists between the conductors. The nature of that path is determined by the type of antifuse structure used. At present, two types of antifuse are commercially produced: the amorphous silicon antifuse and dielectric antifuse.

The amorphous silicon antifuse uses a non-crystalline form of silicon between the conductors, which are typically metal. Under high voltage a section of that amorphous silicon undergoes a phase change and atoms from the metal layers it separates migrate into the silicon material. The result is a thin conducting filament composed of a complex mixture of silicon and metal. The size and resistance of the filament is dependent on the amount of programming current that flowed during its creation.

This structure has been investigated for years and has presented a number of technical hurdles. To keep within reason the programming voltage needed, the amorphous layer must be thin. Early attempts to create these thin layers either required processes too costly for high-volume production or resulted in significant thickness variation because of process equipment limitations. The consequence was a history of devices with unpredictable performance. Only in

the early 2000s has process technology been sufficiently accurate to control the amorphous silicon thickness.

A more persistent problem with some amorphous silicon antifuses has been their response to high-current pulses. The programmed antifuses sometimes revert to a high-impedance state due to cracking or a phenomenon called read disturb. The result is that the antifuse's resistance jumps, which will change the corresponding logic circuit's propagation delays and may even look to.the logic like an open-circuit. This reversion tends to be self-healing; normal logic-high voltages are sufficient to reprogram the disturbed antifuse. However, there is no guarantee that the node containing the disturbed antifuse will see a logic-high voltage again, once the change has occurred. Thus, the tendency to self-heal is not a reliable antidote. Instead, the FPGA design must limit the current flow through the antifuse to avoid stressing the filament.

The other antifuse type, the dielectric antifuse, uses oxide (glass) as the insulating layer. Application of high voltage creates multiple conducting filaments which are prone to self-healing. Actel solved that problem with its patented PLICE antifuse structure. Instead of using a single oxide layer, the PLICE antifuse uses a sandwich of oxide, nitride, and oxide (ONO). The ONO layer lies between a polysilicon conductor and a heavily-doped n+ diffusion region of the base silicon wafer. Under the programming voltage, the ONO sandwich melts and the base wafer grows an epitaxial "bump" into the polysilicon in the shape of a dome. Growth of the bump shatters the ONO layer, allowing diffusion of the substrate n+ into the polysilicon to form a low-resistance path.

The bump typically is 10x taller than the ONO layer thickness, preventing any possibility of reinstating the oxide barrier. The bump's size also makes the structure tolerant of current-induced stresses. Thus, the PLICE antifuse can safely handle much higher currents than can amorphous silicon. If anything, the high currents would increase the bump's size, strengthening the connection.

Although the PLICE antifuse uses the base silicon as part of its connection between metal layers, it does not steal any die area from the logic circuits in a channelled gate array. The PLICE structure is small enough to fit in the space between metal traces in the channel.

4.5 Evolution of Antifuse Alternatives

Low resistance and capacitance values are among the primary attributes of a good programmable connection for logic. The need for low resistance comes from its interaction with both the connection's capacitance and the parasitic capacitance that occurs in the metal interconnection network and the input structures of logic gates.

The greater the capacitance in a circuit, the more drive current the circuit requires in order to quickly shift logic states. However, the connection's resistance attenuates the drive signal, restricting the amount of current available to change logic states. The combined effect of this resistance and capacitance is to slow the propagation of electrical signals through the circuit. This slowing, in turn, limits the clock frequency the logic can use. Keeping the connection's capacitance and programmed resistance low minimizes the problem.

Comparing antifuse alternatives solely on the basis of capacitance and typical programmed resistance, however, is to take a near-sighted view. There may be other factors limiting the circuit's clock speed. One such factor is extendability, how well the antifuse structure works over a range of IC sizes. Another is scaleability, how readily the structure shrinks as process lithography improves. The key to creating a useful product is finding an optimum combination of all factors.

Consider, for example, the current-carrying capacity of an antifuse structure. Amorphous antifuses, as already described, risk being damaged by too great a current. Thus, an FPGA using amorphous antifuses must be designed to avoid current spikes. Yet current spikes are common in digital circuits. Circuit capacitance and logic switching speed determine the size of those spikes. Therefore, the amorphous-antifuse FPGA must place limits on clock edge rate based on the circuit's capacitance.

One prominent contributor to circuit capacitance is the metal interconnect track. Its capacitance is a function of its length; the longer the track, the greater the capacitance. As the array size gets larger, then, the amorphous-antifuse FPGA must either reduce circuit speed or limit track length to keep current spikes under control. Reducing circuit speed is an obvious disadvantage. Limiting track length is also a disadvantage, however, because it reduces the user's ability to fully utilize the available gates. Gates widely separated cannot be used in the same circuit.

The physical layout of an antifuse can also put a limit on the FPGA's ability to scale down as semiconductor processing achieves smaller circuit sizes. A via-type antifuse for example, typically used with amorphous silicon, runs into problems at smaller geometries. To create a repeatable antifuse, the fabrication process must lay down a uniform, controlled thickness of antifuse material. Placing material in a well, as occurs when creating a via between metal layers, results in thinning at the well's corners, as shown in Figure A-3. That thinning is difficult to control, reducing the repeatability of the antifuse layer thickness. The thinning becomes more prominent as the well gets smaller. Thus, the via structure for an antifuse is difficult to scale reliably, reducing the opportunity to benefit from process lithography improvements.

The PLICE antifuse has neither of these limits. The programmed connection is tolerant of current pulses, so is able to handle large circuits without the need to reduce clock speeds or restrict track lengths. The PLICE structure is planar, not well-like, so thinning is not prominent. The result is controlled, repeatable connection.

Another factor to consider is cost. The amorphous-silicon antifuse has the advantage that it can reside between two metal layers. Placing the antifuse between metal layers allows the FPGA to use a sea-of-gates architecture, thereby devoting most of the silicon to logic circuits rather than reserving an area for interconnect channels. The result is a smaller, therefore cheaper, device for a given gate count.

While it is possible to place a PLICE antifuse between two metal layers, the needed metal-poly-ONO-poly-metal sandwich requires too many processing steps. The added processing cost would outweigh the size-reduction savings. A channeled architecture is the most cost-effective match to the PLICE structure.

The cost advantage afforded by a sea-of-gates architecture is of no value without a reliable antifuse, however. No one cares that the designer saved a few dollars when the customers start complaining about failed equipment. Evaluating the reliability of an antifuse is an involved task. Simple burn-in tests aren't adequate; the design must pass tests that accelerate its probable failure modes. Such tests include voltage stress and temperature stress of both programmed and unprogrammed antifuses. The PLICE antifuse has proven its reliability to be less than 10 FITs

4.6 GSFC NASA Advisory

In 2004 Actel RTSX-S and SX-A FPGA devices produced in the 0.25µm MEC/Tonami process were seen to experience programmed antifuse parametric failures during controlled laboratory testing, with the number of failures significantly exceeding the expected fall out rate for parts of this class. These failures were detected in devices programmed with the old algorithm (i.e. software versions prior to DOS 3.81/Win 4.44.0) that were operated in an in-specification electrical environment. Failures were also detected in devices programmed with the "new" programming algorithm at the "P4B2" stress level. Data sets showed a decreased failure rate for devices programmed with the new programming algorithm at varying levels. As a result, Actel at that time implemented a new wafer level visual inspection so that 4 die from each wafer was examined for alignment and photoresist residue. It was considered that a significant number of failures of this class were not detectable by testing either at the part level by ATE or at the board or box level in the target system. The failure mechanism was a timing fault, and required testing that was sensitive to timing faults.

An examination test data showed a failure rate decreasing with time and accelerated by a combination of increased voltage and temperature. Back in November 2004, no programmed antifuse failures were observed on the 0.22µm SX-A, 0.22µm eX, or 0.25µm RTSX-SU FPGAs produced at the UMC foundry. These UMC-produced devices had an antifuse structure physically different from those produced in the MEC foundry. Additionally, there were other design changes at the circuit and structural levels.

An Actel Industry Tiger Team (AITT) was set up and was composed of members from the Aerospace Corporation, JPL, Northrop-Grumman, Lockheed-Martin, General Dynamics, Boeing, and NASA represented by the Office of Logic Design. Tests and analysis were performed to understand the root cause of failure and to develop screening procedures. The key finding from the AITT testing was a failure rate of over 6% for the RT54SX32S, with the devices operated within the manufacturer's specification. The conditions for these tests were relatively benign. The devices were biased with VCCA = 2.5V, which is in the midpoint of the recommended operating range, the temperature was nominal (approximately 40 ºC from self-heating in the test chamber), and there was effectively no output switching. Thus, the test conditions were less stressful than a typical flight design.

Recommendations by Actel in 2004 where that:

1. Actel MEC SX-A FPGAs should not be used in safety-critical applications. Similarly, Actel MEC RTSX-S FPGAs should not be used in manned, safety-critical applications. These two recommendations applied to both the “old” and “new” programming algorithms.
2. Current and prospective users of Actel UMC A54SX-A and the new Actel UMC RTSX-SU FPGAs were urged to follow the NASA Office of Logic Design UMC device testing progress. Actel internal testing had detected no programmed antifuse failures on these two UMC device types at the time.
3. It was recommended that projects employ the following three techniques to decrease the risks associated with the usage of Actel MEC SX-A and Actel MEC RTSX-S FPGAs:

    - ensure that test procedures have maximised fault coverage and all circuit nodes are heavily exercised.
    - maximise the number of operating pre-launch hours, in particular high temperature environmental testing.
    - ensure that all specifications, manufacturer’s guidance and good engineering practices are always followed with conservative design practices employed. In particular, logic structures that use the routed array clocks or local signals must employ skew-tolerant clocking techniques.

4.7 ESA Alert

ESA Alert EA-2004-EEE-07-B was released in April 2005 for part numbers RT54SX32S, RT54SX72S, MEC/A54SX32A, MEC/A54SX72A. The cause of these failures was seen to be a significant resistance increase of individual programmed antifuses during device operation. The failure manifested itself as an increase of the propagation delay of an internal path within the FPGA. Sudden increases by one to three orders of magnitude caused functional failures as a result of timing violations in the design. As the failure mechanism was a timing fault, it was recommended that testing be sensitive to timing faults. An examination of the test data showed a failure rate decreasing with time and which might possibly be accelerated by a combination of increased voltage and temperature. It was claimed that a significant number of failures of this class may not detectable by testing either at the part level by ATE or at the board or box level in the target system.

In May 2004 Actel introduced the new programming algorithm incorporated in the Silicon Sculptor programming SW versions DOS 3.81 / Win 4.44 through DOS 3.86.1/Win 4.49.1 (March 2005) to improve the programming conditions for high current antifuses. Extensive tests were conducted in

the US by NASA, Aerospace Corporation, Actel and other users to determine the reliability of RTSX_S FPGAs programmed with the old and new programming algorithms. Data sets showed a decreased failure rate for devices programmed with the new programming algorithm at varying levels. The validity of some of these test results were disputed by Actel because additional tests conducted on a different lot programmed with the new algorithm did not produce failures. Actel then released the modified new algorithm, implemented in the Silicon Sculptor SW release DOS v3.87/Win v4.50.0 in March 2005.

All antifuses in the RT54SX32S, RT54SX72S, MEC/A54SX32A, MEC/A54SX72A device types had the same construction, however, depending on their specific purpose Actel distinguished between antifuses subjected to high and low programming currents. The “new” programming algorithm was designed to reduce the potential of antifuse overheating on the high current antifuses during programming but did not address the low current antifuses. Subsequent independent tests performed on parts programmed with the “new” algorithm have not produced consistent results allowing a clear determination of the level of stability improvement of the high current anitfuses. The “modified new” programming algorithm changes the low current antifuse programming conditions but incorporates no further changes on the high current antifuse programming. This “modified new” algorithm requires a change of the fuse file format in a way that can only be supported by the Silicon Sculptor II programming hardware and requires the generation of fuse maps (AFM) with the Designer Software release 6.1 SP1 or later, which conforms to the new standard.

4.8 ESA FPGA Policy

In 2005 RD-3 identified the following main issues:

- The lack of visibility of the manufacturer processes (including qualification) due to ITAR restrictions.
- The weaknesses of the US QML system. Although most of them are not FPGA specific, the potential consequences for antifuse based FPGAs are more severe than for other part types.
- The lack of screening of the component after programming. The programming physically alters the component and its quality after programming cannot be assured alone by the screening on the blank part performed by the manufacturer.

The FPGA Policy WG recommended that it be the policy of ESA that:

> *The level of assurance and quality controls applied to FPGA should be equal to that applied to other types of components, particularly those that perform similar functions, such as Application Specific Integrated Circuits (ASIC). The quality controls and assurance activities should be applied in all stages of the procurement, design, programming, integration, verification and use of this class of component.*

Based on the above identified issues and considerations RD-3 made the following six recommendations:

1. *ESA should reinforce the past and existing initiatives and efforts to collect and analyse European space user field experience[1] and organise and fund a more systematic assessment programme.*

2. *ESA should continue to obtain enhanced visibility of the test structure design and the test conditions applied by the vendor (including test vectors) during the internal qualification and lot acceptance testing, and, assess if the approach is sufficiently representative for common ESA space applications.*

3. *The ESA Component Division should assess any FPGA family prior to its first use in an ESA project. The scope and extent of this assessment needs to be determined according to the technologies involved and the available data. Existing funding of technologies (e.g. GSTP) should be seriously considered for these activities.*

4. *The WG recommends that PADs for all FPGAs are to be systematically submitted to ESA for approval. The PAD shall allow traceability to the information related to the procurement of blank parts, the programming and the acceptance of the programmed parts. The current ECSS-Q-60 standard should be updated accordingly.*

5. *Dynamic post–programming burn-in activities at component level shall be required for FPGA (they should be equivalent to MIL-STD-883 TM1015). The current ECSS-Q-60 standard should be updated accordingly.*

6. *ESA shall assess the capabilities of existing European organisations to perform FPGA post-programming screening and test.*

5 WORK LOGIC

5.1 Microsemi Quality Management System (QMS)

Microsemi has established and implemented quality and reliability objectives to ensure that all of its products conform to customer requirements. It is Microsemi's goal to continuously improve the quality and reliability of its operations at all levels, from market research and product design to product delivery and customer service. This is reflected in Microsemi's company-wide policies, which are geared towards continuously improving all levels of operation.

5.1.1 Microsemi Quality Certificates

Microsemi conforms to nationally and internationally recognised standards and today has a large portfolio of quality and reliability certifications. Microsemi has achieved the following certifications and registrations:

- AS9100:2009 Rev C Certificate
- Class Q and V Certification for MIL-PRF-38535 (DLA Land and Maritime)
- ISO 90001:2008 Certificate
- Laboratory Suitability for RD-11
- PURE Certificate
- Sony Green Partner Certificate
- STACK International Supplier Certification

5.1.2 Quality System

Microsemi maintains a quality system to ensure that products conform to specified requirements. Necessary equipment, controls, and processes are in place to ensure that the desired level of quality is continually achieved. Microsemi has various procedures and systems in place in order to achieve this end and which include:

- Contract review
- Document and data control
- Control of supplier and subcontractor quality
- Product identification and traceability
- Process control

- Control of inspection, testing, measuring and test equipment
- Control of non-conforming products
- Corrective and preventive action system
- Control of handling, storage, packaging, preservation and delivery
- Internal quality audit
- Training
- Servicing
- Statistical process control
- Continuous improvement process

There is no perfect quality system, and therefore, Microsemi recognises the need for on-going product and process improvements. Microsemi reassesses its quality improvement activities on a regular basis to ensure that its customers are provided with products and services that have a high level of quality and reliability.

5.1.3 Qualification Program

Qualification is a means of verifying that changes in the circuit design, the fabrication process, packaging materials, and/or assembly methods enable the product to meet the specified reliability requirements. In addition, the qualification process is a source of information on the major characteristics of new products and process technologies.

Microsemi's standard reliability qualification programs are described hereafter (refer to Figure 2), followed by explanations of significant reliability tests. Product reliability has been evaluated on Microsemi's numerous existing products. Reliability tests are classified by geometry and and have been conducted on different package types. Descriptions of each test and a summary of relevant data are provided hereafter.

New fab process technology (see Figure 3) requires three wafer diffusion lots for qualification of each wafer foundry. Products can be mixed during qualification as long as data is collected from at least one run of the product with the largest die size.

New package qualifications (see Figure 4) require three package assembly lots for qualification of each assembly site. Assembly lots can be mixed from different fab lots yielded from different fab sites as long as data that is collected for that package is based on the product with the largest

die size and highest lead count. A new package is defined as the first member of the package family for Microsemi. Ceramic package qualification is per QCI requirement, as defined in RD-11.

Any new product with a die size that is 15% (measurement per die side) greater than the qualified product within the same product/process families requires qualification on one lot. This requirement also applies to package families.

When an existing package is transferred to another assembly vendor, one lot is required for each package family (in addition to the reliability and qualification data from the original assembly vendor). Qualification must be done on the largest body size, highest lead count, and largest die size per package family.

Table 1 indicates the reliability test methods and test conditions used for the reliability tests detailed in Figures 2 to 5 inclusive. Table 2 indicates the necessary testing requirements in the case of process and design changes by Microsemi.

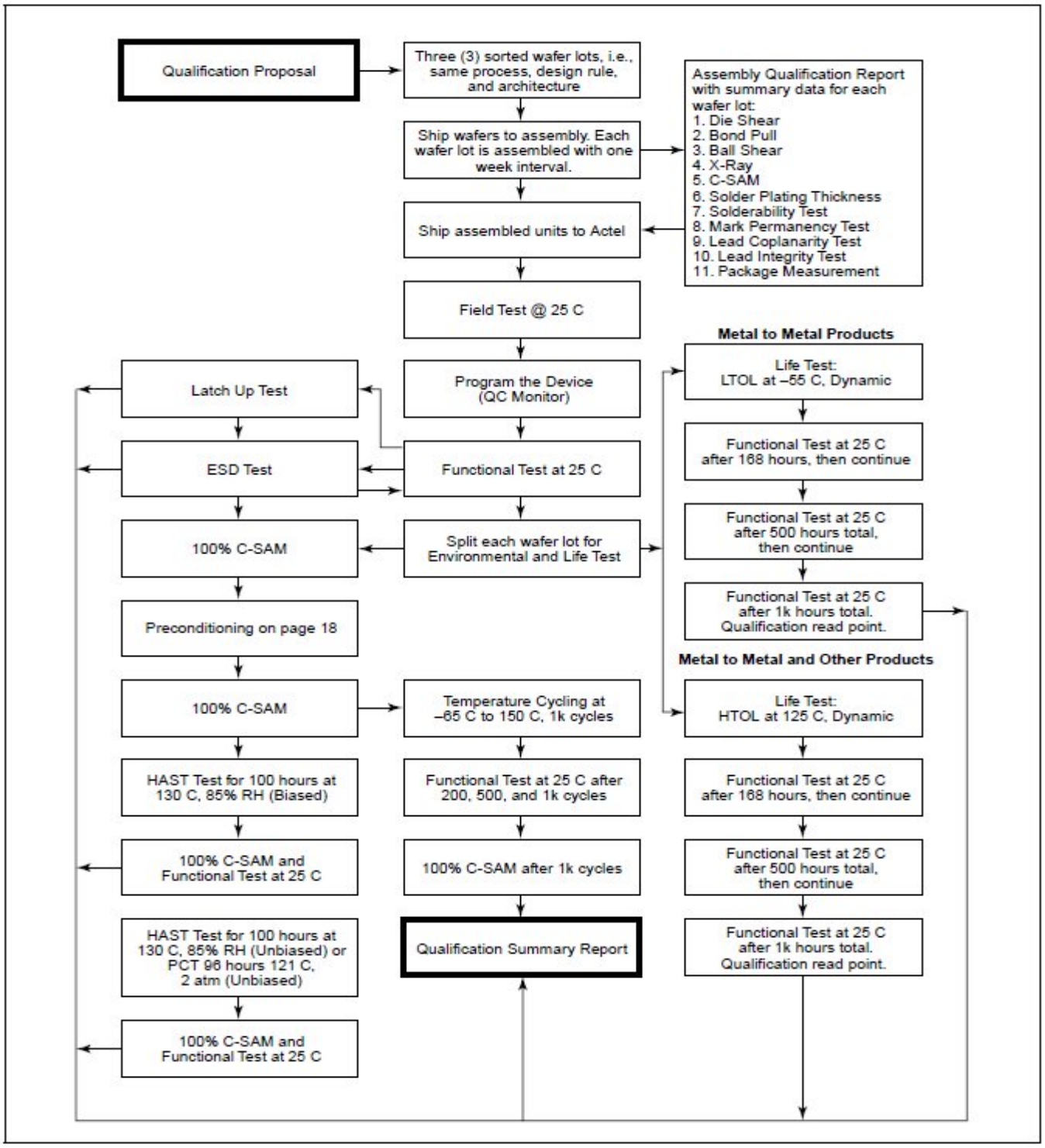


Figure 2: New Product Qualification (typical flow)

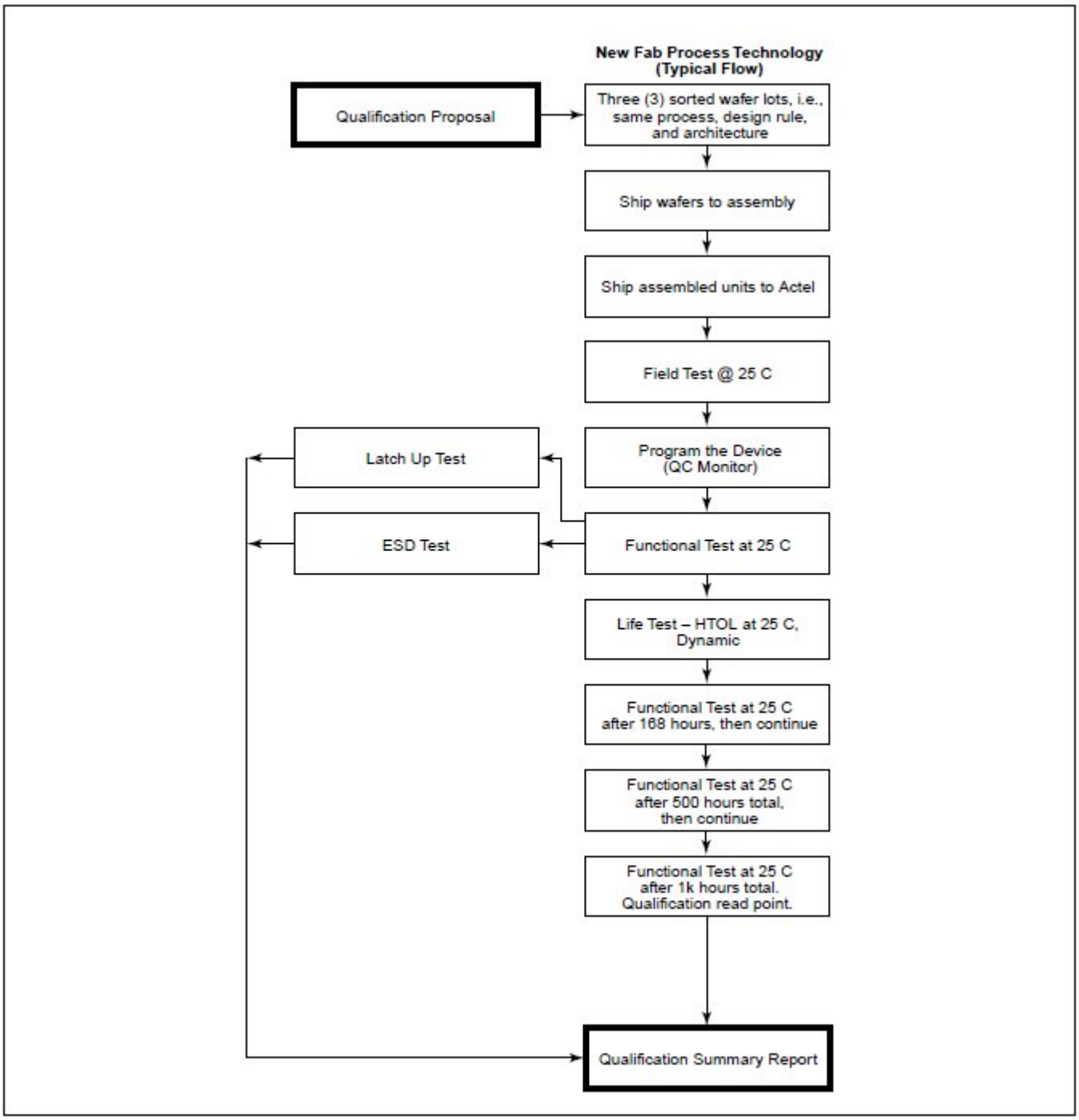


Figure 3: New Fab Process Technology (typical flow)

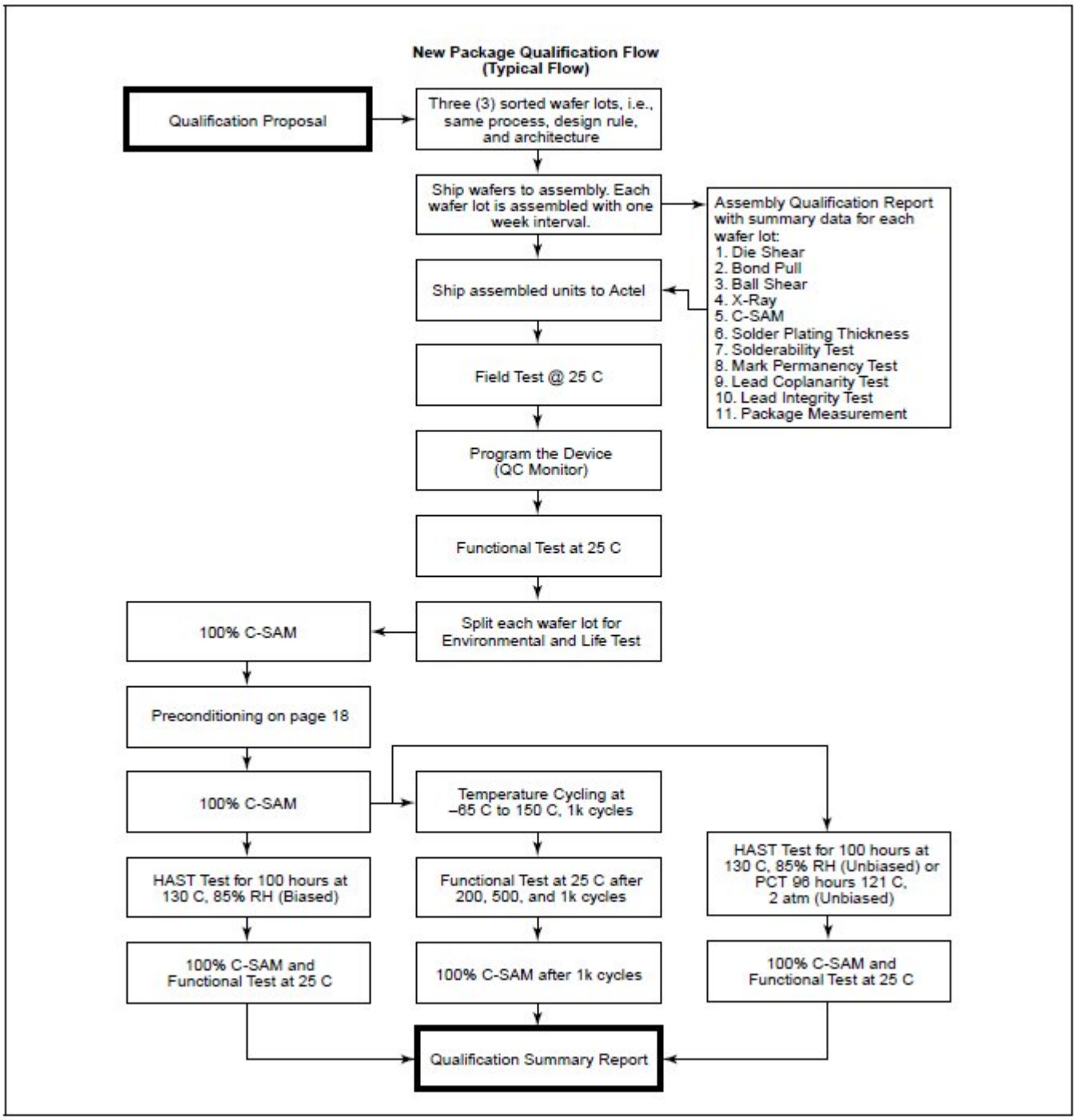


Figure 4: New Package Qualification Flow (typical flow)

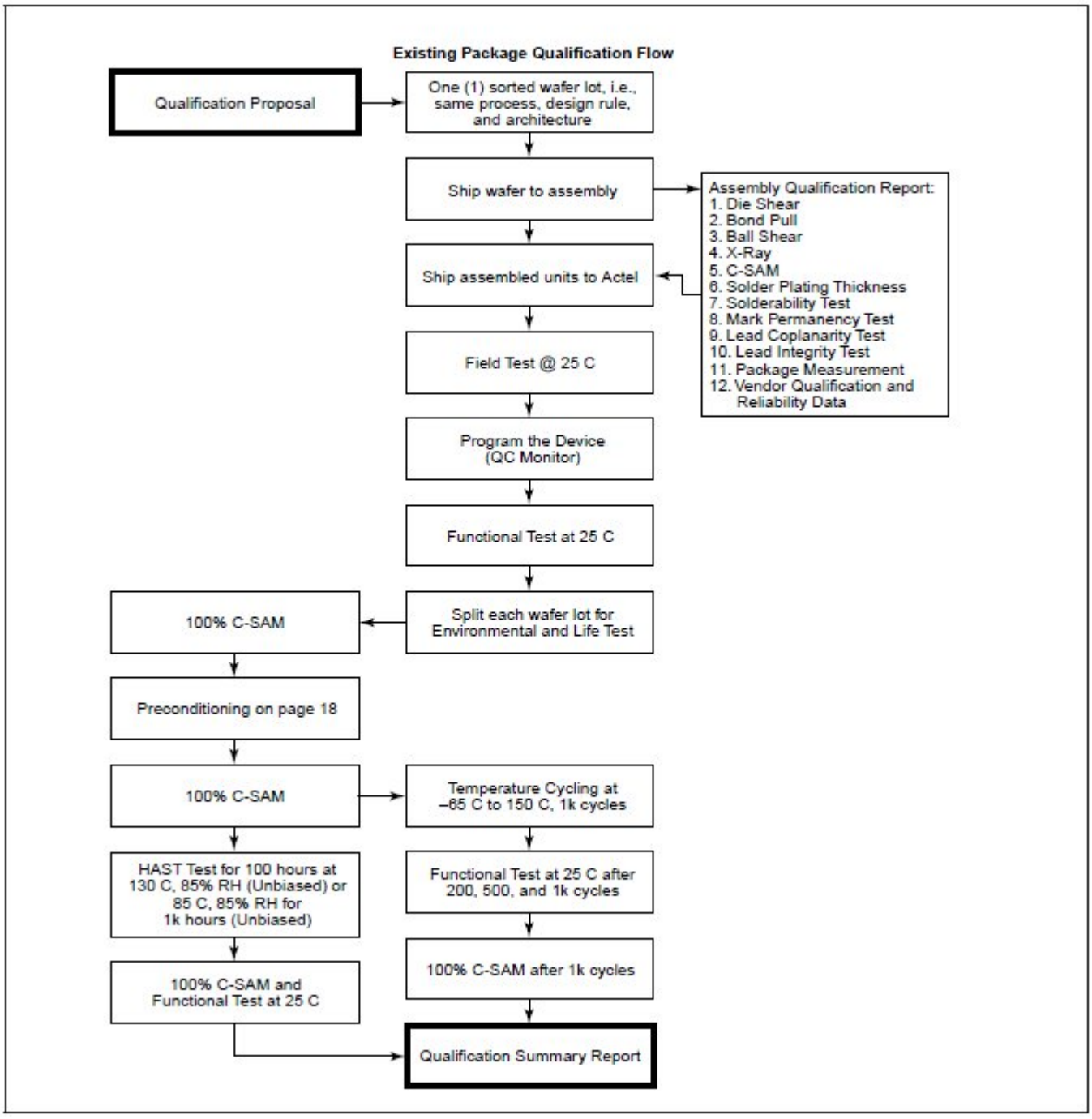


Figure 5: Existing Package Qualification Flow

Event	Test Method	Purpose of Test	Conditions
1. HTOL	Mil 1015	Determine the effect of high temperature and voltage on device performance	5.75V[1], 125°C, 1,000 hours
2. Preconditioning Stress Test (Plastic Package)	JEDEC-A113	Stress the integrity of the plastic package through board assembly simulation	Appendix A on page 57
3. HAST	JEDEC -A110	Evaluate the moisture resistance of die in plastic package	130°C, 85% RH for 100 hours
4. Temperature Cycle	Mil 1010, Cond C	Accelerate the thermo-mechanical failure mechanism of the package	1,000 cycles
5. Temperature Humidity		Accelerate the moisture dependent failure mechanism of the plastic package	85°C, 85%RH Unbiased 1,000 hours
6. Thermal Shock (optional for Plastic Package)	Mil 1011	Accelerate the thermo-mechanical failure mechanism of the package	–65°C to 150°C, liquid to liquid, 15 cycles
7. High Temperature Storage (optional for Plastic Package)		Detect mechanical reliability problems like bond integrity caused by temperature change	150°C Unbiased 1,000 hours
8. Solderability	Mil 2003	Determine the solderability of the device terminations to simulate the soldering process that will be used in the device application	
9. Mark Permanency	Mil 2015	Evaluate the marking integrity by using various solvents	
10. Lead Integrity	Mil 2004	Determine the package lead integrity	
11. Physical Dimension	Mil 2016	Verify the physical dimensions of the device are in accordance with the applicable procurement document	
12. Group D—Hermetic Packages Only	Mil 5005	Ceramic package integrity tests	
13. LTOL[2] (Low Temperature Operating Life)		Determine effect of low temperature and voltage on device performance	4.0V[1], –55°C 1,000 hours

Notes:

1. *3.0V for 0.25µm, 4.0V for 0.35µm.*
2. *For M2M products only. 3.0V for 0.25 µm, 4.0V for 0.35 µm.*

Table 1: Reliability Test Conditions

Test Description	New Assembly Plant [1 & 2]	New Pkg [3 & 4]	New Lead Finish	Change in Packaging Material(s) [5]	Mask changes affecting die size or active element [1]	Major Fab Process Change [1 & 6]	Existing Pkg Already Qualified by the Vendor [2 & 5]	New Device
1. HTOL					X	X		X
2. HAST[7]		X			X[8]	X[8]		X[8]
3. Temp Cycle	X	X		X	X	X	X	X
4. ESD					X[9]	X[9]		X[9]
5. Latch Up					X	X		X
6. Bond Pull	X	X		X			X	
7. Ball Shear	X	X		X			X	
8. Die Shear	X	X		X			X	
9. Solderability	X	X	X	X			X	
10. Lead Plate Thickness	X	X		X			X	
11. Mark Permanency	X	X					X	
12. X-Ray	X	X		X			X	
13. Thermal Shock (Optional)	X			X			X	
14. C-SAM	X	X		X			X	
15. AC/DC Char					X	X		X
16. Sort, FT Yield Analysis	X	X	X	X	X	X	X	X
17. Program Yield Analysis					X	X		X
18. High Temperature Storage	X			X			X	
19. Temperature Humidity – Unbiased 85°C/85%RH	X			X			X	

Notes:

1. Analysis is necessary. Once a wafer fab is qualified for a given die redesign change, other fabs can be qualified by test 18 only (no additional HTOL is necessary).
2. MInor Fab change qualification requires determination by the TRB.
3. Major Process Change, refer to Appendix A of MIL-PRF-38535, and MIL-STD 883.
4. New packages are defined as those that have been qualified for the first time.
5. The biggest package and die size for each family must be used for qualification.
6. A Major Die Redesign change is defined as any change of active device size or design rules. If a mask change is minor such as adjust CD, change E-Test structure, etc. only sort and final test yield are required.
7. May substitute 1,000 hours biased THB (85°C, 85% RH).
8. One lot is required for in-house reliability testing. Use qualification and reliability data from the vendor as supporting information.
9. Only required if I/O buffer is redesigned.

Table 2: Special Combination Qualification Requirements for Process and Design Changes

5.1.4 Quality & Reliability Testing

5.1.4.1 High Temperature Operating Life (HTOL)

The intent of an HTOL test is to operate a device dynamically (meaning the device is powered up with I/Os and internal nodes toggling to simulate actual system use) at a high temperature (usually 125°C or 150°C) and extrapolate the failure rate to typical operating conditions. This test is defined by RD-11 in the Group C Quality Conformance Tests. The Arrhenius equation (Equation 1) is used to calculate the extrapolation:

$$R = R_0 * \exp(Ea/kT) \qquad \text{Eq. 1}$$

where R is the failure rate, R0 is a constant for a particular process, T is the absolute temperature in degrees Kelvin, k is Boltzmann's constant and Ea is the activation energy for the process in electron volts.

To determine the acceleration factor for a given failure mode at temperature T2 as compared with temperature T1, we derive from the Arrhenius equation:

$$A_{(T1,\ T2)} = \exp^{[(Ea/k) * \{(1/T1)-(1/T2)\}]} \qquad \text{Eq. 2}$$

To use the Arrhenius equation, Table 6.3 gives the activation energies of typical semiconductor failure modes.

Failure Mechanism	Activation Energy
Ionic Contamination	1.0 eV
Oxide Defects	0.3 eV
Hot Carrier Trapping in Oxide (Short Channels)	–0.06 eV
Silicon Defects	0.5 eV
Aluminum-Silicon-Copper Electromigration	0.6 eV
Contact Electromigration	0.9 eV
Electrolytic Corrosion	0.54 eV

Table 3: CMOS failure modes

To evaluate Microsemi FPGAs, an actual design application is programmed into most devices (some units are burned in unprogrammed) and a dynamic burn-in is performed by toggling the clock pins at 1MHz or higher. The designs selected use 85 to 97% of the available logic modules and 85 to 94% of the I/Os. Outputs are loaded with 1.2 to 2.8kΩ resistors to Vcc. Under these conditions, each unit typically draws a minimum of 100mA during dynamic burn-in. Most of this current comes from the output loading, while about 5mA is from the device supply current.

For a 125°C burn-in, this results in junction temperatures of at least 150°C for plastic packages and 145°C for ceramic packages (depending on package type). Because junction temperatures can vary a great deal due to package, product, frequency, design, voltage, and other factors, the ambient temperature is used to calculate failure rates. These are worst case conditions because ambient temperature is always lower than junction temperature, and there is less acceleration when extrapolating device hours at lower temperatures. Most burn-in is done at Vcc = 5.75V or Vcc = 6.0V for 5.0V devices and Vcc = 4.0V for 3.3V devices (for voltage acceleration of the antifuse) and 125°C or 150°C.

As mentioned previously, some units are burned in unprogrammed. To accomplish this, internal circuitry is used to take advantage of the product's test features to shift commands to the chip serially during burn-in. All internal routing tracks are toggled between 0V and Vcc. When vertical tracks are at Vcc, horizontal tracks are held at 0V, and vice versa. Thus, all antifuses that can connect vertical and horizontal tracks receive a full Vcc stress in both directions. These toggling vertical tracks connect to logic module inputs and outputs when a part is programmed. Finally, a command is sent to the chip to toggle some external I/O pins between 0V and Vcc. This dynamic burn-in circuit is the same one used by Microsemi to screen unprogrammed products to RD-11 requirements. Since virtually all antifuses receive a full Vcc stress, this screen is much more effective in catching unprogrammed antifuse infant mortality failures than is burning in programmed devices, as it only stresses a fraction of the antifuses.

A failure is defined as any device that shows a functional failure, exceeds data sheet DC limits, or exhibits an AC speed drift. Among the parts tested, no speed drift, faster or slower, has been observed within the accuracy of the test setup. Failure rates at 55°C, 70°C, and 90°C have been extrapolated by using the Arrhenius equation and general activation energies of 0.6 eV and 0.9 eV. Poisson statistics have been used to derive a calculated failure rate with a 60% confidence level. Poisson statistics are valid for low failure rates and failure modes occurring randomly with time. At 55°C, the calculated failure rate with a confidence level of 60% (0.6 eV) was 22

FITs, or 0.0022% failures per 1,000 hours. This number was derived from nearly nine million device hours (at 125°C) of data. There were seven total failures out of 7704 tested units representing 134 different wafer lots. There were no infant mortality failures, which would normally occur in the first 80 hours of burn-in. Six of the seven failures observed were due to common CMOS failure modes (gate oxide failure, silicon defects, or open Via). The single antifuse-related failure in nine million device hours at 125°C represents a product antifuse failure rate of significantly less than 10 FITs at 5.5V.

5.1.4.2 Blank Level Burn-in

The following paragraphs detail the pre-programmed burn-in tests which Microsemi Radiation Tolerant (RT) FPGAs undergo before shipment to customers. The systematic and thorough burn-in tests include static burn-in and dynamic burn-in, with the intention that customers do not then need to perform additional burn-in or testing of these devices.

5.1.4.2.1 Burn-In Types

There are two categories of burn-in: steady state (static) and dynamic:

1. Static burn-in applies DC voltage levels to the pins of the device with the unit powered up. Static burn-in is by far the simplest to implement. By choosing appropriate biasing conditions and load resistors, it is possible to design a single burn-in circuit that can be used for both un-programmed and programmed devices. It would not matter what pattern is programmed into the device. Static burn-in can be an effective screen for failure modes that may happen at device inputs or outputs. Static blank burn-in (SBBI) does not toggle any I/O's or internal nodes. SBBI is considered an effective screen for mobile ionic contamination failure modes. However, design of seal ring barriers and improved passivation makes this failure mode highly unlikely.

2. Dynamic burn-in applies AC signals to device inputs with the unit powered up. These signals are selected so that the device receives internal and external stresses. It is effective at stressing internal device circuits and screen failure modes such as metal electro-migration. A properly designed dynamic burn-in can effectively stress inputs, outputs, and internal circuits. Microsemi has been able to use the testability features of our FPGAs to

allow effective dynamic burn-in of un-programmed devices. This dynamic burn-in allows users to stress circuits in a way that static burn-in would be unable to duplicate. Dynamic blank burn-in (DBBI) aims to stress un-programmed antifuses as vertical and horizontal tracks are driven to 0 and 1 alternately. In addition, inputs, outputs and internal circuits are stressed by alternate toggling of tracks which also causes input and output tracks of logic modules to toggle as well as exercising transistors in logic modules. I/O's are also stressed during DBBI.

5.1.4.2.2 Burn-In Procedure

During burn-in of un-programmed devices, test commands are serially shifted into each device by using the SDI/TDI pin and clocked by using the DCLK/TCK pin. There are three tests shifted into each device:

1. The first test stresses each cross-antifuse with a voltage on VPP by applying the maximum recommended operating condition on the un-programmed antifuses. This voltage is applied to all vertical tracks while the horizontal tracks are grounded.
2. The second test is identical to the first except that the horizontal tracks are driven to Vpp at maximum recommended operating condition while the vertical tracks are grounded. Not only do these tests stress the antifuses, but they also toggle all routing tracks in the chip to the maximum recommended operating voltage and ground. All input and output tracks to the logic modules are also toggled.
3. The third test drives several I/O pins on the chip to a low state. Prior to this, they are at high impedance state and held at Vcc through pull-up resistors. This test confirms that the burn-in is being properly implemented by looking at these I/O pins to see if they display the proper waveform. It also passes current through each I/O as it toggles low. Although the chip is un-programmed, these tests allow users to apply stresses to the inputs, outputs, and internal nodes that are similar to what a programmed device may see in normal operation. Once burn-in is completed, post-burn-in testing, as specified by RD-11, is performed to ensure that fully compliant devices are shipped to the customers.

5.1.4.3 Other FPGA Test Modes

Although the majority of Microsemi's RT FPGAs are one-time programmable, these devices' unique architecture permits a degree of testability comparable to reprogrammable devices. Special

test modes allow functional testing of un-programmed devices at essentially 100% fault coverage. Details of the various test modes are as follows:

- **Shift Registers test:** The shift register circling the periphery of the chip can be both downloaded and uploaded. This allows the use of various test patterns to ensure that the shift register is fully functional.

- **Continuity and Shorts test:** All vertical and horizontal tracks can be tested for continuity and shorts. There are several ways to implement these tests. One way of doing continuity testing is to pre-charge the array, turn on all vertical or horizontal pass transistors on a track, drive the track low from one side of the chip, and read a low on the other side. Shorts can be detected by driving every other track low after pre-charge and reading back on the other side. Note that these tests also confirm that the vertical and horizontal pass transistors will turn on.

- **Charge level test:** It is important for programming to make sure that all tracks can hold the pre-charge level. By charging a track, floating it, and waiting a predetermined amount of time, the track can be read back and confirmed to be still high.

- **Pass transistors test:** Leakage of vertical and horizontal pass transistors can be tested by driving one side of a track to a voltage via the Vpp pin and grounding the other side. All pass transistors except the one being tested are turned on. If excess current is detected on the VPP pin, the pass transistor is considered defective.

- **Clock buffers test:** The dedicated clock buffers, which travel across all horizontal channels, can be tested by driving with the clock pin and reading for the proper levels at the sides of the array.

- **Internal data path test:** The internal output of any logic module can be looked at to identify broken data path. This test is done by directing the logic module output to one of two dedicated vertical tracks, which can be observed externally on the special Probe A or Probe B pin. This ability to observe internal signals (even on un-programmed parts) allows Microsemi to perform a large number of functional tests. The first of such test is the input buffer test. Input buffers on all I/O pins can be tested for functionality by driving at the input pad and reading the internal I/O output node through the probe pins.

- **Output buffers test:** The output buffers are driven low, high, or tri-state to test VOL, VOH, IOL, IOH, and leakage on all I/Os and I/O configurations (i.e. single ended, differential, voltage reference, etc …).

- **Logic module functionality:** One of the key tests is the ability to test functionally all internal logic modules. By turning on various vertical pass transistors and driving from the top or bottom of the chip, any of the eight to ten module inputs can be forced to a high or low. The output of the module can then be read through the Action Probe pins. The logic module test allows 100%fault coverage of each module. In addition, the architecture allows modules to be tested in parallel for reduced test time. This test also includes functionality testing for SRAM and DSP math-blocks.

- **Speed test:** Microsemi FPGAs have one or two dedicated columns on the chip that are transparent to the user and used by the factory for speed selection. These columns are referred to as the Binning Circuit. Modules in the columns are connected to each other by programming antifuses. The speed of the completed test circuit can then be tested. The Binning Circuit allows the separation of units into different speed categories. It also allows the speed distribution within each category to be minimised.

There are also several tests to confirm that the programming circuitry is working. Details of these tests are as follows:

- **Leakage test:** This is a basic junction stress/leakage test. The program mode is enabled and Vpp voltage plus a guard band is applied to the Vpp pin. All vertical and horizontal tracks are driven to Vpp; thus, no voltage is applied across the antifuses. The IPP current is then measured. If it exceeds its normal value, the device is rejected.

- **Antifuse shorts test (or blank test):** This test ensures that all antifuses are not programmed. The array is pre-charged, and then the vertical tracks are driven to ground. The horizontal tracks are then read to confirm that they are still high because a programmed or leaky antifuse would drive a horizontal track low. The test is repeated by driving horizontal tracks low and reading vertical tracks.

- **Programming circuitry functionality:** The functionality of the programming circuitry can be verified by programming various extra antifuses, on the chip, that are transparent to the user.

- **Device identification and traceability:** Microsemi RT FPGAs also have a Silicon Signature, which consists of hardwired (no antifuses) manufacturer ID number as well as a device ID number. These numbers can be read by a programmer, and the proper programming algorithm can be automatically selected. The Silicon Signature also consist of words (programmable antifuses) used to store information such as the chip's run number and wafer number. Thus, each Microsemi RT FPGA has traceability down to the wafer level. By programming this information, the functionality of the programming circuitry is also tested. Microsemi software also allows the user to program a design ID and check sum into the Silicon Signature. By later reading this back, the user can verify that the chip is correctly programmed to a given design.

- **Antifuse stress test:** The most important antifuse test is the stress test. When this test is enabled, a voltage applied to the VPP pin can be applied across all antifuses on the chip while the other side is grounded. The voltage applied is the pre-charge voltage plus a significant guard band. After the voltage is applied, the antifuse shorts test is again used to make sure no antifuses have been programmed. The antifuse stress test is effective at catching antifuse defects. Because the reliability of the antifuse is much more voltage dependent than it is temperature dependent, this electrical test is also an effective antifuse infant mortality screen. Therefore, it is unnecessary to do any kind of burn-in for production units to screen out antifuse infant mortality failures. However, burn-in is still an effective screen for standard CMOS infant mortality failure mechanisms, and it is required by RD-11 Method 1005.

5.1.4.4 RTSX-SU Voltage Acceleration

To prove that Actel antifuse-based FPGA products can operate for 10 years with the required reliability, accelerated testing methodologies must be used. Accelerated testing to establish the reliability of the programmed antifuse is of the utmost importance.

Basically the programmed filament is TiN, which carries a high current density. Since this material fails by thermomigration and not electromigration, the temperature gradient across the filament is the critical parameter. This particular antifuse structure also has a certain level of tungsten in it, which also fails by thermomigration. Therefore the thermal characteristics are examined to determine the filament temperature under various temperature and voltage conditions in order to

predict the ability to accelerate the testing of programmed circuits. Microsemi has demonstrated that by raising the operating voltage, it is possible to accelerate the wear-out of a weakly programmed antifuse without wearing out the normal population of nominally programmed antifuses.

In its white paper on RTSX-SU voltage acceleration, Microsemi presents a method of using VCCA to accelerate the aging of a weak subpopulation of antifuses based on thermomigration. The data is in good agreement with the previously reported phenomenon of thermomigration of TiN with similar activation energy. In addition, a conservative acceleration factor in excess of 10X per 0.25-volt increase in the core voltage has been calculated. The critical constants for building a simulation have been experimentally determined as shown in the following equation:

$$\text{Resistance} = 0.16 \times (1{,}000/\text{IPP})^{1.32}$$

where:

IPP is in mA
$R/R0 = 1 + \beta \times (T–T0)$, where β is 0.0006
Theta = 0.0005 × (IPP) + 0.0009, where IPP is in mA and Theta is mW/K
Ea of 1.6 eV and Diffusivity = 1E3

5.1.4.5 Microsemi Accelerated Reliability Testing

The failure rate of semiconductor devices is inherently small. For this reason, the Microsemi uses accelerated testing to assess reliability of its devices. Overstresses are used to produce the same failure mechanisms that would be seen under normal conditions but in a much shorter period of time. Acceleration factors are used by Microsemi to estimate failure rates based on the results of accelerated testing. The objective of this testing is to identify the failure mechanisms and eliminate them as a cause of failure during the useful life of Microsemi products. Die selection is determined by both the largest die size and/or the currently available die. Microsemi will, whenever possible, test the largest die in a given family. Package selection for the testing is determined by test board availability and will not always include the largest package available.

Below in Table 4 the reliability summary and FIT rate by device technology is indicated. It should be noted that all FIT rates and MTTF numbers reported in Table 3 and in RD-4 use a base set of

assumptions. FIT rate is calculated using RD-5. The failure rate is calculated using Chi-square distribution at 60% confidence interval from the small number of failures and limited sample size of the population tested. The Chi-squared value is calculated from the inverse Chi-squared distribution using the desired probability level and degrees of freedom. Assuming that the actual usage voltage is within the rated specification, acceleration coefficients are calculated for temperature stress. Sample sizes, total devices tested, device hours, and failures can be found in the data tables for each product family. The Arrhenius Life-Temperature relationship is widely used to model product life as a function of temperature. This relationship is used to express both a single failure mechanism's sensitivity to temperature and the product thermal acceleration factor. For the full reliability summary report refer to RD-4.

Device Technology	Number of CMOS Failures	Device Hours	T_J (°C)	EA, eV	Confidence	FIT	MTTF
1.0 µm CMOS FPGA	1	3.60E+08	55	0.7	60%	5.62	1.78E+08
1.0 µm CMOS FPGA (RH1020)	0	3.97E+07	55	0.7	60%	23.05	4.34E+07
0.8 µm CMOS FPGA (RH1280)	1	9.16E+07	55	0.7	60%	22.04	4.54E+07
0.8 µm CMOS FPGA	0	2.05E+08	55	0.7	60%	4.47	2.24E+08
0.6 µm CMOS FPGA	0	1.82E+08	55	0.7	60%	5.04	1.99E+08
0.6 µm RT54SX CMOS FPGA	0	2.29E+07	55	0.7	60%	39.88	2.51E+07
0.45 µm CSM CMOS FPGA	1	1.03E+08	55	0.7	60%	19.62	5.10E+07
0.45 µm UMC CMOS FPGA	0	2.56E+07	55	0.7	60%	35.79	2.79E+07
0.35 µm CMOS FPGA	0	6.31E+07	55	0.7	60%	14.51	6.89E+07
0.25 µm MEC CMOS FPGA	2	7.51E+07	55	0.7	60%	41.40	2.42E+07
0.25 µm Infineon Flash CMOS FPGA	0	3.62E+07	55	0.7	60%	25.30	3.95E+07
0.25 µm UMC CMOS FPGA	0	7.78E+08	55	0.7	60%	1.18	8.5E+08
0.22 µm UMC CMOS FPGA	0	5.13E+08	55	0.7	60%	1.78	5.60E+08
0.22 µm UMC Flash CMOS FPGA	0	6.89E+07	55	0.7	60%	13.28	7.53E+07
0.15 µm UMC CMOS FPGA	2	4.41E+08	55	0.7	60%	7.04	1.42E+08
0.13 µm Infineon Flash CMOS FPGA	0	4.38E+08	55	0.7	60%	2.09	4.78E+08
0.13 µm UMC Flash CMOS FPGA	1	2.57E+08	55	0.7	60%	7.87	1.27E+08

Notes:

1. *Please refer to the "0.25 µm UMC FPGA Reliability Summary" section on page 33 for RTSX-SU antifuse FIT rate reliability data.*
2. *Technically, mean time between failures (MTBF) should be used only in reference to repairable items, while MTTF should be used for non-repairable items. However, MTBF is commonly used for both repairable and non-repairable items, hence MTTF or MTBF = 1/FIT.*

Table 4: Microsemi Reliability Summary & FIT Rate by Device Technology

5.1.4.6 Enhanced Antifuse Qualification (EAQ)

All Actel radiation-tolerant FPGAs are qualified in accordance with the RD-11 Class B specification prevailing at the time of qualification. The procedures described in this section are in addition to those procedures performed in compliance with RD-11 Class B.

5.1.4.6.1 High Stress Test Designs

The test designs employed for enhanced antifuse qualification are specifically designed to isolate antifuse failure mechanisms. They accomplish this by achieving an extremely high utilisation factor for logic modules and by implementing a variety of test structures, which thoroughly exercise all of the various antifuse deployments. The test designs (multiple delay lines of combinatorial modules, I/O test block and RAM test blocks) are extremely sensitive to small changes in net propagation delay, which could be caused by a change in the impedance of an antifuse. Such an impedance change could indicate damage in that antifuse. Figure 6 shows top-level EAQ overview of the high stress test design.

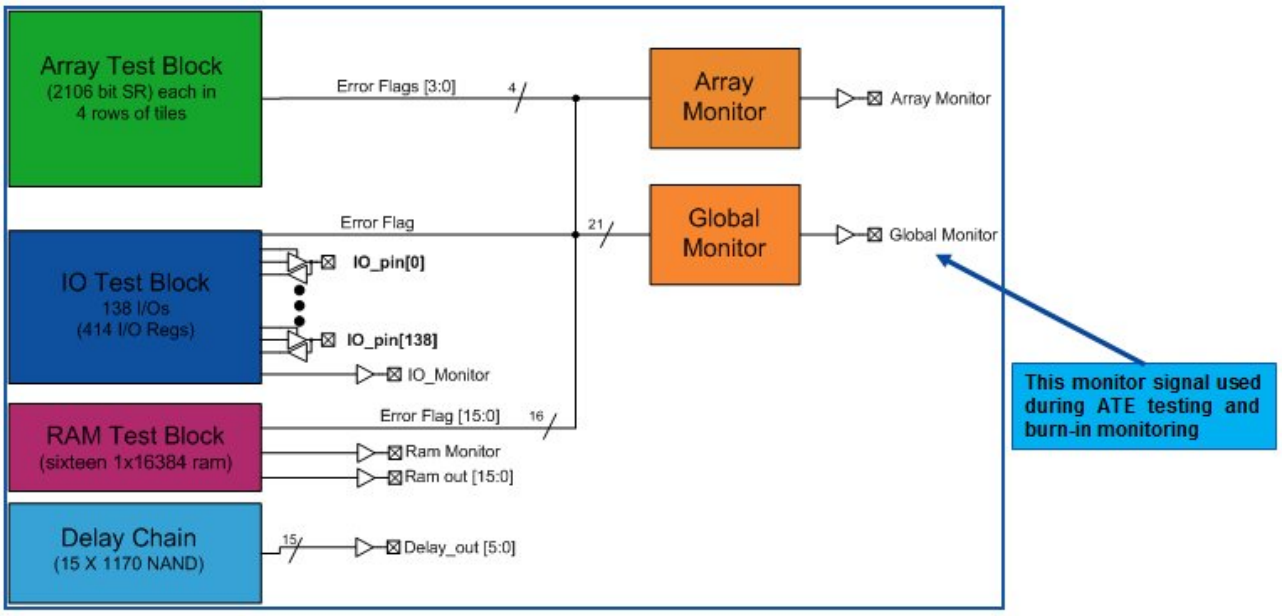


Figure 6: Top Level EAQ Diagram

In Figure 7 an overview of the SRAM block is illustrated. With the embedded SRAM blocks, full test coverage on all SRAM cells can be achieved with varying depth and width configurations.

Figure 8 presents the I/O test block of the high stress test design. This is a scalable block for maximising I/O utilisation by utilising all possible I/O configurations and controlled simultaneous switching outputs. In this design both input and output buffer of each I/O are exercised.

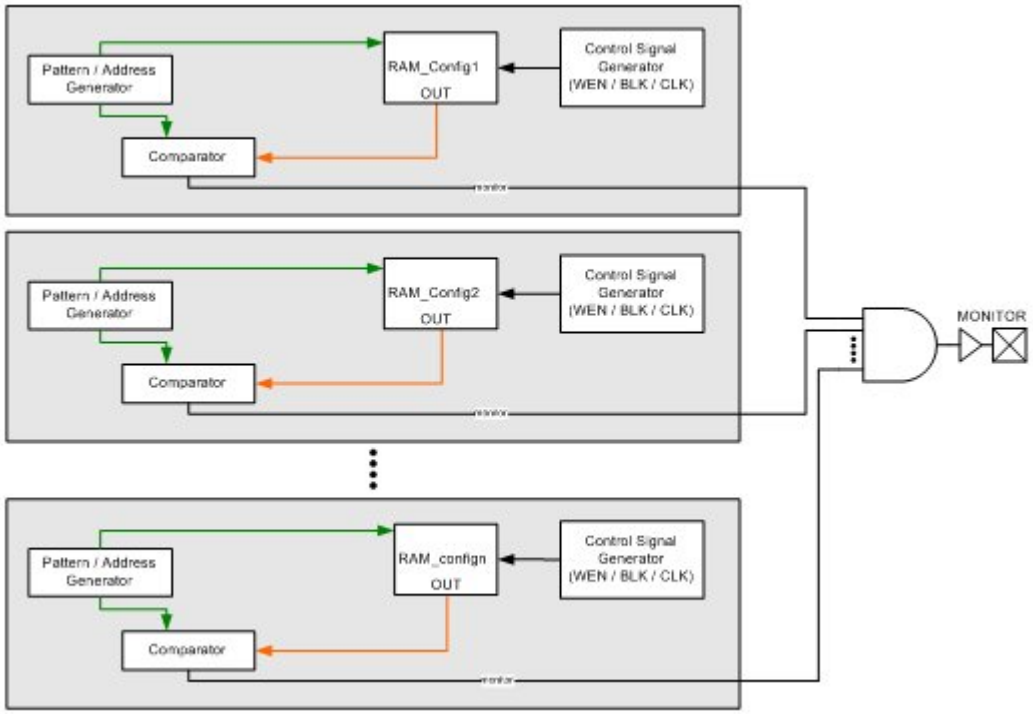


Figure 7: SRAM block overview

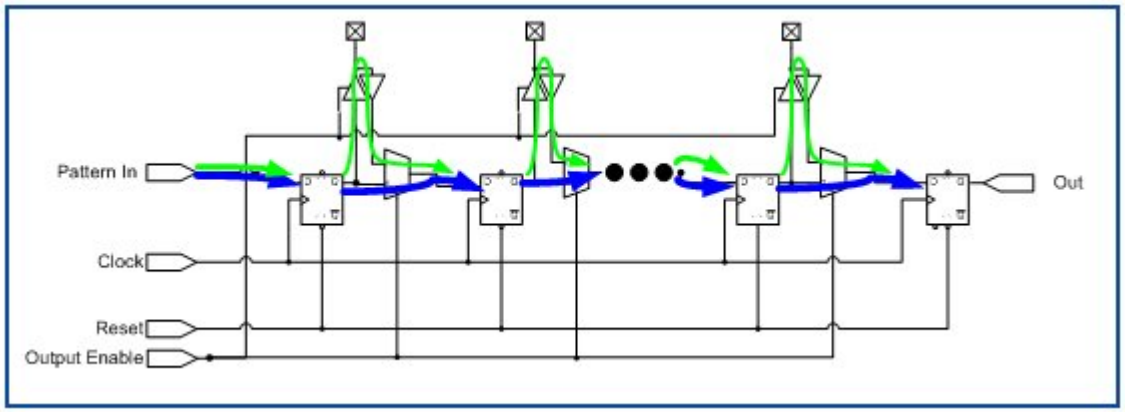


Figure 8: I/O Test Block

Figure 9 illustrates the HSB design overview. The goal of the high Single-S and Single-B antifuse design is to increase the utilisation of Single-S and Single-B antifuses, have short delay lines of combinatorial and sequential logic, together with multiple delay lines per device compared against each other at every burn-in pull point. Figure 4 indicates the delay lines and it should be noted that all delay lines exercised during burn-in.

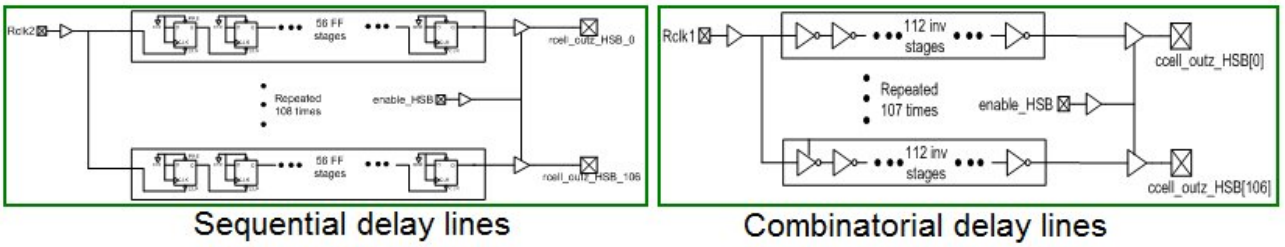


Figure 9: HSB Design Overview

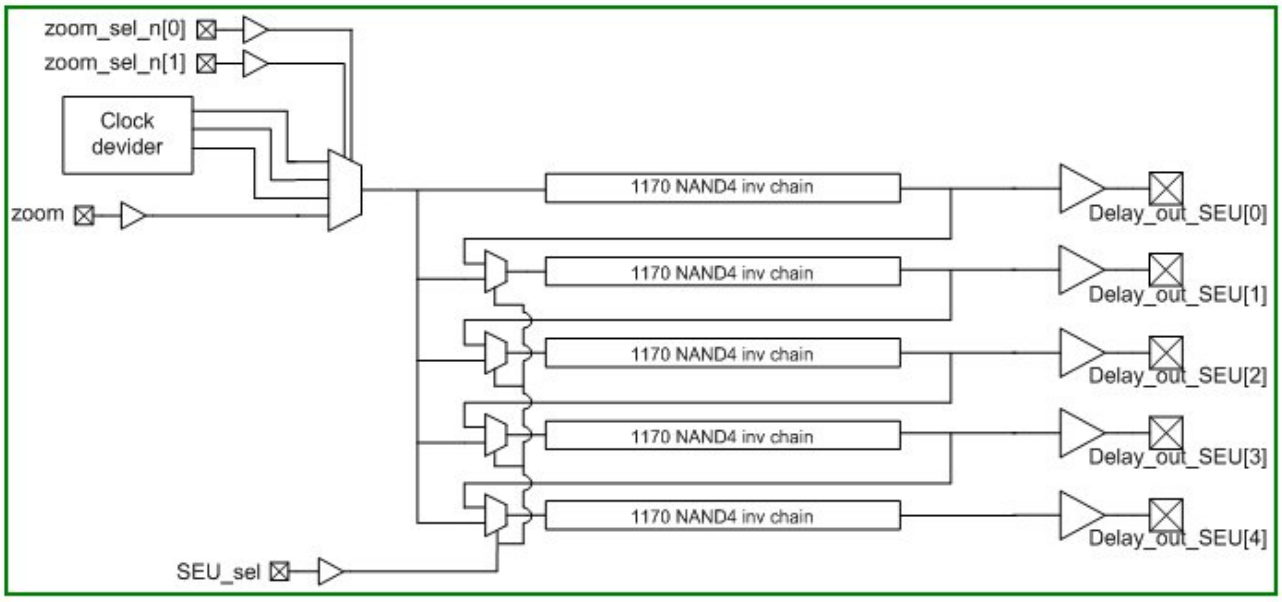


Figure 10: SEU Combinatorial Delay Block

Figure 10 illustrates the SEU combinatorial delay block of the high stress test design. The SEU delay lines have longer delays than EAQ and HSB designs. The delay line can be exercised through an input pin or a clock divider block. In addition each delay line can be cascaded to make up one long delay line.

However, it should be noted that Microsemi may modify the high stress test designs without notice in order to achieve higher levels of antifuse coverage or better resolution or perception of timing changes.

5.1.4.6.2 EAQ Test Method

As a supplement to the RD-11 Class B qualification procedures for each space-flight FPGA family, a sample of units is programmed with the high stress design and subjected to a dynamic high temperature operating life (HTOL) test for a minimum of 1,000 hours. The units may be sampled from multiple wafer lots. Additionally, multiple part types within the device family being qualified may be sampled. The EAQ test is not a pass/fail test. It is simply used to gather information on the long-term reliability of the antifuses used in Microsemi's space-flight FPGAs and to perform reliability testing beyond the requirements of RD-11 Class B. Tables 5 & 6 below list the test conditions and results for the EAQ tests performed since inception of the procedure. In some cases, testing has been sponsored by independent organisations.

Device	Units Started Testing	Hours	Device-Hours	Antifuse Failures	Test Conditions
RTSX32SU	150	1,000	150,000	0	T_J = 153ºC, V_{CCA} = 2.75 V
RTSX32SU	149	250	37,250	0	T_J = 155ºC, V_{CCA} = 3.00 V
RTSX32SU	150	1,000	150,000	0	T_J = 153ºC, V_{CCA} = 2.75 V
RTSX32SU	150	1,000	150,000	0	T_J = 150ºC, V_{CCA} = 2.50 V
RTSX72SU	75	500	37,500	0	T_J = 150ºC, V_{CCA} = 2.50 V
RTAX1000S	291	1,000	291,000	0	T_J = 132ºC, V_{CCA} = 1.60 V

Table 5: EAQ HTOL Results for RTSX-SU and RTAX-S Space-Flight FPGAs

Device	Units Started Testing	Hours	Device-Hours	Antifuse Failures	Test Conditions
RTSX32SU	150	250	37,500	1	T_J = –27ºC, V_{CCA}= 2.75 V
RTSX32SU	150	250	37,500	0	T_J = –27ºC, V_{CCA}= 2.75 V
RTSX32SU	150	500	75,000	0	T_J = –29ºC, V_{CCA}= 2.50 V
RTSX72SU	75	1,000	75,000	0	T_J = –29ºC, V_{CCA}= 2.50 V
RTAX1000S	292	250	73,000	0	T_J = –54ºC, V_{CCA}= 1.60 V

Table 6: EAQ LTOL Results for RTSX-SU and RTAX-S Space-Flight FPGAs

One antifuse failure occurred on RTSX32SU during Low Temperature Operating Life (LTOL) testing, manifesting itself as a marginal increase in propagation delay. This failure was due to an S-antifuse on a net with only one antifuse (this is known as a "single S-antifuse net"). An update to the routing software in release 6.2-SP1 was developed to mitigate this failure mechanism by significantly reducing operating current stress in single S-antifuse nets.

Table 7 below indicates the ELA sample size by device type where zero rejects are allowed.

Device	ELA Sample Size
RTSX32SU	100 (0)
RTSX72SU	100 (0)
RTAX250S	100 (0)
RTAX1000S	24 (0)
RTAX2000S, RTAX2000D	14 (0)
RTAX4000S, RTAX4000D	8 (0)

Table 7: ELA Sample Size by Device Type

5.1.4.7 Enhanced Lot Acceptance (ELA)

In addition to enhanced qualification procedures, Microsemi has also implemented supplementary testing performed on a per-wafer-lot basis, in order to ensure that no process-dependent antifuse failure mechanisms are present. The enhanced lot acceptance tests are supplementary, and are performed in addition to the lot acceptance tests and screens that are already in place.

There are three types of enhanced lot acceptance screening:

1. Cross-section analysis of samples from each wafer
2. High-temperature operating life (HTOL) test of units sampled from each wafer lot
3. Thermal runaway characterisation test of two units sampled from each wafer lot.

5.1.4.7.1 ELA Cross Section Analysis

In order to ensure that there are no construction issues which may lead to reliability problems, two dice are sampled from each wafer of incoming RTSX-SU and RTAX-S FPGAs. The dice are cross sectioned and a sample of electron micrographs are inspected by technology experts in Microsemi's Technology Development (TD) group. Any construction issues observed by the TD team will result in the wafer in question being quarantined until its reliability can be assured by more detailed testing.

5.1.4.7.2 ELA HTOL Test

A high temperature operating life test is performed on a sample from each wafer lot of RTSX-SU and RTAX-S FPGAs.

5.1.4.7.3 Thermal Runaway Characterisation Test

As process nodes get smaller and geometries decrease, the transistors have a lower threshold as to when a device can get into thermal runaway. RTAX-S is based on a 0.15µm process and as a result can reach a thermal runaway state at a smaller junction temperature than the earlier generation RTSX-SU 0.22µm process based product. Given this expectation, Microsemi has taken two major steps to ensure that RTAX-S wafers do not go into thermal runaway. One of the steps is reduce the specification for the junction temperature of the product from 150°C to 125°C, which is typical for 0.15µm CMOS process (as stated in the RTAX-S/SL Family FPGAs datasheet). The second step is to institute a thermal characterisation test as part of the production process starting with wafer lots fabricated in 2007 and beyond. In this test, two units from every wafer lot are tested at ambient temperatures up to 135°C to characterise the device thermal stability at temperatures higher than the 125°C junction temperature. Any units that exhibit thermal runaway (sharp and uncontrollable increase of Icc current at high temperature) are scrapped along with the wafer lot.

5.1.4.7.4 ELA HTOL Test Design

The design used during ELA testing will, in most cases, be identical to the high stress design used for EAQ. The objective of the design is to exercise as many different antifuses of as many different types as possible and to observe timing changes with resolution as fine as possible. In order to optimise resolution and coverage, Microsemi may change or update the ELA test design without notice.

5.1.4.7.5 ELA HTOL Test Method

The enhanced lot acceptance testing requires that a sample of packaged units be removed from the first assembly lot from each wafer lot of RTSX-SU and RTAX-S space-flight FPGAs. The sample size is determined by the product type. RTSX32SU and RTSX72SU are sampled at a minimum of 100 units per wafer lot. The larger RTAX-S parts are sampled at a lower rate, since there are fewer parts per wafer lot. The sampled units are subjected to HTOL testing for a minimum of 168 hours. RTSX-SU FPGAs are operated at junction temperature of 145ºC, and RTAX-S FPGAs are operated at a junction temperature of 125ºC. After the HTOL, a full electrical test is performed on the sampled units at room temperature. This testing will be performed in parallel with the production screening process for the flight units, and must be completed prior to shipment of flight units from the wafer lot. Any failures detected during the electrical test will be subjected to a full failure analysis. The lot will be put on hold pending resolution of the failure analysis. During this time, no customer shipments will be made from the lot.

5.1.4.7.6 ELA HTOL Results

Table 8 below presents the results from the enhanced lot acceptance testing performed on the RTSX-SU and RTAX-S product families since inception of the enhanced procedure.

Product	Wafer Lot	Quantity of Units	Failure Quantity	Number of Hours	Unit hours	Type of Test	Wafer Lot Status
RTSX32SU	D19S61	100	0	168	16,800	HTOL	PASS
RTSX32SU	D1AYJ1	100	0	168	16,800	HTOL	PASS
RTSX32SU	D1AYJ1	100	0	168	16,800	HTOL	PASS
RTSX32SU	D1JW21	100	0	168	16,800	HTOL	PASS
RTSX32SU	D122H1	100	0	168	16,800	HTOL	PASS
RTSX32SU	D1N8F1	100	0	168	16,800	HTOL	PASS
RTSX72SU	D1HLH4	100	0	168	16,800	HTOL	PASS
RTSX72SU	D1HLJ1	79	0	1,000	79,000	HTOL	PASS
RTSX72SU	D1HLJ1	100	0	168	16,800	HTOL	PASS
RTSX72SU	D1MM81	100	0	168	16,800	HTOL	PASS
RTSX72SU	D1N8A1	100	0	168	16,800	HTOL	PASS
RTAX2000S	D1GAG1	14	0	168	2,352	HTOL	PASS
RTAX2000S	D1N9H1	14	0	168	2,352	HTOL	PASS

Table 8: ELA Results for RTSX-SU and RTAX-S Space-Flight FPGAs

5.2 MEC Antifuse Technology

5.2.1 MEC Antifuse : Construction

The RT54SX-S and A54SX-A devices were manufactured using a 0.25µm technology at the Matsushita (MEC) facility in Japan. It was a 3 layer metal process for the RTSX32S and A54SX32A devices versus 4 metal layers for the RT54SX72S and A54SX72A devices. The architecture of the RT54SX-S devices was an enhanced version of Actel's A54SX-A device.

The MEC antifuse construction was as follows:

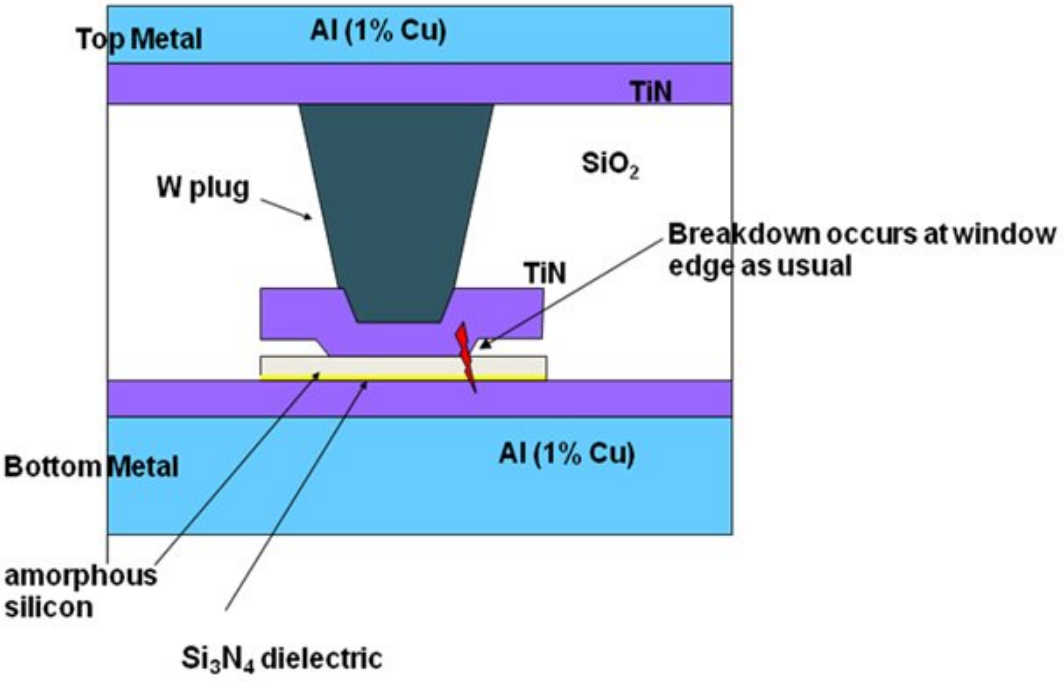


Figure 11: MEC Antifuse Construction

5.2.2 MEC Antifuse : Failure Mechanism

The failure mechanism observed on MEC antifuses was caused by residual polymer in the via at the bottom of the tungsten plug.

- Once the link has begun to form at the edge of the cell opening under the via residual polymer in the area is heated to approximately 1000°C causing the polymer to outgas residual volatile compounds.

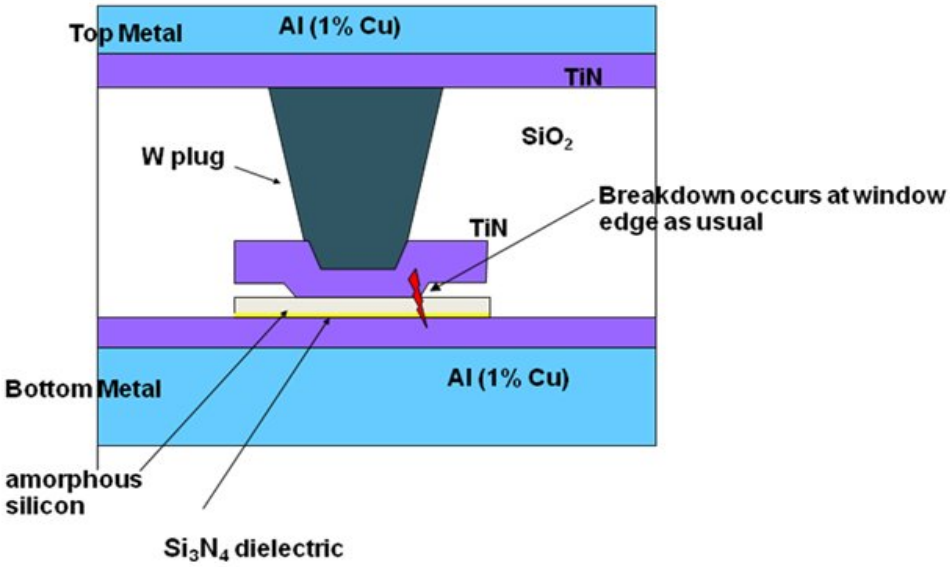


Figure 12: MEC Antifuse showing Breakdown at the Window Edge

- This causes a pressure wave that drives the forming link of TiN into the amorphous and under the oxide and away from the hard tungsten plug.

At this temperature the oxide as well as the a-Si is soft and easily flows out of the way, back filling the area vacated by the TiN.

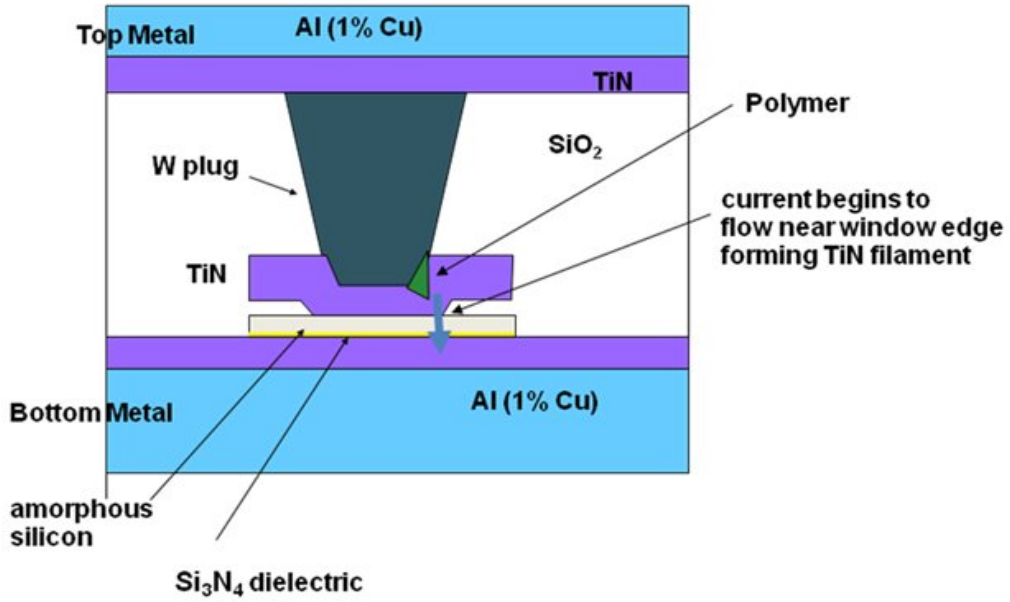


Figure 13: MEC Antifuse showing Current Flow near Window Edge

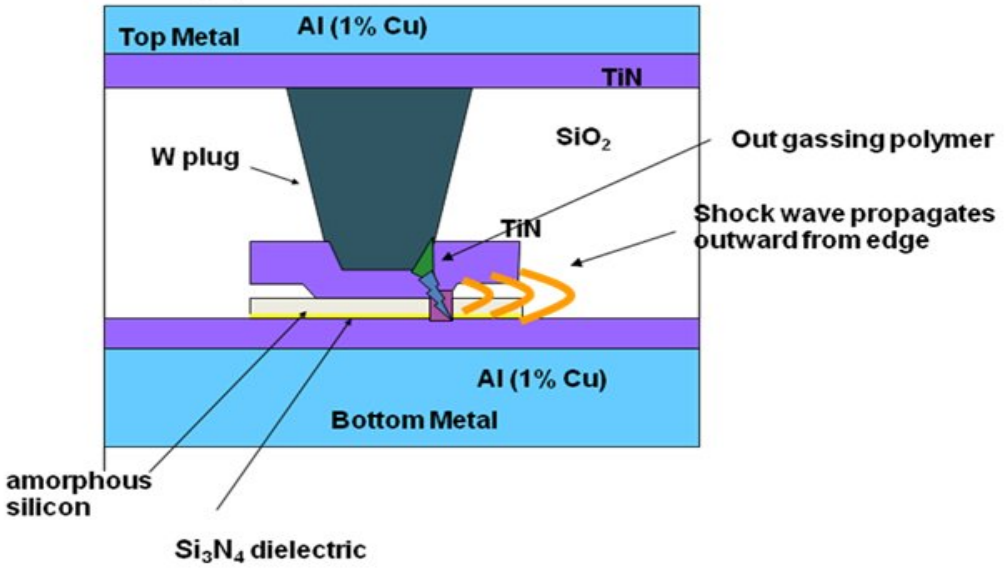


Figure 14: MEC Antifuse showing Shock Waves near Window Edge

- The current is momentarily interrupted by the link being blown out and the voltage begins to rise.
- Simultaneously the pressure wave is pushing TiN into the oxide and therefore forms a new link with a new collapsing voltage spike in the oxide once the TiN reaches the top TiN plate.

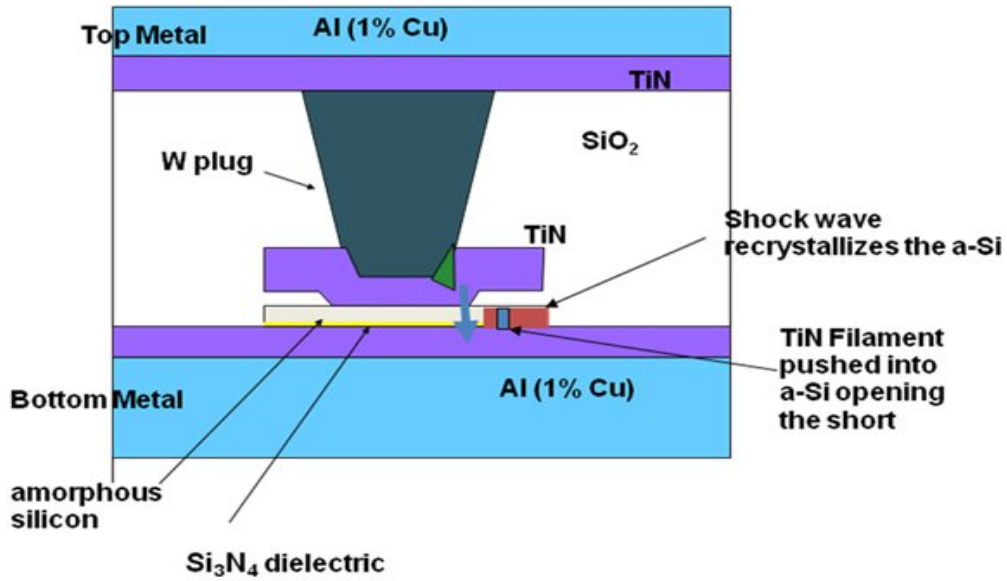


Figure 15: MEC Antifuse pushed TiN Filament

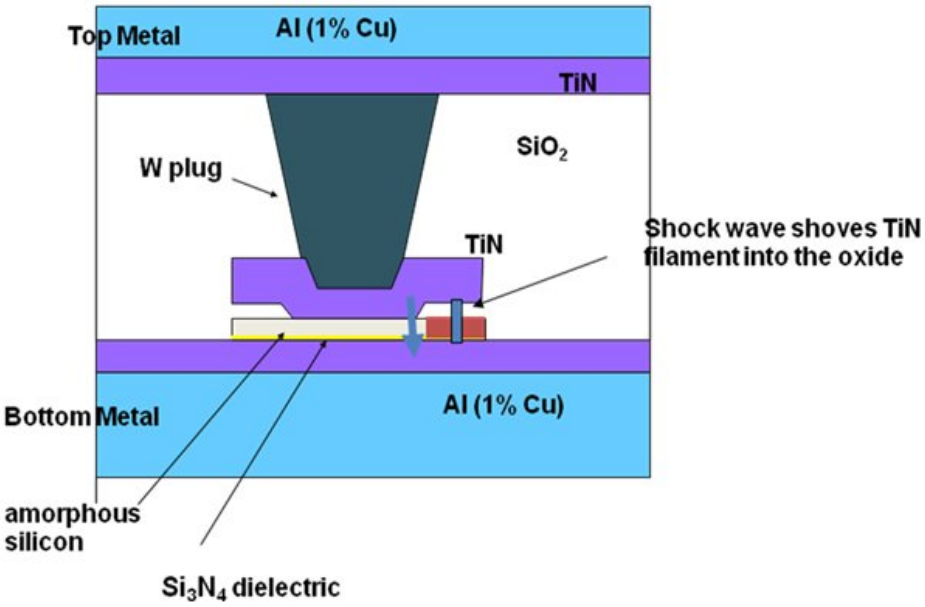


Figure 16: MEC Antifuse with TiN pushed into Oxide

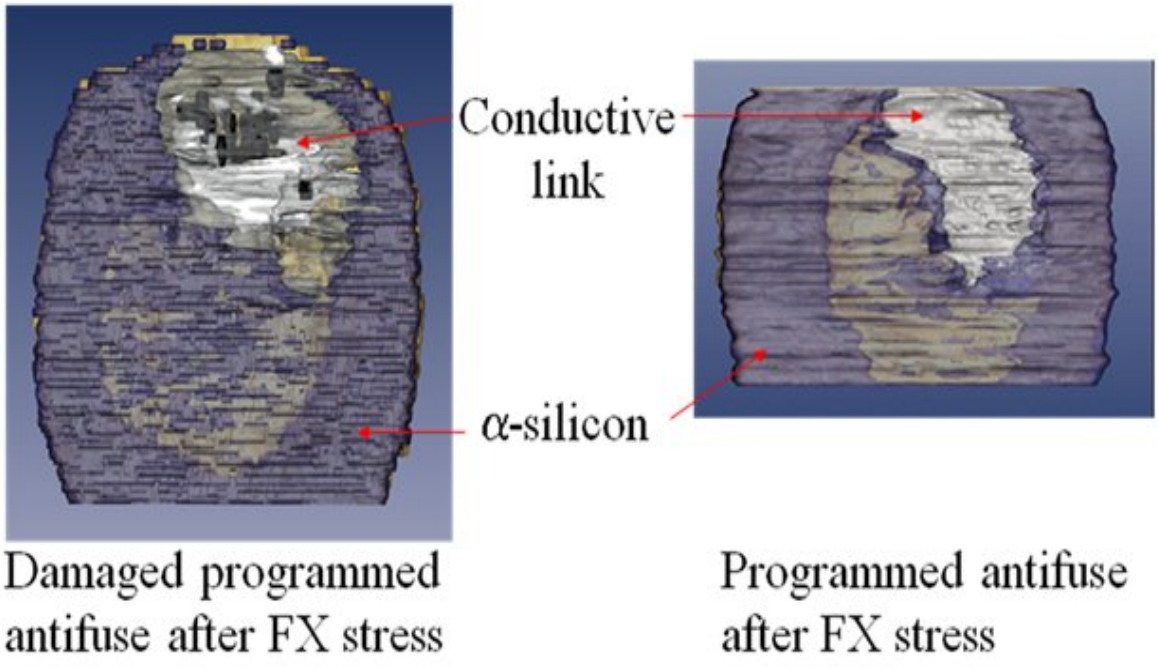


Figure 17: Damaged Programmed & Programmed MEC Antifuses

5.2.3 MEC Antifuse : Reliability Data

5.2.3.1 Independent Review on NASA Space Flight Missions

As of 2004 the 0.25µm SX-A/SX-S parts had been used successfully, with over a million units in use and with a rated reliability of approximately 10 FITS, based on a qualification program of approximately 3,000 parts that underwent post-programming dynamic testing. However, there have been several "clusters of failures" at several aerospace organisations. Previous generations of devices operated essentially failure-free throughout the entire industry. At this point no data indicated device failure when operated in compliance with the manufacturer's specification. However, a correlation between damage to the parts and exceeding absolute maximum ratings had been shown. While the sensitivity of the programmed antifuse was considered the weakest link of these devices in particular, the lower margins and increased susceptibility to damage is a trend of modern, high-performance digital electronics in general.

In January 2004, a meeting was held at the NASA Goddard Space Flight Centre (GSFC) to address the issue of Actel SX-S FPGA reliability as related to the failures reported by General Dynamics, Boeing Satellite Systems and the Jet Propulsion Laboratory (JPL). In May 2003 General Dynamics had reported failures (both SX-A and SX-S) on their Department of Defense (DOD) programs but declined to participate or provide access to relevant data. On other DOD programs, Boeing Satellite Systems reported failures in the latter half of 2003 and presented their preliminary data. For the Mars Exploration Rover (MER) and the Mars Reconnaissance Orbiter (MRO) programs, JPL reported manufacturing defects at a rate far higher than that expected from the manufacturer's published reliability data. The reported failures raised concern for all users of these devices throughout NASA, the Department of Defense and others.

The electrical environment created by both the automatic test equipment and the post-programming burn-in equipment at the facility used for MER parts testing had been found to be electrically "dirty." Standard design and test practices (e.g., terminating the 50Ω outputs of laboratory instruments, adequate supply bypassing, proper termination of device inputs, prevention of bus contention, as well as others) for digital systems were not followed. As a result supply voltages exceeding absolute maximum values, violation of input transition time limits, large device currents from improper configuration, and potential bus contention were observed. These factors contributed to excessive stress levels potentially leading to device damage. It was also an

observation that the test personnel did not fully understand the operation of the equipment, the implications of exceeding specifications, and performance requirements of the parts.

The MER program had an unusually high fallout rate in screening with 16 parts failing out of approximately 75 i.e. over 20%. The failures fitted into several categories. The three programming failures were not considered a problem, inherent in the technology, and have been credibly explained by the manufacturer, starting with the first generation of these parts for aerospace systems over a decade ago. However, most of the failures were not benign. One was a result of a test configuration error, with clock inputs not properly terminated, resulting in high device currents. Several other devices were most likely victims of electrical overstress from the "dirty" environment created by the test equipment. Based on the data and analysis presented, it was concluded at this time that the likely causes of the MER failures were related to the testing and not the devices. The conclusion was supported by the available data, analysis, the known electrically dirty environment, and experience with these devices.

The MRO program's fallout rate was even higher than MER's at 50%, with three out of 6 parts being rejected. Some of these parts had an inexplicable test signature of higher device leakage currents at 25°C than at either -55°C or +125°C, not a pattern typical of these devices in particular or CMOS devices in general. Device evaluation in the NASA test fixture was further recommended with data collected at additional temperature points to permit a proper evaluation.

The details of post-programming burn-in (PBBI) and the use of automated test equipment (ATE) were discussed extensively. The discussion included the capabilities of the equipment with respect to fault detection, the design of the equipment and operating principles, a review of the data, and the performance and risks associated with these test sets. Also discussed was the demonstrated reliability of the devices in qualification tests along with the vulnerability of these parts to damage from "dirty" electrical environments. It was concluded that post-programming burn-in and the automated testing of these devices are not recommended since in many cases the risk of the tests outweighs the benefits.

If PBBI and/or ATE testing is to be performed, a quantitative justification of the desired reliability improvement should be required, along with an analysis of the fault acceleration and detection capabilities of the test. In addition the test equipment must be designed, reviewed, and qualified to flight-type electrical standards and meet all device specifications.

5.2.3.2 PPBI for RT54SX-S and A54SX-A Devices

As indicated in RD-6, this Actel paper addresses the concern of burn-in (BI) for programmed FPGAs with regard to the RT54SX-S and A54SX-A FPGA devices in the un-programmed versus programmed mode. It was noted that during blank device electrical testing, these devices were subjected to controlled voltage stress conditions significantly higher than the maximum operating conditions specified in the datasheet. Because of the lower defect densities and the voltage screening performed by the manufacturer, infant mortality failures have not been an issue. The un-programmed antifuse infant mortality failures are sufficiently screened out during blank device electrical testing. Therefore, the manufacturer considers it unnecessary to do a burn-in to screen out failures of this type in standard commercial production units. Voltage stress testing of semiconductor devices is a much more effective screen than a temperature burn-in. The fallout seen during the burn-in test phases have been due to handling and improper burn-in conditions, not defects. Pre and post BI methodologies for un-programmed units were covered for dynamic and static BI conditions. In conclusion by the manufacturer, data demonstrated that PPBI for RT54SX-S and A54SX-A products was not required nor recommended.

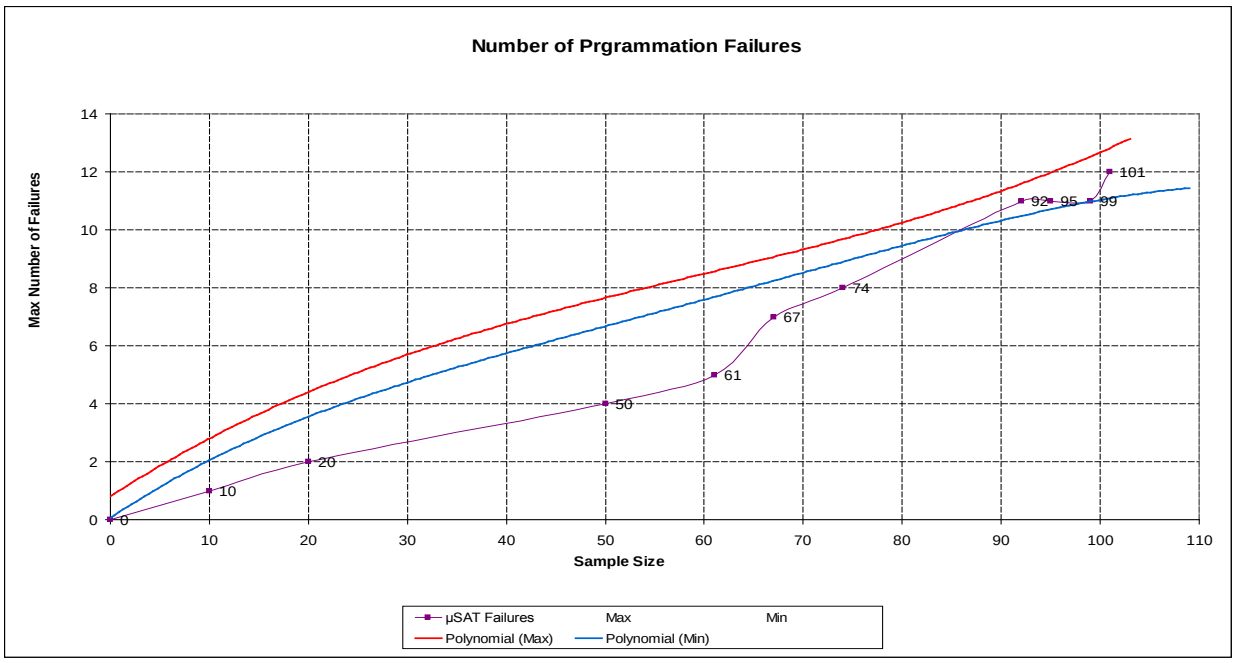
5.2.3.3 Thales CS & CNES RTSX-S Experience

Over the years, Thales CS together with CNES has programmed up to 101 RT54SX32S devices. Over this time period 12 programming failures have been observed on these devices (refer to Figure 18 below). In these instances no post-programming burn-in sequence was applied to the devices. These failure were simply noted as programming failure and no common failure root cause was identified among these 12 failing RT54SX32S devices.

5.3 UMC Antifuse Technology

5.3.1 UMC Antifuse : Construction

An amorphous-silicon antifuse at its most basic is a dielectric separating two electrodes, with amorphous silicon as the dielectric. The dielectric normally exhibits giga-ohm-level resistance, effectively isolating the electrodes. Upon application of a suitable programming voltage and current, however, a region of the amorphous silicon forms a conductive channel weaker than 100 ohms connecting the electrodes.



Red curve presents the maximal programming failures (ACTEL information)
Blue curve presents the minimal programming failures (ACTEL information)
Purple curve presents the number of programming failures

Figure 18: RT54SX32S programming failures at Thales CS & CNES

The programmed antifuse behaves as a stable, reliable, linear resistor within its operating range and should maintain its low resistance during the device's lifetime. If damaged, however, the programmed antifuse adopts a nonlinear behaviour and its resistance becomes unstable. The resistance of a damaged programmed antifuse can vary from a hundred to tens of thousands of ohms and can change substantially over time when significant current flows through it.

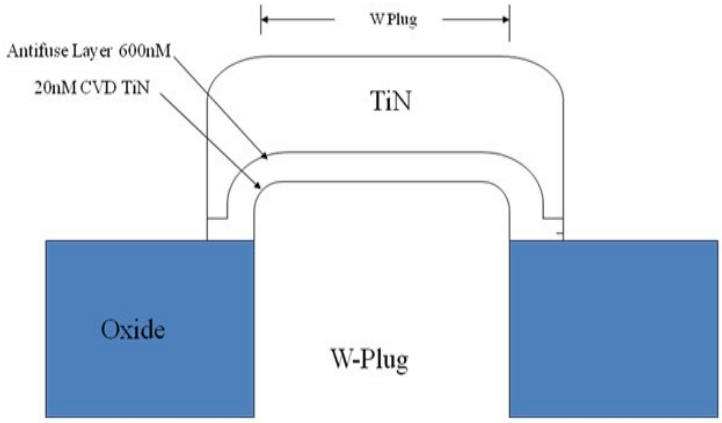


Figure 19: UMC Antifuse Construction

5.3.2 UMC Antifuse : Failure Mechanism

In the UMC RTSXA antifuse there was a very low antifuse failure rate on low programming current/ high stress input antifuses. These occurred if the antifuse programmed at the outer edge away from the tungsten plug, starving the filament of tungsten. These were eliminated by lowering the stress on the high stress antifuse and improving the programming conditions. This has never occurred on AX or RTAXS antifuses due to the higher programming currents, lower stress and smaller geometry of the AX product.

5.3.3 MEC Antifuse versus UMC Antifuse Comparison

Figure 20 below shows as SEM cross-section of the MEC antifuse, while in Figure 21 a SEM cross-section of the UMC antifuse is illustrated.

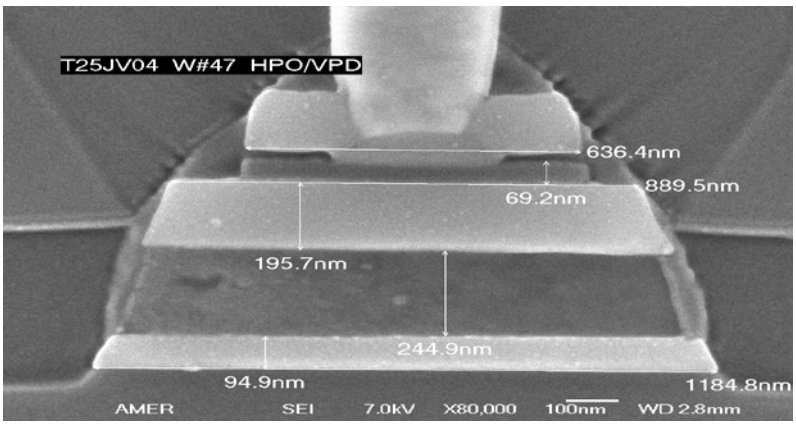


Figure 20: MEC antifuse cross-section

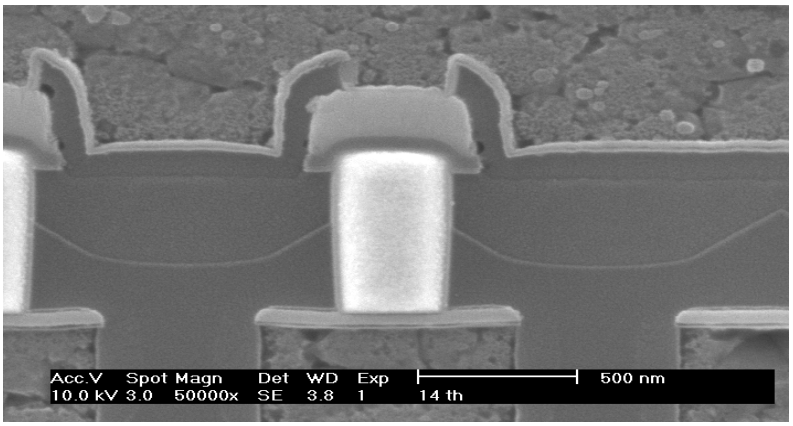


Figure 21: UMC antifuse cross-section

In the UMC process technology flow, following the CMP of the tungsten plug the oxide is recessed by an oxide polish. This raises the edge of the plug above the oxide. The breakdown/link formation is therefore at the exposed corner. The antifuse sandwich is then deposited and includes a 2500A TiN cap plate. As a result the antifuse filament is comprised of TiN and tungsten. This sandwich is then masked, an oxide is deposited and a contact opening is etched in the oxide. This prevents any shorts at the edge of the antifuse structure. The standard Ti/TiN/aluminum top metal is then deposited.

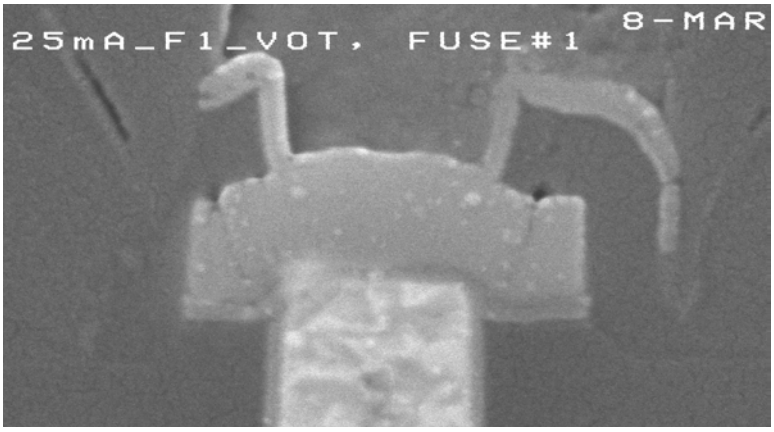


Figure 22: Programmed UMC antifuse cross-section

As a result of this process integration change, the UMC version of the Microsemi antifuse is highly unlikely to incorporate oxide into the filament. It should be noted that

- The point of formation is above the oxide.
- The heat flow is with the electron wind such that the heat is flowing away from the oxide into the TiN plate.
- The tungsten plug has one order of magnitude higher thermal conductivity than TiN.
  - The tungsten is next to the oxide helping to cool it
  - The TiN will heat up the most but it is not near the oxide
  - Tungsten does not react with oxide like titanium

5.3.4 UMC Antifuse : Reliability Data

Below in Table 9 the reliability summary and FIT rate by device technology is indicated. It should be noted that all FIT rates and MTTF numbers reported in Table 9 and in RD-4 use a base set of assumptions. FIT rate is calculated using RD-5.

Device Technology	Number of CMOS Failures	Device Hours	T_J (°C)	EA, eV	Confidence	FIT	MTTF
1.0 µm CMOS FPGA	1	3.60E+08	55	0.7	60%	5.62	1.78E+08
1.0 µm CMOS FPGA (RH1020)	0	3.97E+07	55	0.7	60%	23.05	4.34E+07
0.8 µm CMOS FPGA (RH1280)	1	9.16E+07	55	0.7	60%	22.04	4.54E+07
0.8 µm CMOS FPGA	0	2.05E+08	55	0.7	60%	4.47	2.24E+08
0.6 µm CMOS FPGA	0	1.82E+08	55	0.7	60%	5.04	1.99E+08
0.6 µm RT54SX CMOS FPGA	0	2.29E+07	55	0.7	60%	39.88	2.51E+07
0.45 µm CSM CMOS FPGA	1	1.03E+08	55	0.7	60%	19.62	5.10E+07
0.45 µm UMC CMOS FPGA	0	2.56E+07	55	0.7	60%	35.79	2.79E+07
0.35 µm CMOS FPGA	0	6.31E+07	55	0.7	60%	14.51	6.89E+07
0.25 µm MEC CMOS FPGA	2	7.51E+07	55	0.7	60%	41.40	2.42E+07
0.25 µm Infineon Flash CMOS FPGA	0	3.62E+07	55	0.7	60%	25.30	3.95E+07
0.25 µm UMC CMOS FPGA	0	7.78E+08	55	0.7	60%	1.18	8.5E+08
0.22 µm UMC CMOS FPGA	0	5.13E+08	55	0.7	60%	1.78	5.60E+08
0.22 µm UMC Flash CMOS FPGA	0	6.89E+07	55	0.7	60%	13.28	7.53E+07
0.15 µm UMC CMOS FPGA	2	4.41E+08	55	0.7	60%	7.04	1.42E+08
0.13 µm Infineon Flash CMOS FPGA	0	4.38E+08	55	0.7	60%	2.09	4.78E+08
0.13 µm UMC Flash CMOS FPGA	1	2.57E+08	55	0.7	60%	7.87	1.27E+08

Notes:

1. *Please refer to the "0.25 µm UMC FPGA Reliability Summary" section on page 33 for RTSX-SU antifuse FIT rate reliability data.*
2. *Technically, mean time between failures (MTBF) should be used only in reference to repairable items, while MTTF should be used for non-repairable items. However, MTBF is commonly used for both repairable and non-repairable items, hence MTTF or MTBF = 1/FIT.*

Table 9: Microsemi Reliability Summary & FIT Rate by Device Technology

5.3.5 Risk Minimisation of Antifuse Failures

Antifuse instability can cause field failures if a deployed device contained damaged antifuses. If the antifuse is being used to tie a gate high or low, the damaged antifuse will still serve to hold its gates at the proper logic levels. The signal propagation and switching speed of a CMOS logic circuit, however, are functions of the line resistance and load capacitance. In a high-speed circuit, the damaged antifuse's unstable resistance can create variations in circuit timing. The delay can change from nanoseconds to microseconds, leading to field failures that are difficult to diagnose.

Excessive operating current through the antifuse is the typical cause of damage. DC current density has an influence on the mean time to failure for programmed antifuses. The cross sectional area of the pathway is a function of the programming current and programming algorithm along with the height, width and polarity of the programming pulses, and is typically a hundred nanometers squared. Increasing the current density through the programmed antifuse strongly accelerates the failures. This strong dependence also means that reducing the operating current can significantly increase the lifetime of the programmed antifuse.

Such DC currents do not often occur in the normal operation of an FPGA. Typically, the programmed antifuse in a design connects a CMOS driver circuit to a capacitive network. In this arrangement, only AC capacitive currents flow through the programmed antifuse. The peak AC current which is a function of the switching frequency, load capacitance, antifuse resistance, and driver output, can stress the programmed antifuse and result in failure over time. Controlling the operating conditions at the programmed antifuse is only one step that can be taken to make the most of device reliability. There are also factors during the logic design, design routing, antifuse program sequencing, and testing that can affect reliability. Proper care can reduce the likelihood of damaging a programmed antifuse.

The first step in reducing the likelihood of damaging a programmed antifuse involves design. During logic design, following a few simple rules can help ensure reliability by avoiding risky situations. To prevent inadvertent programming of antifuses during normal operation, for instance, no antifuse should be directly connected to any external signal or power bus. Noise on external signal or transients on the power and ground buses can create a high enough voltage across an unprogrammed antifuse to initiate programming.

Testing should screen 100% of the unprogrammed antifuses at the wafer level to ensure they will not program below a certain voltage and that they will remain in their high resistance unprogrammed state. A similar check at final test should ensure that the unprogrammed antifuses are not damaged during packaging. The wafer level test and the final test should verify that the programming circuitry can pass the proper voltages and currents. A final check should be done on the programmer immediately prior to programming to ensure that antifuses did not become damaged after final test.

Design routing creates the final circuit networks, which in turn determine the effective downstream capacitance for each programmed antifuse. Keeping that capacitance below a set threshold will limit the peak AC current through the programmed antifuse. Thus, design routing software can

reduce the number of antifuses operating at high currents by limiting the downstream capacitance. The router can select less capacitive wire lengths for different speed applications, or buffer large networks to create smaller less capacitive networks. Lowering the number of antifuses operating at high currents increases the programmed part's reliability.

An often-overlooked step is to control the order in which the antifuses get programmed. As the device is being programmed, networks form. Programming pulses applied to one network may capacitively program any antifuses connecting to another network. As a result, the antifuse can become damaged, creating a yield or even a reliability problem. Sequencer software should forbid these cases and finds an alternate sequence. Finally, control of the programming current is critical for ensuring antifuse reliability.

5.4 Microsemi OTP FPGA Programming Equipment

In antifuse FPGAs it is not possible to test that every antifuse will program, therefore a small percentage will fail programming. The objective, however, is that the programmed part is 100% functional once programmed. This is typically achieved by: testing that the required antifuse is in fact programmed, that no nets are left floating and that there are no shorts between nets. The Microsemi programming algorithm serially identifies each antifuse requiring programming and applies a voltage in pulses to program the antifuse. A soak "overprogram" step is performed to ensure that the antifuse is fully programmed and the resistance of the antifuse is uniform across the chip. During programming, the programmer has the ability to ensure that each identified antifuse to be programmed is fully programmed and only that antifuse is programmed, otherwise it identifies the part as a programming failure. There are numerous tests performed before and after every antifuse is blown to ensure correct functionality after programming. For example, a standby Icc measurement is recorded pre-programming and post-programming to ensure that the chip Icc characteristics have not changed due to programming.

5.4.1 Overview of OTP FPGA Programming Hardware

The programming hardware consists of the Silicon Sculptor programmer and socket module. The programmer contains a processor, memory, communication port and different types of pin drivers that are used to generate the waveforms required to program the device. The socket module is a passive part and is used as a routing resource to route the pin driver of the programmer to appropriate pin on the socket module.

Starting with Silicon Sculptor software version 4.62.0, Microsemi has introduced an updated auto-calibration utility for the Silicon Sculptor II and Silicon Sculptor 3 programmers. When self-test is run with no adapter modules attached, the updated software may state that the low end calibration point of Icc is out of range. To correct this situation, the end user needs to repeat self-test after fitting an SM48DB adapter DIP module to the programmer. The enhanced calibration software will then make an automatic adjustment of the low end Icc calibration point internal to the programmer, if it is found to be significantly below its normal 30 mA value. Inclusion of this automatic adjustment in the Silicon Sculptor software may eliminate the need to return the programmer to its manufacturer for calibration tuning. It is noted that all programmers supplied from Microsemi and the original equipment manufacturer, BP Microsystems, are calibrated at the BP factory. Calibration is validated at Microsemi and a calibration certificate, valid for one year, is attached to the programmer prior to shipment. At the end of one year, customers are encouraged to perform the "validation of calibration" tests to allow another year to be added to the certificate. If validation of calibration fails and the newly-introduced automatic calibration does not result in the unit passing, then the unit must be taken out of service.

In addition to the validation of calibration procedure referenced above, it is suggested that self-test be done on the programmer before each and every programming operation, especially if the programmer has not been used for more than several days. When programming multiple times per day and every day, the frequency of applying the self-test procedure may be reduced but should be done at least weekly. With the new auto-calibration routine built into the current software, it is recommended that self-test be performed with an SM48DB adapter module fitted to the programmer to ensure that the benefits of auto-calibration are obtained. It is recommend that the latest version of software is used whenever an auto-calibration of the Silicon Sculptor programmers is performed.

5.4.2 Overview of OTP FPGA Programming Software

The operation of the Silicon Sculptor programming software can be broken into three areas:

1. Download and Check of Programming File

Upon loading of a new AFM file (antifuse map, used to identify which antifuses are to be programmed), the file checksum is computed and compared against an expected value. If an error

is detected, the file is cleared from the buffer to prevent the programming operation. An error is reported, indicating that the file load operation has failed. The operator is required to intervene. In most cases, corruption in the programming file cannot be fixed and requires the operator to generate a new programming file.

2. Application of Programming Waveform to Part

Device specific algorithms control the power supply sequence, signal and supply timing, and voltage levels applied to the device. These algorithms are thoroughly verified through observation of each operation on a digital oscilloscope. Algorithm changes are governed by procedures that call for requalification of the algorithm if major changes are made to timing and/or voltage levels.

3. Programming Checks Performed

A device ID code check is run on each device to ensure that the device matches the AFM loaded. A blank check verifies that the device has not been previously programmed or is a programming failure. During programming, each programmed antifuse resistance is checked multiple times under different voltage conditions. At the conclusion of programming in each device row (channel) an End of Channel test is run to verify that no unintentional antifuses were programmed in that row. Once all rows have been programmed, the End of Programming tests are run which check for net shorts and additional unintentionally programmed antifuses. Standby Icc tests are performed before and after programming to verify the integrity of the device. Once all tests have passed, the checksum and Pfuse (which enables device operation in user mode) are programmed and then verified.

5.4.3 Frequently Asked Questions on Silicon Sculptor Test, Calibration and Diagnostics

Question 1: Is there any confirmed experience with parts that have been correctly programmed according to the Silicon Sculptor programming report but later were determined to deviate from the fuse file (this excludes all design errors)?

Answer 1: One instance of an unintentionally programmed antifuse escaped the test sequence on the Silicon Sculptor programmer, resulting in a stuck-at functional failure. The End of Programming (EOP) test sequence was modified as a result and revised Silicon Sculptor

programming software was rolled out to Microsemi customers (PCN 1019 and Addendum, http://www.actel.com/documents/PCN1019_Addendum.pdf)

Question 2: In the event of an antifuse programming failure, is there a flag programmed into the failed device that marks it as a programming failure and allows the programmer to recognise it as such when reinserted for another programming attempt?
Answer 2: There is no flag programmed into an FPGA which fails to program. However, the blank check or Icc/EOP tests will detect that programming had previously been attempted on a part.

Question 3: What is the scope/coverage of the Silicon Sculptor self-test in terms of HW modules/IFs/Firmware?
Answer 3: The Silicon Sculptor Diagnostic test will verify that the Technology Adapter, motherboard, power supply, pin drivers and communications are operational. It should be noted that the Silicon Sculptor Diagnostics will not test the Technology Adapter if there is no socket module installed. If a socket module is installed then the Technology Adapter and the socket module circuitry will also be tested to ensure proper operation.

Question 4: Is it only a pass/fail message returned to the user or is the programmer responding with a differentiated failure message/code in the event?
Answer 4: Diagnostics will list an output of all the pass or failures for each subtest component and provide a final PASS or FAIL condition at the end of the test.

Question 5: How does the calibration work?
Answer 5: Verification of calibration is available during diagnostics with the proper socket module (SM48D). Calibration of the site can be verified but not actually calibrated in the field. An oscilloscope and multimeter are required to perform the verification of calibration.

Question 6: Which parameters are calibrated?
Answer 6: No actual user calibration can be performed in the field. Instead, the verification of calibration will verify the accuracy of our diagnostic test. More details about calibration can be found in the document: BPWinCalibrate.pdf
http://www3.bpmmicro.com/web/helpandsupport.nsf/69f301ee4e15195486256fcf0062c2eb/9f1320b2ddb6145e862578fd0058971e/$FILE/BPWin%208th%20Generation%20Verification%20of%20Calibration.pdf.

Question 7: What are the most likely causes for calibration failure?
Answer 7: It is likely that if calibration is failing then the diagnostic test will also flag a specific hardware set as failing. The possible failures, if calibration is out of tolerance are many. It could be power supply, pin driver, regulator, or power supply cabling to name but a few.

Question 8: Is the programmer equipped with a software self-test function (e.g. for detecting incomplete/invalid configurations or file corruptions, etc.)?
Answer 8: Yes. While loading the programming file, the file checksum is calculated and compared against the expected value. If a mismatch is detected an error is reported and the loaded file is cleared from the programmer buffer to prevent the user from performing the programming operation.

5.4.4 Reliability of OTP FPGA Programming Equipment

Reliability of the Silicon Sculptor programmer can be inferred from the absence of failures in programmed Radiation Tolerant FPGAs which have been subjected to high temperature operating life tests after being programmed on the Silicon Sculptor programmer. Microsemi has tracked the number of device-hours of reliability testing performed on RT FPGAs with each silicon sculptor software revision since version 3.89. A summary of reliability testing is presented here. Further details can be obtained from Microsemi on request.

12 Most Recent Releases		Top 12 by Device-Hours	
Silicon Sculptor Software Version	**Device-Hours**	**Silicon Sculptor Software Version**	**Device-Hours**
V5.22.0	330,608	V4.68.1	561,704
V5.18.1	2,856	V5.6.0	411,056
V5.18.0	96,464	V5.22.0	330,608
V5.14.1	180,080	V5.2.0	249,688
V5.12.1	85,536	V5.14.1	180,080
V5.12.0	22,384	V4.80.0	160,368
V5.10.1	14,000	V5.8.1	109,520
V5.8.1	109,520	V5.18.0	96,464
V5.6.0	411,056	V5.12.1	85,536
V5.4.1	66,848	V4.78.0	80,000
V5.2.0	249,688	V4.70.1	75,376
V4.80.0	160,368	V5.4.1	66,848

Table 10: Reliability Device Hours by Silicon Sculptor S/W Version

The reliability tests shown in Table 10 were performed on RTSX-SU and RTAX-S/SL devices. Test hours are accumulated through device qualification tests, on-going reliability tests, and enhanced lot acceptance (ELA) tests which require a specific number of devices to be programmed and tested before accepting each RT FPGA wafer lot for assembly, test and shipment to customers.

Until recently, customers could return Silicon Sculptor programmers directly to the manufacturer (BP Microsystems). In such cases, Microsemi may not have received notification from either the customer or BP Microsystems, therefore failure rates and root causes have not been tracked. New procedures require BP Microsystems to refuse to accept direct customer returns and instead all returns must be administered by Microsemi so that accurate failure rates and associated root causes can be tracked.

5.4.4.1 Qualification of Programming Software

Qualification is required for any programming algorithm update that results in changes to programming voltages or timing. The qualification is performed on all affected devices with sampling criteria to give an LTPD-5 for major changes and LTPD-3 for new programming algorithms. In addition to the programming software qualification, an Enhanced Lot Acceptance (ELA) sample test is performed on all RT FPGAs, utilising the latest released programming software version. Therefore all releases of programming software are used to program RT FPGAs, regardless of whether or not each version contains changes which affect programming of RT FPGAs.

For the purposes of qualification, changes to software are considered to fall into three categories – New, Major Change, Minor Change.

New: A newly developed algorithm for a new technology or foundry.

Major: A change of greater than 10% to waveform timing, programming pulse count, programming voltages, DC current tests, DC voltage tests or an increase in LVGOX stress of >100mV. Any change to any programmer hardware in the circuits that apply or measure voltages or currents. Any change to Antifuse programming or soak polarity. Any change to antifuse programming order, blank check test voltages, end of channel test voltages and end of programming test voltages if they exceed levels currently used in manufacturing test.

Minor: Any change to data shifting, ID code readback, silicon signature readback, checksum readback. Any change to how errors are displayed , the GUI or interface, blankcheck, EOC and EOP tests not listed above.

New, Major and Minor Changes are qualified with the following sample sizes using the stress tests and sample sizes as indicated in Table 11.

		New	Major	Minor
Antifuse	HTOL	0/76*	0/45	N/A
	LTOL	0/76*	0/45	N/A
	Thermal Shock**	As applicable	N/A	N/A
	Temperature Cycle	0/76*	0/45	N/A

Table 11: S/W Qualification Sample Sizes

Minor changes are tested by performing programming and functional yield analysis of affected products using LTPD of 10. The programming software is designed so that every family of devices has its own set of code residing in specific files. During regression testing, there are tools in place to compare the source code of all the programming modules with the previous software release to make sure that there are no unintentional changes.

5.4.4.2 Root Causes of Programming Failures

There are several factors that could potentially generate a programming failure. These errors can be split into two categories:

1. Setup issues.
   a. If the operator does not follow the procedure recommended by Microsemi to ensure the integrity of their programming hardware, programming failures could occur if the hardware is faulty. The error messages reported depend on the specific problem with the programming hardware.

2. Device issues.

b. Because of the nature of antifuse technology, a programming yield loss is expected. There are two main errors that could occur during programming related to the device.
   i. Antifuse time out failures caused by the programmer not being able to program the addressed antifuse.
   ii. Pre-/post-programming standby Icc, End of Channel (EOC) or End of Programming (EOP) failures, normally caused by programming an extra antifuse.

5.4.5 Users Return of Experience on Microsemi Programming Equipment

In the following paragraphs, programming issues which have been encountered by Thales Alenia Space, Astrium and Tesat are described.

5.4.5.1 Thales Alenia Space - Return of Experience

5.4.5.1.1 Designer Software Releases

Even if this is not directly part of the programming equipment, Thales Alenia Space considers that the design software shall be dealt with under the programming aspects of the FPGA devices. The software defines the allocation of the different antifuses and antifuse types, to implement the design inside the device, and is therefore directly linked to the programming equipment.

The Designer software is regularly updated by Microsemi. The frequency of these updates generates significant constraints for users (software installation, additional programming file generation, ...). In 2012, Thales Alenia Space has noted a significant reduction in the number of Designer software releases.

2012 : up to now, 1 release of Libero IDE (Designer is included)
2011 : 5 releases
2010 : 4 releases
2009 : 4 releases
2008 : 9 releases
2007 : 10 releases
2006 : 6 releases

5.4.5.1.2 Silicon Sculptor Software Releases

As Designer software, the Silicon Sculptor software is regularly updated by Microsemi. Similarly, this generates significant constraints for users (software installation for example). In 2012, Thales Alenia Space has noted a significant reduction of Silicon Sculptor software releases.

2012 : up to now, 3 releases
2011 : 7 releases
2010 : 7 releases
2009 : 5 releases
2008 : 9 releases
2007 : 8 releases
2006 : 7 releases

It is worth mentioning that the users are requested to use the latest update of this software (both Designer and Silicon Sculptor) in order to get support from Microsemi in the case of any issues encountered. In addition, it should also be highlighted that many of these S/W release updates do not even apply to RT devices.

5.4.5.1.3 Silicon Sculptor - 2 Malfunctions:

In 2004, Thales Alenia Space encountered some programming problems on an RT54SX72S device. As a resolution of the issues, Microsemi ultimately replaced the equipment although no explanation was provided by Microsemi on the problem root cause. In early 2007, similar problems occurred on a number of A54SX72A FPGAs. In this instance, the situation was resolved by switching from the Silicon Sculptor 2 to the Silicon Sculptor 3. No new problems have appeared since using Silicon Sculptor 3.

5.4.5.1.4 Silicon Sculptor Software Issues /Enhancements:

Down through the years, Microsemi has published many PCNs on Silicon Software issues and enhancements. Such PCN are available on the Microsemi/Actel website, while some of these have been considered critical enough to justify ESA Alerts:

- PCN-0705 (classified as Minor): Introduction of an Auto-Calibration Routine in Self-Test for Silicon Sculptor (II and 3) Programmers. Refer to ESA Alert EA-2007-EEE-01.
- PCN-0718 (classified as Major): Programming issue in Silicon Sculptor v4.68.0. See ESA Alert EA-2007-EEE-07.

5.4.5.1.5 ESD issue on programming adapters, PCN 0512:

In September 2005 Microsemi informed its customers of an issue with the programming hardware. It had been discovered that the removable lids of the two-piece adapters used for some ceramic CQFP packages could accumulate ESD charges of over 2,000V. A lid exchange program was set up. This issue was not minor, especially as it was followed PCN-0502 of April 2005 which informed customers about the extreme ESD sensitivity of the RT54SX-S and RTSX54-SU families.

Table 12 indicates Thales Alenia Space programming yield numbers by Microsemi FPGA family.

	FAMILY						
	ACT1	ACT2	ACT3	RT54SX	RT54SX-S	RT54SX-SU	RTAX-S
Antifuses type	ONO BAE Systems	ONO Matsushita	ONO Matsushita	M2M Matsushita	M2M Matsushita	M2M UMC	M2M UMC
Programmed	100	134	74	253	64	241	74
Rejected	15	5	2	19	3	8	5
Programming yield	85%	96.3%	97.3%	92.5%	95.3%	96.7%	93.2%

Table 12: Thales Alenia Space Programming Yield

5.4.5.2 Astrium - Return of Experience

In 2006 four failures were discovered on RTSX72SU-1CQ256 flow “B” FPGAs during first functional tests. The parts were programmed using Silicon Sculptor II programmer with programming software release 4.55. Different investigations performed by Astrium and Actel demonstrated that:

- A default in the Silicon Sculptor II had produced unwanted programmed antifuses. The calibration and diagnostic procedure of the release 4.55 was not able to detect the calibration failure.

- The unwanted shorts between one logic module output and Vcc or GND were not detected by Silicon Sculptor post programming verification of the release 4.55.

Astrium returned the Sculptor II programmer to Actel used in programming the RTSX72SU-CQ256B failed devices. The main purpose of the investigation was to find out if there was a correlation between the programmer and the time-zero functional failures observed on the four programmed devices. Although the devices were programmed with programming software release 4.55, Actel had introduced a new programming software release 4.62.0 introducing modified calibration tests of the programmer.

Actel received the Sculptor II programmer and the socket module (SM208CQSX-ACT) from Astrium. Upon receipt of the programmer, the Programmer Diagnostic test was performed on the programmer using the Silicon Sculptor II programming software release 4.62.0. The Sculptor software reported an out of calibration message on the Vcc supply as follows: "*Testing current regulators: Coarse mode Icc regulation faulty or needs calibration (7.998mA should be 30mA)*". The Programmer Diagnostic test was performed one more time to confirm the failure. It also reported the same out of calibration message as follows: "*Testing current regulators: Coarse mode Icc regulation faulty or needs calibration (8.172mA should be 30mA)*"

It was possible and most likely that this particular programmer may have caused the functional failures that Astrium had experienced in the past. Because the Vcc driver controls the device power pins during antifuse programming and testing, it must be accurate and stable to ensure antifuse reliability after programming. The programming software release 4.55 was not able to detect this failure of calibration of the Silicon Sculptor programmer.

Programming of Microsemi/Actel devices using Silicon Sculptor II consists of two main processes: programming the antifuses and running End of Programming (EOP) tests. The EOP tests consist of a number of checks which confirm the integrity of the part. Since high voltages are involved during programming, it is possible that in a very small number of cases, the device may be overstressed. A consequence of this is that there may be unwanted shorts in the design. One function of the EOP tests is to check for these shorts. If any shorts are detected, the device is designated a programming failure. Microsemi/Actel discovered that there was one class of potential shorts which could escape the EOP tests. These were signal tracks inadvertently shorted to Vcc or GND. Therefore, Silicon Sculptor could claim the part was programmed correctly, but once the part was put on a PCB, it would fail immediately since one

of the active signal nets had been shorted to Vcc or GND and would not operate. An Enhanced Integrity Test (EIT) is included in the latest version of the EOP test software, which is embedded in the Silicon Sculptor programming software. This fully checks for signal tracks inadvertently shorted to Vcc or GND. This is included in Silicon Sculptor software version WIN 4.60.2 and later.

It was concluded that in the case of Astrium, the root cause for the subject failure was a programming fault that was not detected by Silicon Sculptor II programming software version 4.55 during programming. Actel performed trials on this particular device using the programming software version 4.59.2 or later and the results showed that the software detects the failure at programming. The additional test coverage in this version of the Silicon Sculptor II programming software added coverage for stuck at 1 (VCCA) faults. Burn-in and post burn-in testing on ATE would eliminate the possibility CMOS damage. The new software will detect this type of failure during programming and the device will be rejected as a programming failure. This experience confirmed to Astrium the importance of the software and hardware programming tools in the quality of the flight FPGA and the need of a qualification process for programming tools. It is recommended by Astrium that this programming tools qualification follows a quality process that warrants the capability of the tools to produce good and reliable FPGA devices.

5.4.5.3 TESAT Spacecom - Return of Experience

5.4.5.3.1 Silicon Sculptor 2 malfunctions:

On February 24th 2010 TESAT experienced failure messages when performing self-tests on a Silicon Sculptor II with an SMAX208PQACT inserted, using programming software BPWin V4.72.1. Repeated self-tests of the programmer resulted in a PASS after 3 failed attempts. Due to this situation the programmer was not used but calibrated on March 9th 2010. On March 11th 2010 TESAT again experienced a failed self-test which disappeared on the second trial. A blank check on an RTSX32SU-CQ208EX3 then failed with the error message "*Excessive current detected. The protection circuit has shut off the power*." and an internal investigation was started (TESAT internal case number PB64338).

The main topics which were focused upon included:

1. Investigation on failed blank check of the RTSX device. The result was, that due to selecting a wrong package type the blank check failed. Selecting the correct package type later showed that the device was blank and it was possible to successfully program the device. However, due to the failed blank check Microsemi recommended not to use the device for flight as it might have been overstressed.
2. How to proceed when self-test failures occur? It was assumed that self-test failures may occur due to contact problems when the test is performed with an adapter inserted. Therefore, an interim procedure containing self-tests and blank tests was set up to be performed prior to programming a FM part (details also described in TESAT internal case number PB64338). In parallel, options for Silicon Sculptor and Adapter maintenance were evaluated. It should be noted that apart from calibrations that can be performed the programming equipment can only be returned to BP Microsystems for repair. As no official procedure from Microsemi had been available on how to proceed with self-test failures, TESAT decided no longer to use the Silicon Sculptor II and to switch to new Silicon Sculptor 3 equipment.

5.4.5.3.2 Silicon Sculptor 3 malfunctions:

TESAT has not experienced any unexpected behaviour with the current Silicon Sculptor 3 equipment which it uses. So in summary, apart from bad handling of devices TESAT experienced self-test failures of Silicon Sculptor 2 equipment which resulted in excluding this equipment from FM programming. Since transition to Silicon Sculptor 3 no self-test failures have been observed by TESAT.

5.4.6 Programming Best Practices

5.4.6.1 Microsemi Recommended Programming Best Practices

The following documents contain guidelines and recommendations for programming Microsemi FPGAs. References to ESD protection and the use of uninterruptible power suppliers are included. Guidance is provided on the frequency of programmer self-test and calibration verification operations.

http://www.actel.com/documents/SiliSculptQuickRef.pdf

http://www.actel.com/documents/SiliSculptProgCali_UG.pdf
http://www.actel.com/documents/radhardPG_UG.pdf
http://www.actel.com/documents/RTAX-S_Programming_Guide_AN.pdf

5.4.6.2 Astrium Programming Best Practices for Microsemi Devices

5.4.6.2.1 Programming Procedure

Each operation of the programming shall be described in a procedure.

5.4.6.2.2 Programming Tools

1. The reliability of the programming shall be demonstrated. A lot acceptance test performed on parts coming from the flight lot, programmed using the same model of programmer and same programming software version, should be done to demonstrate the reliability of the programming

2. The type of FPGA programmer and programming software version which was used to program the qualification FPGAs shall be used to program all production FPGAs.

3. A process of survey shall ensure that any change of the programmer and software communicated by the FPGA manufacturer/vendor are taken in account and assessed for potential impact.

4. Any change of the programming setup may directly affect the reliability of programmed FPGAs.

5. If a new model of programmer is planned to be used and which is different from the model used for programming the qualification FPGAs, then a delta qualification of the FPGA shall be undertaken in order to validate the new model of programmer for production of flight FPGAs.

6. If the new version of the programming software is planned to be used and which is different from the version used for programming the qualification FPGAs, then a delta qualification of the FPGA shall be undertaken in order to validate the new version of the programming software for production of flight FPGAs.

7. A formal status from the FPGA manufacturer on the new programmer or software shall be recorded.

8. A validation procedure shall be run in order to validate the setup of the programmer and its software before programming any flight parts. The procedure shall be run after any change in the setup including the software release. A record of the validation shall be performed.

9. Device programming shall be performed in a cleanroom.

10. All protection again ESD for 100V susceptible device shall be ensured. The efficiency of the protection shall be measured and shall be recorded.

11. Programming shall only be performed by an operator who has received specific training. The training shall cover ESD risk, EEE handling and the programming of flight parts. The training shall be validated by a certification for the programming of flight parts.

12. The programmer must be supplied by an Uninterruptible Power Supply. The configuration of the UPS shall be an online UPS (sometimes called a true UPS) in order to avoid any loss or perturbations of programmer power supply during loss of utility power or when line voltage varies outside normal limits.

13. The access to the programmer must be limited to qualified and trained operators. Programming of development/engineering parts shall also be performed only by qualified and trained personnel.

14. Each operation of the programming and post-programming screening shall be recorded in a programming report.

5.4.6.2.3 Calibration and Verification of the Programming Tools

1. The programming socket shall be periodically inspected (under high magnification).

2. A calibration of the programmer shall be performed at least every day where the programming HW is used. The calibration shall be record in the programming report.

3. The method of calibration shall include:

    - Functional verification of the programmer.
    - Measurement of the critical electrical parameters of the programmer.

4. The verification of the programming setup could be improved by the programming of an EM part as the first step of the programming campaign.

5. The programming file shall be generated from FPGA manufacturer approved tools.

5.4.6.2.4 Configuration and Marking

1. Each programmed part shall receive a serialisation number. A link with the manufacturer serial number is kept in order to maintain traceability.

2. A method of configuration shall guarantee the programming file used for the programming.

3. The marking shall include the configuration data of the design and the serial number of the part.

4. The marking shall be performed before the programming of the part. A verification of the conformity shall be conducted after programming.

5. Checksum verification is recommended to be used to ensure correct programming file usage.

5.4.6.2.5 Programming

1. All programming files and log files shall be stored for each programmed part.

2. In case of a programming failure, an analysis shall be carried out if the number of failures for each lot/date code which is programmed on the same programmer calibration exceeds the manufacturers recommended limits. If no such recommended limits are available, then a limit of 5% shall be used.

3. Each failure during programming must be investigated and the fault traced.

5.4.6.2.6 Programming Review Board

1. Analysis and corrective actions shall be performed for each failure after programming.

2. A Programming Review Board shall be in charge of the acceptance of the programmed parts following end of post programming tests.

5.4.6.3 Thales Alenia Space Programming Best Practises for Microsemi Devices

The Thales Alenia Space position on FPGA programming activities can be detailed as follows:

- Programming operations shall be documented in procedures.
- Only trained personnel shall be allowed to program flight FPGAs.
- Software version used for programming shall be recorded against the Serial Number of the programmed part.
- Periodic calibration of the programming hardware shall be performed and recorded (see the part manufacturer recommendation for calibration periodicity).
- Cleaning and visual inspection of the programming socket shall be periodically performed.
- Auto-calibration and auto-test shall be run at the beginning of each programming campaign or prior to each programming operation (depending of FPGA type; follow the part manufacturer recommendations).
- Power line supplying the programming hardware shall be filtered and protected (Uninterruptible Power Supply - UPS). Follow the part manufacturer recommendations.
- Programming area shall be classified as an ESD Protected Area (EPA).

Additionally, Thales Alenia Space suggests, as requested several times in the past, that Microsemi sets up a separate programming software configuration specifically for space users. Furthermore, the applicability of the updates to lots and/or date codes, if any, should be detailed by Microsemi.

5.4.6.4 Thales CS Programming Best Practises for Microsemi Devices

The Thales CS position on FPGA programming activities can be detailed as follows:

- Flight FPGAs program by trained personnel following Thales CS procedures.
- Annual calibration of the programming equipment, auto-test is performed for each programming campaign.
- Perform FPGA programming in an ESD protected area.

5.4.6.5 FPGA PPBI WG : ESCC REP-010 Programming Best Practises

Based on inputs from the various WG stakeholders, RD-10 highlights the recommended high-level programming best practises for OTP Microsemi FPGA devices, which include but are not limited to:

- Incoming control, storage management, device traceability and programming operations of the OTP FPGA devices shall be documented in procedures.
- Only trained personnel shall be allowed to program flight FPGAs.
- A method of configuration shall guarantee the programming file used for the programming. Verification of the conformity shall be performed after programming.
- Software version used for programming shall be recorded against the serial number of the programmed part.
- Calibration verification of the programming hardware shall be performed and recorded. Refer to the manufacturer's recommendation for calibration periodicity.
- Self-diagnostic shall be run at the beginning of each programming campaign or prior to each programming operation (depending on FPGA type). Refer to the manufacturer's recommendation concerning self-diagnostic.
- Cleaning and visual inspection of the programming socket shall be periodically performed.
- Power line supplying the programming hardware shall be filtered and protected (i.e. use of on-line UPS (Uninterruptible Power Supply)). Manufacturer's recommendations to be followed.

- Programming area shall be classified as an ESD Protected Area (EPA).
- A Programming Review Board shall be in charge of the acceptance of programmed parts.

5.5 PPBI Data Review

5.5.1 Microsemi/Actel & Serma Technologies PPBI Service

5.5.1.1 Electrical Test Conditions

Tested parameters:

There are two methods depending on the customer's request:

"Design related" method (TAS/Serma Technologies flow):

A dedicated test program is developed for each design, based on the simulation VCD file provided by the user. This allows performing a full functional characterization and the test of all the DC parameters (VOL/VOH, IIL/IIH, IOZL/IOZH, ICC, VIL/VIH). AC parameters are not measured. This method had been used for about 70% of the tested FPGAs up to end 2011.

- "Generic method" (Astrium/Actel flow):

A universal test program is developed for each device/package combination. The specific design functionality is not checked. JTAG instructions are used for positioning the DUT pins for DC tests (ICC, IIL/IIH, IOZL/IOZH). The AC parameter “bin delay” is measured (using confidential information delivered by Microsemi). This method had been used for about 30% of the tested FPGAs up to end 2011.

Test temperature:

All the parts are tested at -55°C, +25°C and +125°C after burn-in. Most often, the pre burn-in measurements are performed at -55°C, +25°C and +125°C. In some cases (less than 5% of the tested parts), the initial measurement is only done at +25°C. In all cases, the drifts between the initial and final measurements at 25°C are calculated after burn-in, and compared to the SMD specification limits.

5.5.1.2 Burn-in test conditions

Polarisation mode:

The burn-in tests are performed in "pseudo-dynamic" mode, with clock signals applied throughout the test. If requested, reset pulses are applied to the parts after power-up, or at regular intervals. All other inputs are statically referenced to ground or power supply by pull-down/pull-up resistors.

Some users implement a specific built-in design in order to activate the maximum of functions during the burn-in and, then, get closer to a full dynamic burn-in. But Serma Technologies is usually not informed of this. The observations during the test set-up (I/O activity, operating power supply value) suggest that such test mode is seldom implemented. It is then difficult to say if a "pseudo full dynamic" mode would improve the burn-in efficiency.

Clock frequency:

Most often, the burn-in clock frequency is set at 1MHz or 2MHz. Some users request to run the parts at the same frequency as in the application (up to 20MHz). No failure during or after burn-in has been observed, nevertheless, less than 10% of the parts have been tested this way.

Duration:

Burn-in duration is either 168h or 240h (50% - 50%). In rare cases, the duration has been decreased to 96h, mostly for delivery time constraints.

Temperature:

Burn-in is performed at +125°C (even for RTAX parts).

5.5.2 Other Non-Microsemi/Actel PPBI Services

5.5.2.1 Thales Alenia Space

Before describing the different approaches applied by Thales Alenia Space, it shall be underlined the following points:

- No specific PPBI activity has been performed on the oldest FPGA families (A1020, RT1280/RH1280, RT54SX16/32),
- Thales Alenia Space Italy started to perform PPBI activities after the MEC issue identification on SX-S devices,
- The PPBI activities were defined on design and/or program/customer requirements/constraints.

5.5.2.1.1 PPBI on Board/Unit During Integration

Has been applied to device types:

- RT54SX32S / RT54SX72S
- RTSX32SU / RTSX72SU (hundreds of SX-S ans SX-SU parts)
- RTAX2000S/SL (some tens of parts)

No PPBI activity was performed on the devices at component-level after programming. The post-programming of the devices at board/unit level was of the order of 300h at maximum allowable unit temperature (60/70°C) at the unit integration phase. This corresponds to about 72h at 125°C, using Arrhenius regression with an activation energy 0.4eV (although the validity of this value remains questionable…). In some cases a log file including the total accumulated functional time (up to 1000h) is provided.

Pros:

- minimised handling of FM devices.
- reduced impacts on the program schedules.
- devices tested/stimulated in the real application environment.
- applicable without problems to classified programs.

Cons:

- delayed screening/verification (big impacts on the programs in case of failure)
- no possibility to perform device dedicated electrical measurements.

Results:

- hundreds of devices, no issue related to FPGA antifuse problems until now.

5.5.2.1.2 Post Programming Microsemi/Serma-like

Has been applied to device types :

- RT54SX32S / RT54SX72S
- RTSX32SU / RTSX72SU (hundreds of SX-S and SX-SU parts)
- RTAX2000S/SL (some tens of parts)
- (Aeroflex UT6325)

The post programming of these devices was performed "in-house" in TAS-Milan or in Microtest test house facilities. The post programming burn-in was performed in accordance with the Thales Alenia Space Italy procedure which includes:

- initial electrical measurements.
- 168/240h of pseudo-static burn-in (only clock signals activated) at 125°C.
- final electrical measurements.

The electrical measurements included continuity, leakage, static and dynamic power consumptions, at three temperatures, when performed at Microtest. The electrical measurements included only static and dynamic power consumptions when the tests were performed in house. These measurements were performed in some cases at three temperatures, in other cases only at ambient temperature.

Pros:

- the tests in-house can be scheduled and managed better than in the test house.
- in both cases of in-house or test house post-programming, no functional test is required, so no additional design activity is required.

Cons:

- functional verification delayed to integration phase.

Results:

- Hundreds of Microsemi devices, no issues related to FPGA antifuses problems until now.
- For Aeroflex devices, see Section 5.5.5.

5.5.2.1.3 PPBI Pilot Project for Italian Program (Pseudo-Dynamic BI)

Has been applied to device :

- RTAX2000S (1 part)

The post programming activity has been performed in Microtest on one device to be used only for this test purpose. The post programming was according to Thales Alenia Space Italy procedure including:

- electrical and functional verification at 3 temperatures (-55, 25, 125°C).
- 240 hours of pseudo-dynamic burn in (clocks and about 16 inputs activated, about 32 outputs monitored, at reduced frequency, using specific test vectors) at 125°C.
- electrical and functional verification at 3 temperatures (-55, 25, 125°C).

Pros:

- pseudo-dynamic BI allows to stimulate a subset of antifuses during BI (more effective than pseudo-static BI with only clocks activated).

Cons:

- too high design effort (double pattern generation, one for functional verification, the other for stimulus during BI).
- too high economical effort with respect to the toggling coverage that is possible to obtain (not enough I/O can be controlled with respect to the pins available for the device, double HW and SW developments required in test house).

Results:

- Successful with no issue related to FPGA antifuses problems.

5.5.2.1.4 Post Programming without Burn-In, as per NASA/JPL Requirements

Has been applied to device type:

- RTAX2000SL-1 (2 parts)

The post programming activity has been performed in Microtest. According to NASA/JPL requirements, the following post programming activities were performed:

- electrical and functional verification at 3 temperatures (-55, 25, 125°C)
- about 300h of functional testing accumulated during the Unit integration phase

Pros:

- reduced test time duration (only one day is enough for post programming if the development and debugging operations are scheduled in time).
- functional/electrical verification before mounting the device on the final board.

Cons:

- reduced post programming screening provided at component level (the screening is performed at Unit level during integration through extended functional testing).

Results:

- No issue related to FPGA antifuses problems.

5.5.2.1.5 Sentinel-1 Screening Flow

Has been applied to device types:

- RTAX2000S-1 CGA624 (20 parts)
- RTAX2000S-1 CQ352 (16 parts)
- RTAX250S-CQ208 (4 parts)

In the frame of the Sentinel-1 program, the following post programming screening flow was proposed by Thales Alenia Space Italy and agreed by ESA. The activities were performed in

Microtest for the RTAX2000S-1 CQ352 devices and in Serma Technologies for the remainder. The proposed flow arose from the need to find a way to screen parts after programming the devices with the CGA624 package, which cannot be post-programmed according to current ESA requirements due to column oxidation during exposure to the high temperature of the burn-in. The flow was extended to the CQ packaged devices, based on the fact that the current flowing through the antifuses is considered an effective way to detect their possible weakness.

The activities performed included:

- electrical and functional verification at 3 temperatures (-55, 25, 125°C).
- 8h of functional toggling test (net toggling verified through simulation design tool, higher than 70%) at ambient temperature at the highest possible frequency (80 MHz in our case).
- electrical and functional verification at 3 temperatures (-55, 25, 125°C).

In the beginning the toggling test was required at -55°C (considered a worst case condition) but unfortunately this was not feasible due to condensation problems during the test.

Pros:

- reduced post programming test time/cost effort.
- possibility to have objective toggling coverage data/requirement (through available design tool) that is to say possibility to compare results related to different designs/projects.
- reduced managing of the devices (only one test board is used).
- can be applied to any available package.

Cons:

- no possibility to apply the screening pattern for longer time period, due to cost constraints (the test machine must be dedicated to the single device, the temperature variations are managed through thermostream).

Results:

- No issue related to FPGA antifuses problems.

5.5.2.1.6 Specific Commercial Telecom Project Screening

Has been applied to device type:

- RTSX72SU CQ256 (30 parts)

The customer required the procurement of components at the highest available quality level and a proposal for post-programming alternative to the actual requirement, considering the activity at component level too risky (possibility to damage the components during the handling). The screening was moved to board level which included a dedicated test sequence.

A dedicated test pattern was generated from the test equipment. Due to the high reachability and observability (possibility to stimulate most of the inputs and to monitor most of the outputs from the board interfaces) of the device at unit level, the pattern allowed a toggling coverage (verified through the design tool) higher than 90%.

The pattern was applied to the device for 168h, at ambient temperature, monitoring the output signals from the board. A (desired) collateral effect of this test was the early discovery (during the test set up debug with the EM device) of a design error on a device that had to be used with different configurations on different units.

Pros:

- minimised handling of FM devices.
- reduced impacts on the program schedules.
- devices tested/stimulated in the real application environment.
- objective pattern toggling coverage data available.
- screening performed in the first board debugging phases.

Cons:

- reachable pattern coverage dependant from the specific application (device/board design).
- only functional verifications performed (no FPGA dedicated electrical measurements are possible on board).

Results:

- No issue related to FPGA antifuses problems.

5.5.2.1.7 Thales Alenia Space Conclusion

More than one hundred RTAX devices, many hundreds of RTSX devices and nine Aeroflex devices have been subjected to different kinds of post-programming activities as detailed previously. All devices have been found by Thales Alenia Space to have successfully passed all tests.

5.5.2.1.8 Additional Data – Life Test

Has been applied to device type:

- RT54SX72S (4 parts)

In the frame of a commercial telecommunications program (in 2005) and to validate the lot, the HW/SW programming environment and the designs, Thales Alenia Space Italy performed 1000h of life-test on 2 devices (same lot, different designs) according to Alcatel procedure (same as Thales Alenia Space France – Thales Alenia Space was Alcatel at that time), including:

- electrical and functional verification at 3 temperatures (-55, 25, 125°C).
- 1000h of pseudo-static life-test (only clocks activated) at 125°C.
- electrical and functional verification at 3 temperatures (-55, 25, 125°C).

The electrical measurements included continuity, leakage, VOH, VOL, static and dynamic power consumptions.

Pros:

- the validation can be performed independently from the program schedule.
- validation of the lot and the programming environment (HW and SW revisions to be used to program devices coming from a specific lot) is important to guarantee the success of the programming and validity of the programmed FPGA devices.

- minimise handling of FM devices (the activity is performed on devices which shall not be used for flight).

Cons:

- the validation should be performed in advance with respect to the program needs (a failure means lot rejection) when the design is not defined. A meaningful specific design could be used instead of the real one (similar to what is done in Microsemi for lot validation).
- no screening performed on each programmed device (possible weaknesses related to the single device/programming operation, if they exist, are not screened).

Results:

- 4 FM (in flight) RT54SX72S devices from this lot, no issue related to FPGA antifuses problems until now.

5.5.2.2 Thales CS:

Thales CS is a test house which can provide a global solution for PPBI of FPGA and OTP devices. Thales CS applies the current PPBI flow indicated below:

- Programming with Silicon Sculptor 3 or BPM 1610.
- Initial electrical characterisation:
  - the electrical characterisation of components is always performed at 3 temperatures: -55°C, 25°C and 125°C with thermal inducing system.
- Depending on demand, Thales CS can perform:

  Standard test:

  - Continuity test
  - Leakage current measurement
  - Static power supply current measurement.

Full Test: (requiring VCD file or Test Patterns):

- Continuity test
- Leakage current measurement
- Dynamic and static power supply current
- Voltage measurement output (on toggling pins)
- Functional validation
- Research of the maximum functional frequency
- Propagation delay and critical path.

Automatic pattern generation from a VCD:

- Thales CS & CNES has developed a specific software tool to convert simulation results to test vectors.

"Black Box" IP

- Thales CS has developed a black box IP which can be implemented in parallel to the content of the FPGA.
- The black box IP is fully independent of the design but it has to be integrated in the customer design. Depending on the component, the black box IP represents 1-2% of the available gates.
- A pin of the component has to be reserved in the design in order to be able to test the black box IP during burn in.
- This solution does not validate the functionality of the design, but it allows for parametric measurements on FPGAs and enables the verification of the drift induced by the burn-in.
- The black box IP is independent of the user design. The customer can perform the burn-in at its own premises in order to keep the design control.
- The black box IP is still in development at Thales CS and is under licensing patent.

THALES CS black box IP system:

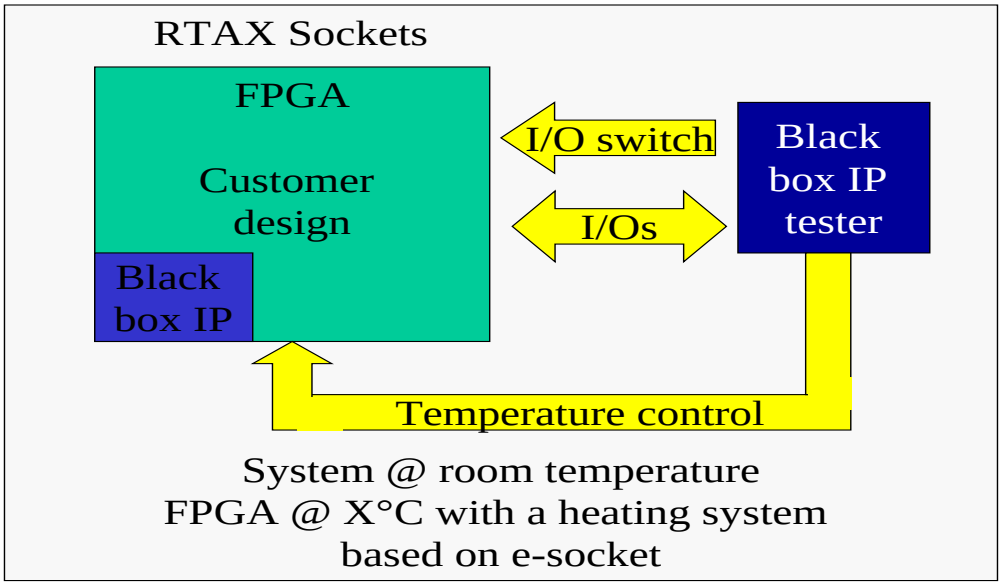


Figure 23: Thales CS Black Box IP System

- Burn-In
  - The burn-in is performed as standard method.
  - A static configuration defined by the designer is applied on components through pull up or pull down resistor.
  - A clock frequency equal to the application is then applied to the component.
  - TCS performed also, full dynamic burn-in on demand.
- Final electrical characterisation at three temperatures.
- Drifts calculations.
- The back box IP represents 1/3% of the available gates but may cover entirely the I/Os of the tested component and can perform the main DC and AC parameter analysis (skew, propagation delay, frequency performance, input and output levels, load, etc).

5.5.3 Microsemi/Actel & Serma Technologies PPBI Service : Data Overview

Table 13 summarises the results of the FPGA PPBI tests by family performed at Serma Technologies since 2004.

Family	Number of tested parts	Number of failed parts				Number of designs
		Global	Pre Burn-in Electrical Test	Post Burn-in Electrical Test	Drift @25°C	
ACT 1	7	0	0	0	0	1
ACT 2	22	0	0	0	0	4
ACT 3	65	**1**	**1 (func)**	0	0	8
RT54SX	19	0	0	0	0	5
RT54SX-S	51	0	0	0	0	11
RT54SX-SU	1250	**2**	0	0	**2 (ΔICCA;ΔICCI)**	117
RTAX-S	681	**13**	**13 (1 func; 12 Icca)**	0	0	67
TOTAL	2095	**16 0,8%**	**14 0,7%**	**0 0%**	**2 0,1%**	

Table 13: Serma Technologies PPBI Data by Family

Table 14 summarises the results of the FPGA PPBI tests by part reference type performed at Serma Technologies since 2004.

Part #	Number of tested parts	Number of failed parts			Number of designs	Number of final users
		Pre Burn-in Electrical Test	Post Burn-in Electrical Test	Drift @25°C		
ACT 1						
RT1020-CQ84	7	0	0	0	1	1
ACT 2						
RH1280-CQ84	3	0	0	0	1	1
RT1280-CQ172	9	0	0	0	2	2
RH1280-CQ172	10	0	0	0	1	1
ACT 3						

RT14100A-CQ256	65	**1** (func)	0	0	8	3
RT54SX						
RT54SX32-CQ256	19	0	0	0	5	1
RT54SX-S						
RT54SX32S-CQ256	34	0	0	0	5	2
RT54SX72S-CQ256	17	0	0	0	6	3
RTSX-SU						
RTSX32SU-CQ84	34	0	0	0	6	2
RTSX32SU-CQ208	146	0	0	0	13	6
RTSX32SU-CQ256	260	0	0	**1** (ΔICCI)	15	8
RTSX72SU-CQ208	139	0	0	0	17	7
RTSX72SU-CQ256	671	0	0	**1** (ΔICCA)	66	11
RTAX-S						
RTAX250S-CQ208	260	0	0	0	10	3
RTAX250S-CQ352	28	0	0	0	2	2
RTAX1000S-CQ352	49	**2** (Icca; Func)	0	0	5	5
RTAX2000S-CQ256	38	0	0	0	6	5
RTAX2000S-CQ352	228	**11** (Icca – note 1)	0	0	34	8
RTAX2000S-LG624	54	0	0	0	8	5
RTAX4000S-CQ352	24	0	0	0	2	2
TOTAL	2095	**14**	0	**2**		

Table 14: Serma Technologies PPBI Data by Part Reference Type

Electrical Fails Detected Prior to Burn-In:

- Functional failures (nominal levels) at +25°C

Two parts were found to fail functionally at room temperature, namely an RT14100A-CQ256 and RTAX1000SL-CQ352E device.

- Static ICCA (core power supply current) at +125°C

For 12 FPGAs, identified as low power devices (RTAX2000SL & RTAX1000SL), the measured current value at +125°C exceeded the SMD specified limit (up to 185mA for a limit of 150mA on the RTAX2000SL and up to 95mA for a limit of 90mA on the RTAX1000SL). As this was not considered as a reliability issue, the customer agreed to relax the limits. In addition, all parts were submitted to the burn-in test where no failure or drift was detected after burn-in. In particular, the ICCA current values had not changed significantly.

- JTAG functional failure at -55°C

For two different projects, the prototype part RTSX32SU used for the test and burn-in set-up, was not functional at -55°C (JTAG functional mode). No fail was observed at +25°C or +125°C. The FM parts were then tested: they passed all the tests at the 3 temperatures, and no fails were detected after burn-in.

- Programming file error

Non conformity to the customer specification was detected during test setup (for instance, the VIL/VIH level measured values were not coherent with the customer's specified I/O type). The analysis revealed a programming issue (error in the file used for programming the parts) where the wrong I/O type was selected in the user file (CMOS/TTL mixed-up). Note that this mistake might have not been detected during the tests at board or system level.

- VIL/VIH input levels fails

It is common to observe functional fails (or VIL/VIH measurement values outside the specified limits) when the specified TTL levels (0.8V/2V) are applied during the test. Often, the levels applied to the Clock or the Reset inputs must be relaxed (VIH=2.4V for instance). It appears that the only way to test properly the VIL/VIH input levels is to implement a specific test mode (NAND-tree structure for instance) that allows measuring the levels in static mode. Usually,

the functional sequence generates too much noise to get clean measurements. This is not considered as a failure, but It shows the design sensitivity to noise (e.g. crosstalk due to high slew rate signals), and may require a specific analysis of PCB routing

Electrical Fails Detected After Burn-In:

Up to January 2013, no electrical or functional failures has been observed on FPGAs which have been submitted to the burn-in test.

Drift fails @25°C:

- Static ICCI (I/O power supply current)

A significant variation of the ICCI power supply current at +25°C was observed after burn-in for a RTSX32SU-CQ256B flight part. At the time of the initial measurements, the high value of the ICCI current had been noticed (about 17mA). The subsequent analysis (variation vs. temperature or vs VCCI) confirmed these results. After burn-in, the measured value was much lower (about 5mA) and coherent with the results observed during the previous BI campaigns (less than 6mA). Because of this "improvement", the computed drift value exceeded the maximum specified limit (-12mA for a limit of ±5mA), and the part was rejected as fail.

A variation in the standby ICCA current value was observed on one RTSX32SU-CQ256 device at +25°C. The standby ICCA current value increased from 2mA prior to burn-in up to 8mA after burn-in. As a result the drift value of 6mA exceeded the maximum specified limit (±5mA).

5.5.4 Other Non-Microsemi/Actel PPBI Data

5.5.4.1 Summary of Independent Reliability Testing on Microsemi AX and RTAX-S FPGAs

Two sets of independent reliability tests pertinent to space-flight applications of the Microsemi RTAX-S/SL FPGAs have been performed.

The first test, performed by The Aerospace Corporation, tested a sample of industrial-temperature AX2000 FPGAs. The decision to test AX FPGAs was taken in order to maximise the number of

antifuse programmable interconnects subjected to test conditions. The industrial temperature AX devices used by The Aerospace Corporation are significantly less expensive than the radiation-tolerant RTAX-S devices, consequently considerably more could be purchased with the funds allocated to the project. The antifuses used in the AX devices are practically identical to those used in the RTAX-S devices, employing the same construction, materials, and dimensions. The programming current used in the RTAX-S devices is a little higher than that used in the AX devices. The ratio of operating current to programming current is higher in the AX devices, resulting in a more stressful test condition than the RTAX-S parts would experience in deployment.

The second test, performed by NASA Goddard Space Flight Centre, tested a sample of RTAX250S and RTAX2000S devices, assembled and tested to RD-11 class B / QML class Q standards.

5.5.4.1.1 Aerospace Corporation Testing

The Aerospace Corporation initiated a long term test of the reliability of the antifuses used in the RTAX-S/SL FPGAs, using industrial temperature AX FPGAs as the test vehicle in order to achieve coverage of a very large number of antifuses. The test sample was broken into three groups – Group A, which was subjected to a high temperature operating life test; Group B, which was subjected to a low temperature operating life test, and Group C, in which samples were exposed to alternating high temperature and low temperature operating life tests. Devices from all three groups were programmed with a design specifically created to maximize the exposure of all categories of antifuses to stress conditions. The design has a very high degree of sensitivity to small changes in timing (on the order of a few nanoseconds), which if present could indicate the transition of a programmed antifuse from the correct low impedance state to a higher impedance. Such a transition would be considered a device functional failure, since it could lead to a signal or clock path becoming slower and consequently causing a set-up or hold time violation.

The test devices were mounted on test boards and placed into the appropriate temperature chambers for each group. Devices were continuously monitored for timing violation by an LED monitoring system mounted on each board. Tests proceeded for over four years, however no instance of an antifuse failure was detected in the testing.

Only one device failed during the test. This device was found to have a stuck-at fault in an SRAM cell at time zero. Failure analysis confirmed that no antifuses were involved in the failing path.

The samples, test conditions, and results are stated in the Table 15 below.

Device	Quantity	Test Type	Total Device Hours
AX2000	277	HTOL (TJ 110°C)	10,894,309
AX2000	272	LTOL (TA -55°C)	10,011,479
AX2000	182	Alternating HTOL and LTOL	5,586,874
Total	731		26,492,662

Table 15: Aerospace Corporation AX Test Conditions and Results

5.5.4.1.2 NASA Goddard Space Flight Centre Testing

NASA GSFC commissioned a reliability test on RTAX-S flight units, choosing to test 82 units each of RTAX250S and RTAX2000S FPGAs screened to RD-11 class B. These devices came from 4 different wafer lots – 2 wafer lots each from RTAX250S and RTAX2000S. Each device was subjected to a total of 3,000 hours of high temperature operating life (HTOL) test, and 3,000 hours of low temperature operating life (LTOL) test. After each 500 hours of burn-in, alternating between HTOL and LTOL, the FPGAs were subjected to testing on automated test equipment at Microsemi's production test facility in Mountain View, California. The life-test procedures are listed in Table 16

The designs programmed into the experimental devices were provided by NASA. These designs were derived from actual flight designs from different flight applications within NASA. The designs are based on a Built In Self-Test (BIST) scheme and incorporate various cores frequently used in FPGA applications (UART, MIL-STD-1553, PIC, XCVER). The BIST output from the different blocks generates a main monitor output to be monitored during the burn-in testing.

LIFETEST PROCEDURES:

Operation	Temperature	Core Voltage (VccA)
ATE Test	Ta = -55C / 25C / 125C	1.425V to 1.575V
Lifetest (0hrs to 500hrs)	HTOL (Ta = 125C)	1.5V (Nominal)
ATE Test	Ta = 25C	1.425V to 1.575V
Lifetest (500hrs to 1000hrs)	LTOL (Ta = -55C)	1.425V (Low)
ATE Test	Ta = 25C	1.425V to 1.575V
Lifetest (1000hrs to 1500hrs)	HTOL (Ta = 125C)	1.575V (High)
ATE Test	Ta = 25C	1.425V to 1.575V
Lifetest (1500hrs to 2000hrs)	LTOL (Ta = -55C)	1.5V (Nominal)
ATE Test	Ta = 25C	1.425V to 1.575V
Lifetest (2000hrs to 2500hrs)	HTOL (Ta = 125C)	1.425V (Low)
ATE Test	Ta = 25C	1.425V to 1.575V
Lifetest (2500hrs to 3000hrs)	LTOL (Ta = -55C)	1.575V (High)
ATE Test	Ta = 25C	1.425V to 1.575V
Lifetest (3000hrs to 3500hrs)	HTOL (Ta = 125C)	1.5V (Nominal)
ATE Test	Ta = 25C	1.425V to 1.575V
Lifetest (3500hrs to 4000hrs)	LTOL (Ta = -55C)	1.425V (Low)
ATE Test	Ta = 25C	1.425V to 1.575V
Lifetest (4000hrs to 4500hrs	HTOL (Ta = 125C)	1.575V (High)
ATE Test	Ta = 25C	1.425V to 1.575V
Lifetest (4500hrs to 5000hrs)	LTOL (Ta = -55C)	1.5V (Nominal)
ATE Test	Ta = 25C	1.425V to 1.575V
Lifetest (5000hrs to 5500hrs)	HTOL (Ta = 125C)	1.425V (Low)
ATE Test	Ta = 25C	1.425V to 1.575V
Lifetest (5500hrs to 6000hrs)	LTOL (Ta = -55C)	1.575V (High)
ATE Test	Ta = -55C / 25C / 125C	1.425V to 1.575V

Table 16: Microsemi Life-Test Procedures

All 164 FPGAs survived the test with no indications of any failures, antifuse or otherwise. Results and test conditions are described in Table 17 below.

Device	Quantity	Hours HTOL (TJ 125°C)	Hours LTOL (TA -55°C)	Total Device Hours
RTAX250S	82	3,000	3,000	492,000
RTAX2000S	82	3,000	3,000	492,000
				984,000

Table 17: NASA GSFC RTAX-S Test Conditions and Results

5.5.4.2 Thales Alenia Space – Return of Experience

Application of PPBI to FPGAs at Thales Alenia Space did not start as a consequence of the MEC antifuses technology Alert in 2004 (RD-1). In fact Thales Alenia Space pioneered this activity in Europe from 1994 based on the earlier experience of OTP PROMs. It should be recalled that fuse problems were encountered on some HARRIS PROMs, as well as other PROMs from RAYTHEON during the 1990s.

Thales Alenia Space France/Belgium/Spain implement a PPBI sequence which includes:

- At pre-BI, perform electrical measurements at 3 temperatures (min/ambient/max) and 3 supply voltages (min/nominal/max & all possible combinations), static parameters + GO/NOGO functional test (VCD as vector stimulus) and monitoring of outputs.
- Combinations of possible supply voltages allow for some clearance against some marginalities ("corner conditions"), as revealed from schmoo plots on some components, an example of which is illustrated in Figure 24 below on an EEPROM.

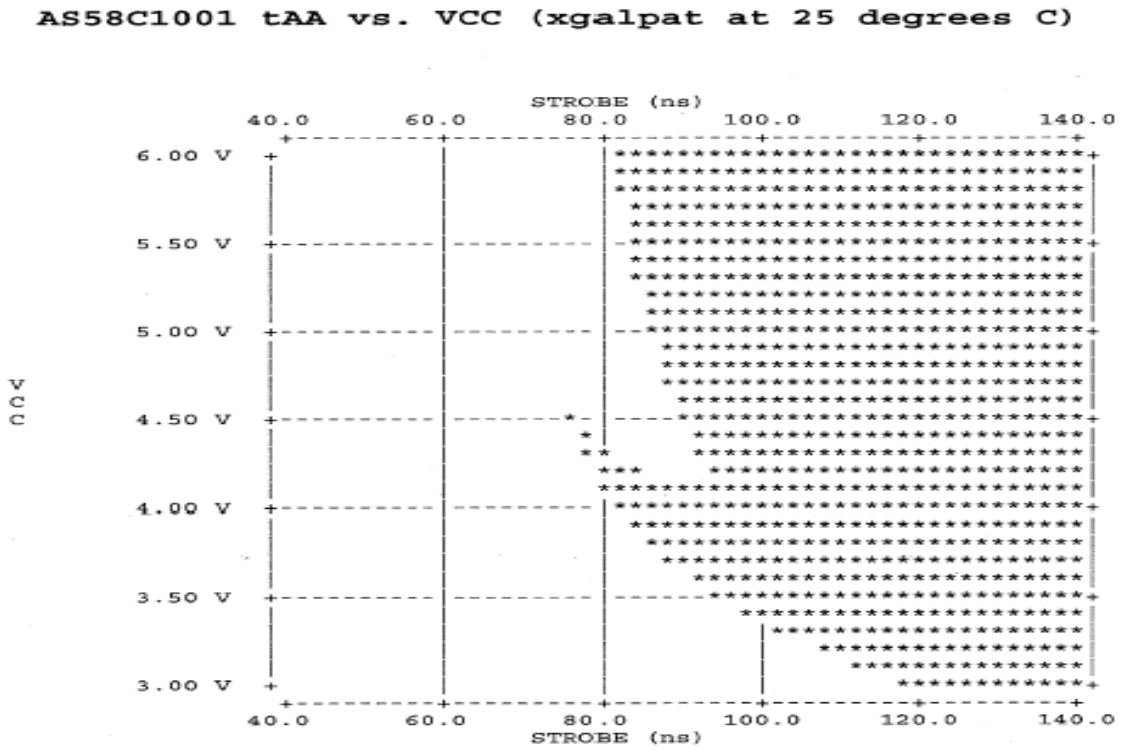


Figure 24: PROM Schmoo Plot from a NASA Workshop

- Burn-in.
- At post-BI, perform the same tests as were performed pre-BI.

The burn-in conditions defined with Microsemi support are as follows:

- Conditions are based on those used by Microsemi for “blank device” burn-in except for the JTAG activation.
- Burn-in is dynamic since clocks are activated and I/Os are biased.
- Parts are biased under maximum recommended operating conditions.
- Burn-in duration depends on projects and customer requirements, typically being 168h (minimum value) or 240h.
- Ambient temperature during burn-in is +125°C.
- Parametric limits are those of the relevant SMD specification (if existing).

It shall be noted that these burn-in conditions are very similar to those used for many years on Atmel ASICs, devices being comparable in terms of function, technology and complexity. For the PPBI implementation, Thales Alenia Space has used Serma Technologies since the beginning. From the starting point in 1994, Thales Alenia Space has in total run 824 FPGAs through the PPBI sequence, of which 28 devices (or 3.39%) have been found to fail. The large majority of these tested FPGAs are already in orbit.

Statistics by FPGA families are presented here below in Table 18:

	Family						
						UMC technologies	
	ACT1	ACT2	ACT3	RT54SX	RT54SX-S	RT54SX-SU	RTAX-S
Sumitted to PPBI	85	129	69	234	61	230	44
Rejects	0	2	0	23	2	2	0
Reject percentage	0	1.55%	0	9.8%	3.3%	0.9%	0
Failures description	-	Vol out of spec at pre-BI test	-	All failures at pre-BI test : * 18 functional failure * 5 parametric failures, Iil and Icc values out of spec	Both failures after BI : Icc stand by value out of spec, and Icc stand by drift out of spec	* 1 RTSX32SU failed Icci drift criterion. Value out of distribution before BI, but fully inside distribution after BI. Failure analysis performed by Microsemi, but non conclusive. * 1 RTSX72SU failed Icca drift criterion. No failure analysis performed because classified design.	-

Table 18: Thales Alenia Space PPBI Data by Family

It shall be noted that these families were not produced on the same technology, foundry and antifuse structure:

- ACT1/RT1020: BAE Systems Manassas foundry. RH1020 procured directly from BAE Systems shared the same technology as the RT1020, only differing by the die revision and all are included in the figures.
- ACT2/A1280XL/RT1280: MEC foundry, 1µm technology, ONO (oxide/nitride/oxide) antifuses. RH1280 procured directly from BAE Systems shared the same technology, RT1280 and RH1280 all are included in the figures.
- ACT3/RT1460/RT14100 : MEC foundry, 0.8µm technology, ONO antifuses.
- RT54SX16/32 : MEC foundry, 0.6µm technology, M2M (metal-to-metal) antifuses.
- RT54SX32/72S : MEC foundry, 0.25µm technology, M2M (metal-to-metal) antifuses.
- RTSX32/72SU : UMC foundry, 0.25µm technology, M2M (metal-to-metal) antifuses.
- RTAX-S series : UMC foundry, 0.15µm technology, M2M (metal-to-metal) antifuses.

Within the global 3.39% reject rate, it should be noted that the failures are not evenly distributed over the different families and device types. The major contributors to this reject rate are RT54SX16/SX32 devices, in addition to RT54SX32S and A1280XL devices. Further important information to be considered is that the majority of these failures were identified at pre-BI electrical test. Only two parts were found to have failed post-BI and both of these were RT54SX32S devices, where one part had an Icc standby current value out of spec and the second part was out of spec for Icc standby current drift.

Migration from the MEC technologies to UMC technologies has led to a marked improvement and a reduced post-programming failure rate. Only one device out of 246 or 0.4% (combining all UMC-based devices, being either SX-SU or RTAX-S series) has been found to fail for PPBI with an Icc standby current value found to be out of distribution (but still inside the parametric limits) at the pre-BI measurement but fully inside the distribution after burn-in. This led to an Icc standby current drift value out of spec. Failure analysis was conducted by Microsemi but found to be non-conclusive.

Thales Alenia Space Italy has a more recent history on PPBI having started only in 2010. The data on Microsemi devices (RT1280, RTSX, RTAX) can be split in two categories, namely:

- Post-programming screening at part-level on Microsemi devices with 0 failed parts on 164 screened devices.
- Post-programming screening at board or unit level with 0 failed parts on 70 screened devices.

It should be noted that some of the post-rogramming screenings implemented by Thales Alenia Space Italy did not use high temperature application. In conclusion, Thales Alenia Space reiterates that no in-flight equipment issue caused by an FPGA failure has ever been recorded.

5.5.4.3 TESAT Spacecom – Return of Experience

TESAT Spacecom started to systematically perform PPBI in 2009 by using the service offered by Serma Technologies. An overall quantity of 141 devices, representing 20 different designs, implemented on six different device types from RTSX32SU-CQ84 to RTAX4000S-CQ352 have been screened. None of the devices have failed either the initial or the final functional and parametric tests. Furthermore, none of the devices have shown any unexpected behaviour or failure at initial equipment operation. Due to poor handling during transport one device exhibited bent leads and had to be reworked.

5.5.4.4 Thales CS – Return of Experience

Thales CS has performed PPBI on Microsemi SX and AX families. For the past year, all components subject to testing have passed the PPBI test.

Reference	Qty tested	Qty Fail
RTSX32SU*	48	0
RTSX72SU*	38	1**
RTAX1000***	24	0

Table 19: Thales CS PPBI Data Overview

* Pseudo-dynamic PPBI.

** Failure occurred between programming and the initial electrical characterisation step, so that the part passed programming but was considered blank on the electrical test equipment.

*** Full dynamic PBBI on 12 components and pseudo dynamic PPBI on 12 components for comparison purposes. No relevant or pertinent differences were observed between the fully dynamic and pseudo dynamic flows.

PPBI on RTAX1000:

Figure 25: Thales CS RTAX1000 PPBI Setup

Thales CS performed a fully dynamic versus pseudo dynamic PPBI comparison on 24 components. 12 components were used with a pseudo dynamic PPBI and 12 components with a fully dynamic PPBI. Thales CS developed a specific design in order to attain 97% coverage of the FPGA gates. For this PPBI configuration 119 IO's were used among the 198 FPGA IOs. During the PPBI test, 42 inputs, 8 I/O's, clock and reset pins were stressed with a pattern generator at 20MHz. 69 outputs were charged in order to stimulate the application. For the pseudo static PPBI configuration only a 20MHz clock was applied to the component.

PPBI Flow:

- Programming with Silicon Sculptor 3
- Initial electrical characterisation at 3 temperatures
- Burn-In 240 h @ 125°C
- Final electrical characterisation at 3 temperatures
- Drift calculation

No relevant or pertinent differences were observed between the fully dynamic and pseudo dynamic flows. As a result, Thales CS has proposed to perform a 1000 hour life-test in order to determine if any significant differences can be revealed.

5.5.5 PPBI Data from Other OTP Device Manufacturers

5.5.5.1 Thales Alenia Space – Return of Experience

The offering of OTP FPGAs suitable for space use is very limited outside the Microsemi families. Thales Alenia Space has previously used the Aeroflex UT6325 (aka Eclipse) device. 9 such Aeroflex parts were submitted to post-programming screening at part-level and no parts were found to fail.

5.6 FPGA PPBI WG Conclusions & Recommandations

Based on the identified issues within this document, the FPGA PPBI Working Group has made the following statements and conclusions:

1. The WG recognises that the Serma Technologies pseudo-static burn-in provides low test coverage & little or no activation of FPGA antifuses.
2. Microsemi already applies two categories of burn-in on all virgin blank parts, namely: static blank burn-in (SBBI) and dynamic blank burn-in (DBBI) using a high stress test design. It is noted that SBBI is applied to E-flow and V-flow/EV-flow RT FPGAs, while SBBI is not applied to B-flow RT FPGAs. DBBI is however, applied to all three screening flows.
3. From Microsemi ELA (Enhanced Lot Acceptance) testing no antifuse failures have been recorded to date.

4. From independent Aerospace Corporation testing a long-term test of the reliability of RTAX-S/SL FPGA antifuses has been performed. From RD-7 it is noted that 731 devices have been tested with 26,492,662 total devices hours and no antifuse failures were detected.
5. NASA GSFC commissioned reliability tests on RTAX250S & RTAX2000S. 164 devices were subjected to 3000 hours HTOL, 3000 hours LTOL with 984,000 total device hours and no antifuse failures were detected.
6. The full Serma Technologies PPBI data set from 2004 through to January 2013 covers 2095 Microsemi FPGAs and indicates that no electrical or functional failures have been observed on FPGAs which have been submitted to burn-in.
7. However, it is noted from the Serma Technologies & TAS data sets that a number of electrical parametric fails have been observed during the PPBI flow after electrical testing but always prior to the burn-in.
8. TAS highlights that a very strong improvement has been observed since migrating from the MEC technologies (global PPBI reject rate of 4.7%) to the UMC technologies (global PPBI reject 0.4%). The reject rate has decreased by an order of magnitude since switching to the UMC foundry.
9. TESAT Spacecom has detected no burn-in fails on 141 devices covering 20 designs over 6 Microsemi device types.
10. Thales CS detected 1 device fail prior to burn-in and no burn-in fails on 110 devices tested.

Based on the above conclusions, the FPGA PPBI WG recommendations were as follows:

1. To remove the post-programming burn-in requirement from RD-8 for UMC-based Microsemi FPGAs on technologies with a clear and defined heritage which is applicable to those part types listed in RD-10. The update of this RD-8 ECSS standard was published on October 21st, 2013 as RD-9.
2. For all Classes of UMC-based Microsemi FPGA components, PPBI shall remain mandatory in the case of a new family, a new technology, or major process, mask or foundry changes.
3. Agreement and consensus that the programming aspects for OTP Microsemi FPGAs shall need to be better documented. To this end RD-10 includes (although not necessarily limited to) some programming best practices for OTP Microsemi FPGAs.
4. To update RD-8 detailing that the programming software to be used should be the latest "qualified" software version with life-test/lot acceptance test data and not necessarily the latest version released by Microsemi. This has been captured in Sections 4.6.4f, 5.6.4f and 6.6.4f of RD-9.

5. Microsemi shall be actioned to not recommend the latest programming software version for space users but instead shall recommend the latest “qualified” software version with life-test/lot acceptance test data (as per the previous bullet).
6. No agreement or consensus was reached on whether or not to perform electrical testing after programming. As a result RD-8 has not been changed in this regard where it is now stated in RD-9 that the supplier shall prepare a post-programming procedure for customer’s approval, depending on part types (including when necessary electrical tests, programming conditions and equipment, programming software version qualified by the supplier, burn-in conditions, additional screening tests and specific marking after programming).

6 ANNEX1: FPGA PPBI WG TERMS OF REFERENCE (TOR)

FPGA Post-Programming Burn-In Working Group.

6.1 Introduction

On July 3rd 2012, the 2nd FPGA Post-Programming Burn-In (PPBI) Workshop was held at ESTEC, Noordwijk. The objective of this workshop was to share experience from users and agencies on the PPBI testing of one-time programmable FPGA devices, to review the PPBI failures encountered by users and specifically Microsemi & Serma Technologies in order to better understand the necessity or not of the current PPBI requirement, to form an opinion if the current PPBI requirement is considered to be valuable or not and to propose alternative methodologies, and to find consensus on an agreed way forward that best serves the European space industry in ensuring a high level of assurance and quality control of one-time programmable FPGA devices.

As an outcome of this FPGA PPBI Workshop it was recommended to form an ad hoc FPGA PPBI WG in Q3 2012 in support of the Component Technology Board (CTB) with the primary purpose of formulating a documented technical justification for the removal/modification or not in certain well identified cases of post-programming burn-in on one-time programmable FPGA devices as currently required per RD-8.

The group was formed as a temporary council to the CTB with a core membership of appointed experts in the field from ESCC participants. The group invited and involved other experts as deemed fit for purpose. The task was originally to be completed with a minimum of face to face meetings before the end of November 2012.

6.2 Scope

The scope of the Working Group (WG) was:

- *To review all available pertinent PPBI test data and relevant PPBI-related screening data and field experience to justify the removal/ modification or not in certain well identified cases of post-programming burn-in on one-time programmable FPGA devices for space applications and not limited to Actel/Microsemi products.*

- *If and where applicable to propose an alternative to burn-in after programming in a manner that ensures the high level of assurance and quality control of one-time programmable FPGA devices.*

- *The key task of the FPGA PPBI WG shall be to analyse and document the afore-mentioned data in a clear and concise manner for review and approval by the ESCC CTB and PSWG in order to support and prepare a pertinent change request for the ECSS-Q-ST-60C . This document shall detail the positions of the European space industry and agencies w.r.t. the benefits and drawbacks of PPBI as part of post programming device screening and the screening tests themselves if any. The target for the FPGA PPBI WG is to prepare this draft document(s) for ESCC technical and policy review by November 29th 2012.*

6.3 Responsibilities

The responsibilities of the WG were to:

- *Determine the reliability of current antifuse technology used for Space FPGA types and their known failure modes.*
- *Determine the level of production testing and pre-programming screening applied by the manufacturer(s).*
- *Determine the reliability of OTP FPGA programming equipment (HW and SW) and associated programming practices and programming experience by users and manufacturer(s).*
- *Compile and compare post programming screening requirements on antifuse based OTP FPGAs in industry, especially for high reliability applications.*

Specifically in this regard it was required to:

- *Compile all relevant and pertinent historical information and data on the MEC technology antifuses highlighted in the ESA Alert ESA Alert EA-2004-EEE-07-B released in April 2005.*

- *Demonstrate that the reliability weaknesses applicable and inherent to the MEC technology antifuses is not applicable to the UMC technology antifuses.*

- *Compile all relevant and pertinent PPBI data and PPBI-related data on the UMC technology antifuse to justify the removal/modification or not of post-programming burn-in on one-time programmable FPGA devices.*

- *Review and consider previous studies and analysis available on the topic.*

- *Propose an alternative to burn-in after programming, if and where applicable, in a manner that ensures the high level of assurance and quality control of one-time programmable FPGA devices.*

6.4 Organisation

6.4.1 General

The FPGA PPBI Working Group defined and implemented its own workplan which was presented at the CTB Plenary meeting. The activities of the WG were not be limited to the preparation and conduct of meetings but were also progressed by means of off-line communication.

6.4.2 Chairperson

The chairperson was to have the full support of his employing organisation to devote an adequate amount of time to the fulfillment of his duties. It was the Chairperson's responsibility to achieve the tasks and deliverables defined for the group while keeping to its schedule. The Chairperson was to provide WG members with adequate material and data at least one (1) week ahead of the next meeting.

Minutes of all WG meetings were to be produced and posted in the group's dedicated data repository on https://spacecompoments.org within one (1) week after the meeting.

The WG Chairperson or his representative reported on the activities and progress of the group to the CTB Plenary. Following the 2nd FPGA PPBI Workshop on July 3rd 2012, the proposed WG chairperson was selected as: **Ken Hernan ESA/ESTEC**

6.4.3 Membership

The following members were appointed to the working group as of August 2nd 2012:

Member	Affilation	Status	Contact E-mail
Joel LE MAUFF	Alter Technolgy	Confirmed	joel.lemauff@altertechnology.com
Vincent LESTIENNE	Astrium	Confirmed	vincent.lestienne@astrium.eads.net
David DANGLA	CNES	Confirmed	David.Dangla@cnes.fr
Jerome CARRON	CNES	Confirmed	Jerome.Carron@cnes.fr
Volker LÜCK	DLR	Confirmed	Volker.Lueck@tesat.de
Ralf DE MARINO	ESA	Confirmed	Ralf.De.Marino@esa.int
Ken HERNAN	ESA	Confirmed	Ken.Hernan@esa.int
John MCCOLLUM	Microsemi	Confirmed	John.McCollum@microsemi.com
Ken O'NEILL	Microsemi	Confirmed	keno@microsemi.com
Maxence LEVEQUE	Serma Tech.	Confirmed	m.leveque@serma.com
Michel CARQUET	TAS	Confirmed	michel.carquet@thalesaleniaspace.com
Aurelien JANVRESSE	Thales TCS	Confirmed	aurelien.janvresse@thalesgroup.com

6.5 Deliverables

The FPGA PPBI WG Report representing the current view of European OTP FPGA users and agencies together with relevant supporting documentation was to be prepared for review by the Silicon WG, CTB and PSWG.

The responsibility for submitting any corresponding change requests to the ECSS Technical Authority shall be with the SCSB and Q-ST-60 WG.