The feasibility of Irradiating Devices Through the Backside

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Contents

- Picosecond irradiation facilities

- Direct front irradiation at 830 nm:

  1-µm step Mapping of SEU's in a dual ported memory.

  Comparison with the chip layout and identification of sensitive nodes

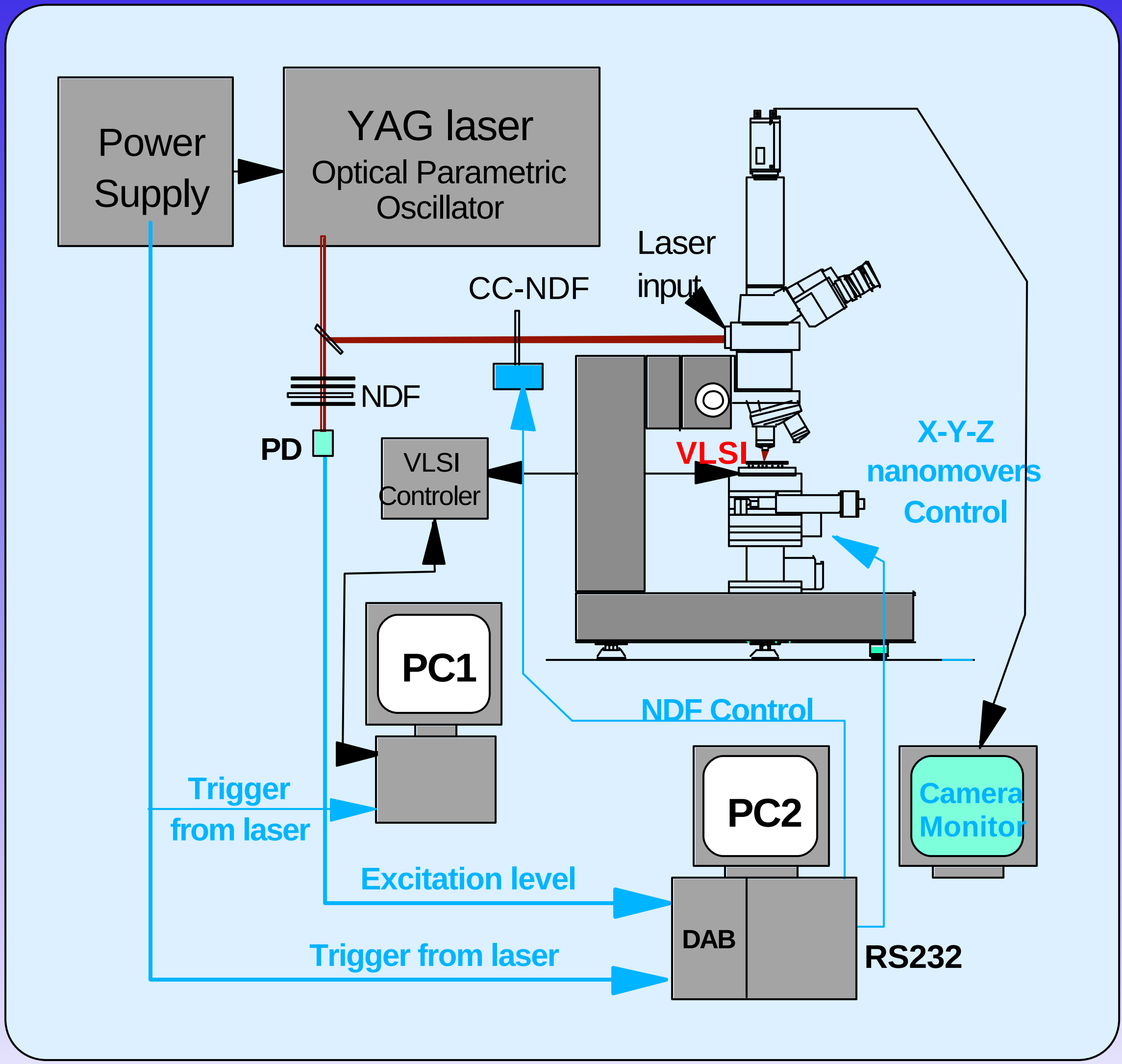
- Back irradiation at 1064 nm:

  Modification of the microscope-camera setup

  IR imaging through the substrate

  Substrate etching

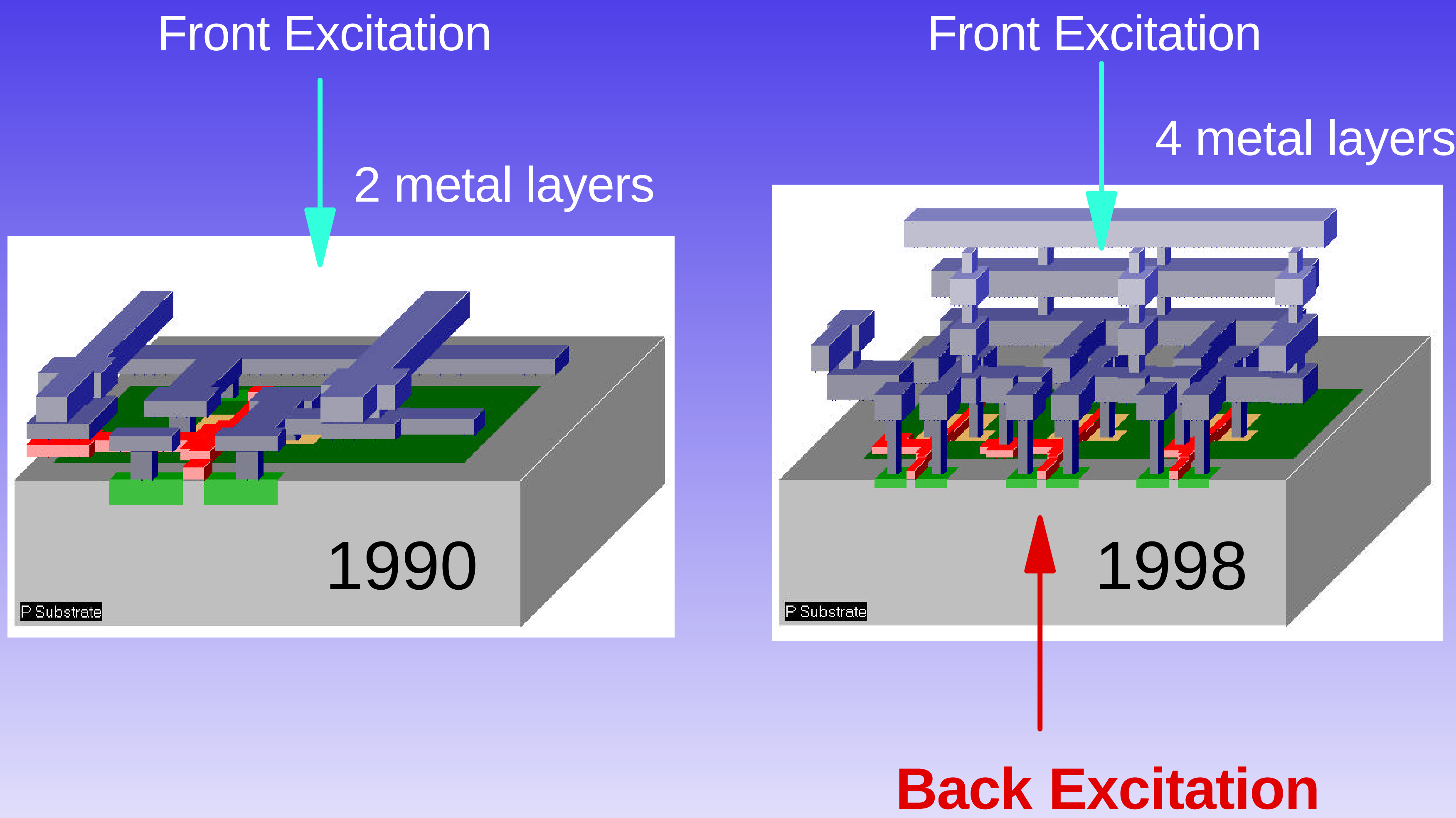
Facilities for picosecond irradiation of Silicon



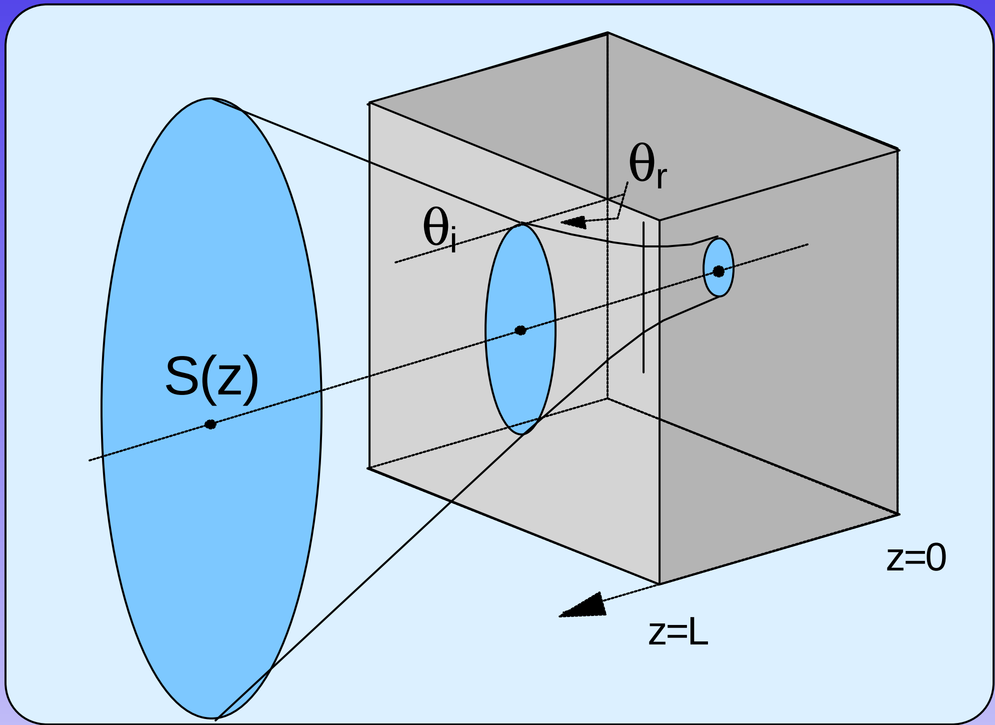
main features:

- Adjustable excitation wavelength
- Picosecond pulses at 10 Hz
- Spot size slightly less than 1 µm
- Automatic scanning and recording

Technology evolution and screening of the active zones by the metallic layers



Back Irradiation through the substrate for flipped-chip packaging



Constraints:

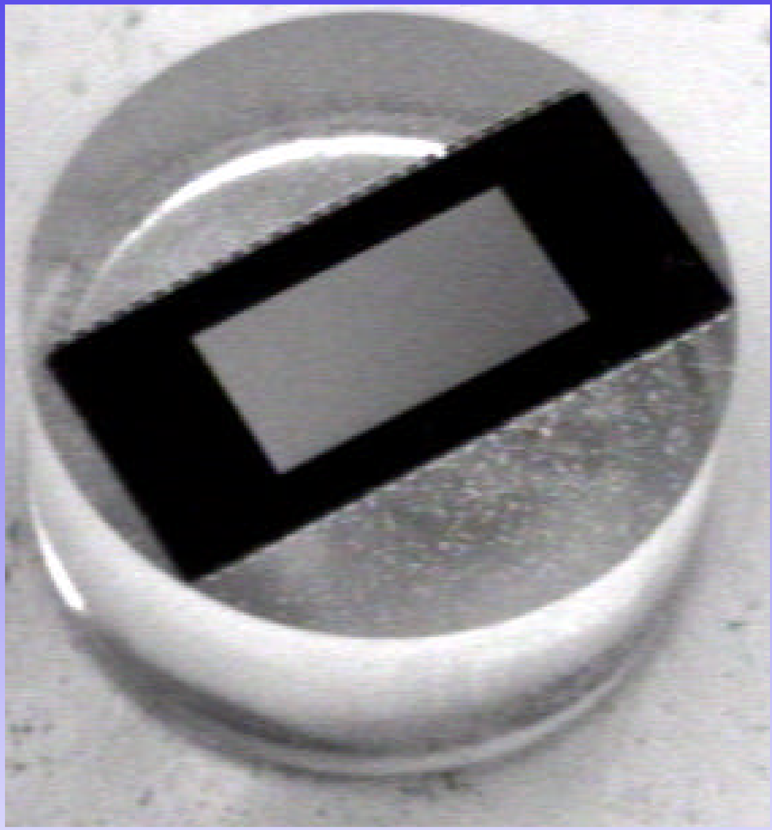
1) Substrate etching versus operation wavelength

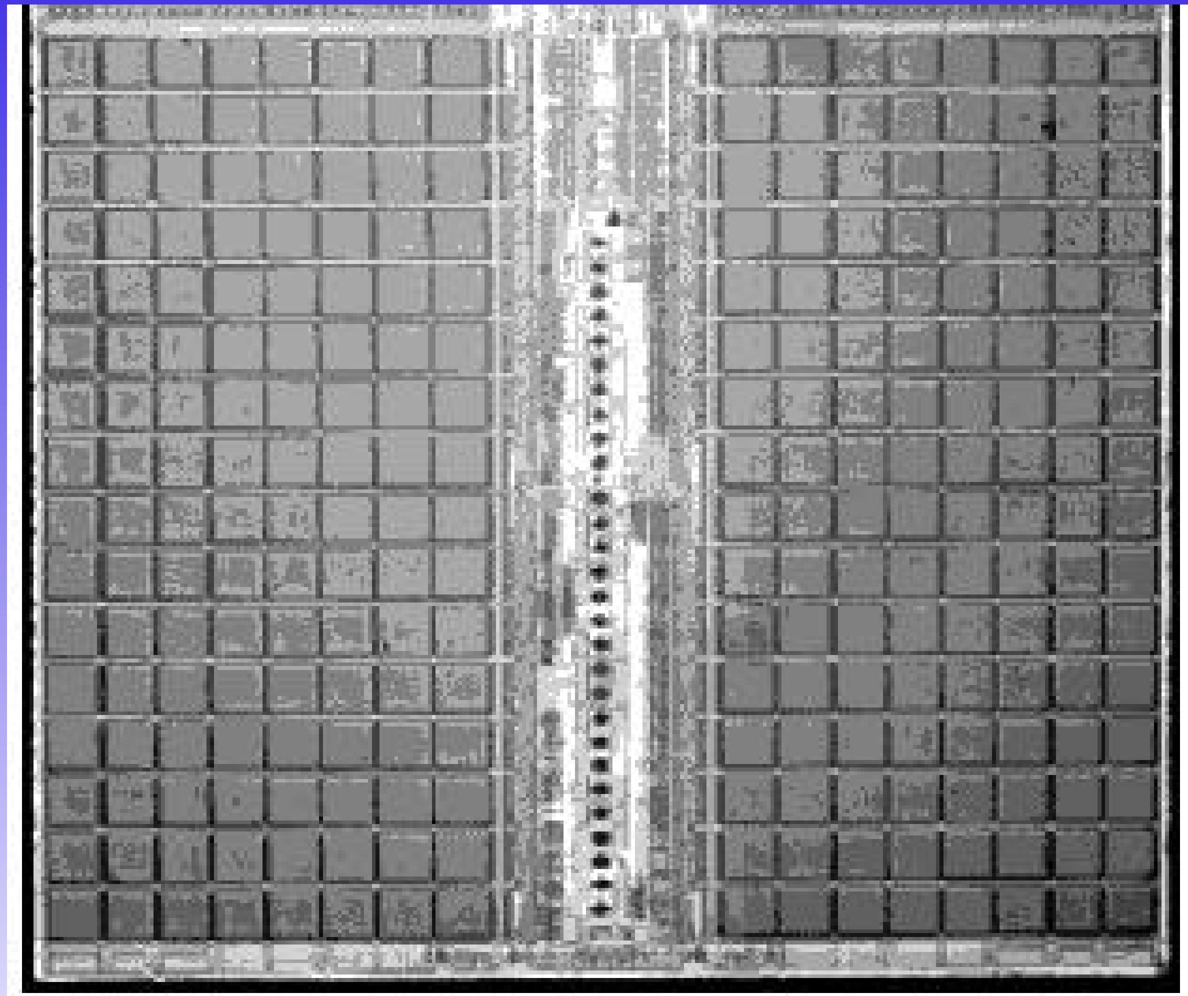
2) Back-surface polishing

3) IR imaging through the surface

SRAM substrate polishing

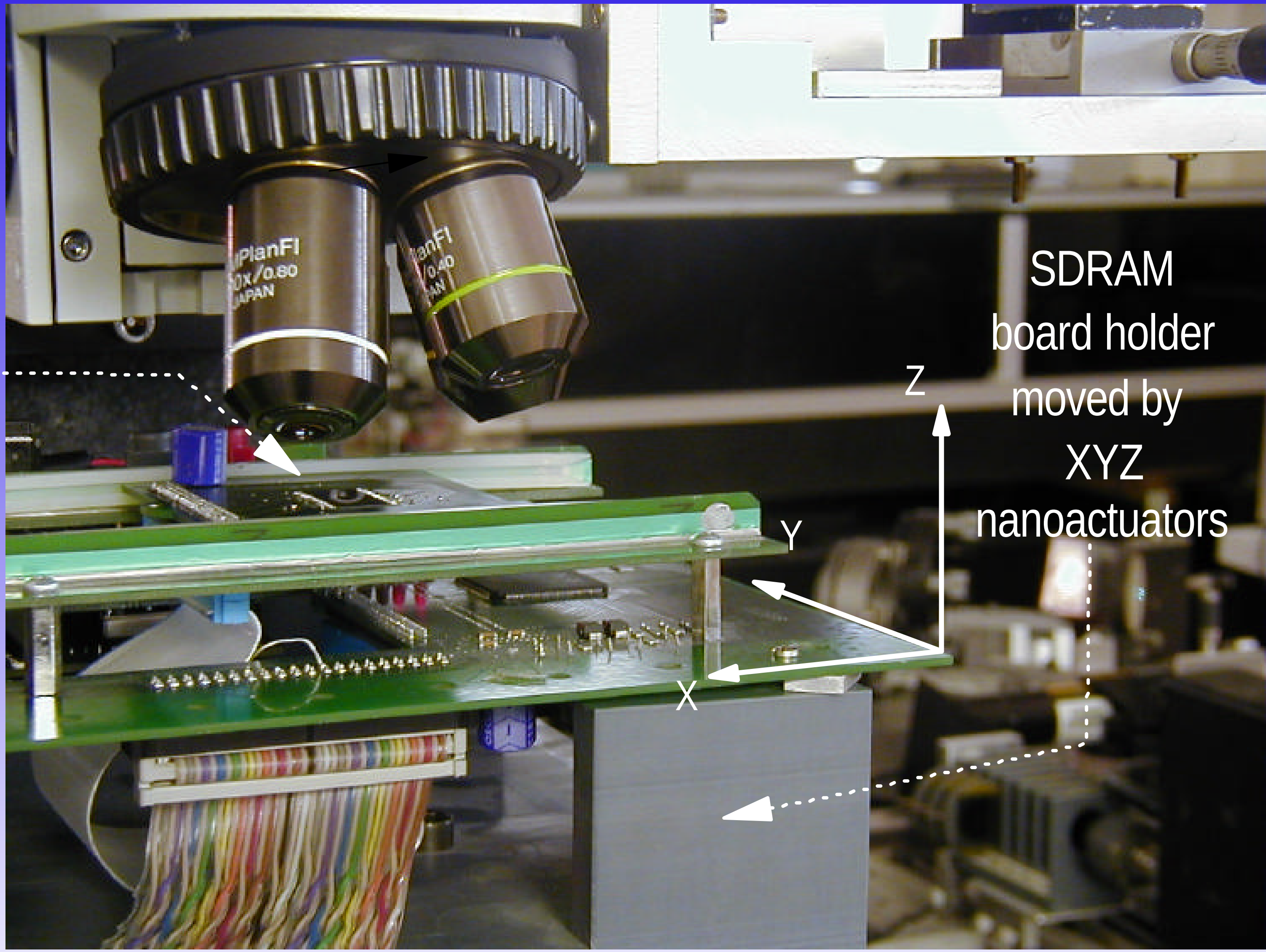
Device: SAMSUNG SDRAM
64 Mb KM41654030 CT G8



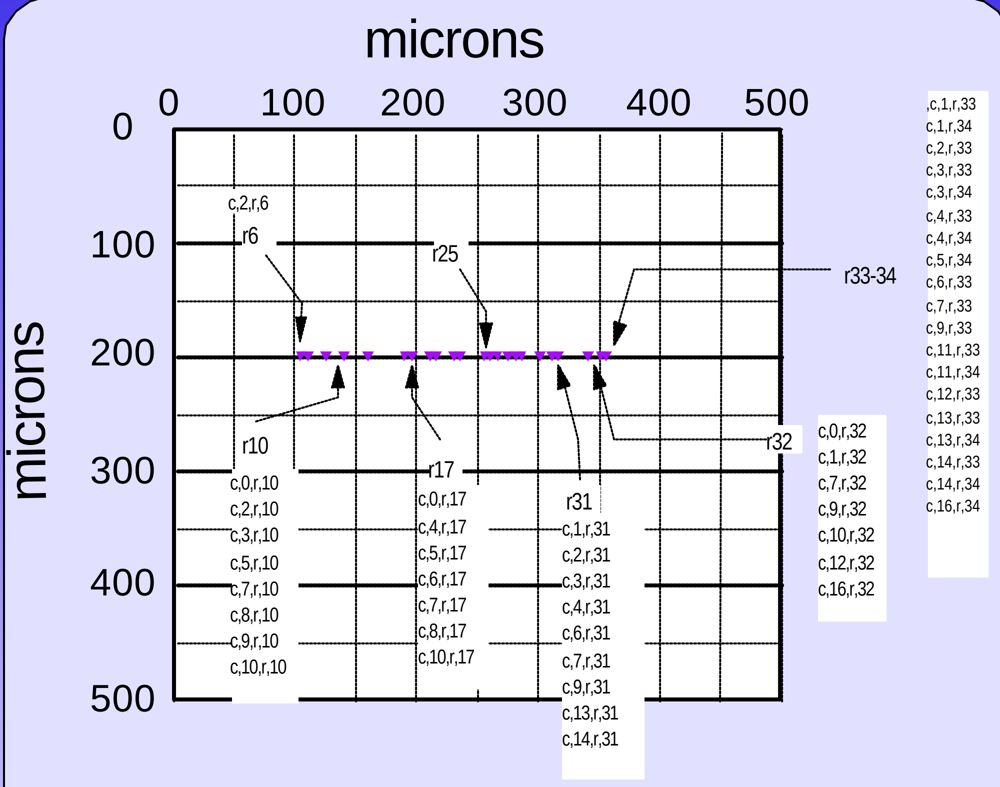


RAM holder and microscope setup

polished
flip-chip
SDRAM



Demonstration of Back Irradiation



lens: x5 NA=0.15 => spot Dia.: 5 microns

Test Conditions:

Device: SAMSUNG SDRAM

64 Mb KM41654030 CT G8

SEU Record: 1 bit chosen in the first byte in 256 kb of a 16-Mb bank.

Pratically (1/500) of one bank

Conclusion

1) We have unambiguously demonstrated that SEU's can be generated with back irradiation at 1.064 μm through the substrate

2) These results are preliminary.