CURRENT STATE AND FUTURE TRENDS OF PCBS IN JAXA

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ABSTRACT

In space application, high density mounting has been necessary with downsizing of electronic devices. Thus the device packages have also been shifting from QFP to area array packages such as BGA/CGA.
In this paper, we report "PCBs for area array packaging" that have been developed with JAXA, and the trend of PCBs including "PCBs for high speed digital signals" which are currently under qualification test.

1. JAXA QUALIFIED PCBs

The following are JAXA qualified PCBs in the present;

JAXA-QTS-2140 PCBs, General Specification for
- Appendix A PCBs
- Appendix B Fine pitch PCBs ; For mounting SMD
- Appendix C Discrete Wiring Boards
- Appendix D Flexible PCBs
- Appendix E Rigid-Flex PCBs
- Appendix F CIC metal core PCBs ; For low CTE, heat sink
- Appendix G PCBs for area array packaging

2. DEVELOPMENT OF PCBs FOR AREA ARRAY PACKAGING

The target of this type of PCB is as follows;

- Corresponding to 1.0mm pitch area array packaging mounting
- 600 or more pins area array packaging

The key technologies of PCB required to mount area array packaging are as follows

- Fine pattern
- Via-in-Pad and filled Via

2.1. Fine pattern

Figure 1 shows the conventional design rule.
The conductor width is 0.13mm, and the minimum drilled hole diameter is 0.35mm.
In this design rule, the number of conductor is limited to one line per 1.27mm pitch.
Two lines per pitch is needed for 1.0mm pitch area array packaging that has 600pins or more.
Figure 2 shows the new design rule we have developed.
Both conductor width and conductor spacing are 0.08mm, drilled hole diameter is 0.20mm.
Two lines per 1.0mm pitch is now realized in this new design rule.
Mounting approximately 1000 pins area array packaging is possible with 14-layer PCBs.
The new design rule requires high accuracy patterning technology.
To meet this requirement, we used Laser Direct Imaging (LDI) for dry film exposure.

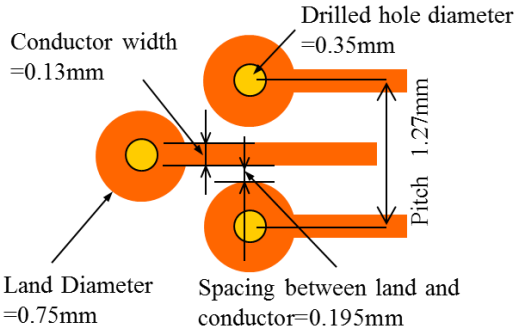

Figure 1. Conventional design rule

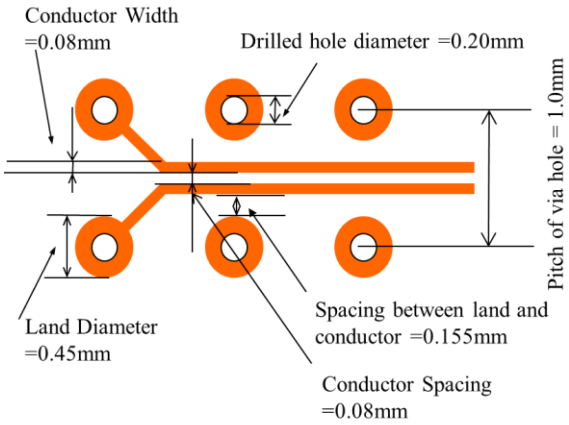

Figure 2. New design rule

2.2. Via-in-Pad (VIP)

With this design rule, we are able to make Fan-out padding (see Figure 3).
However, in this case, the pad size is limited by the land size.
VIP structure is able to create the pad size necessary for area array packaging assembly because the land is used as pad in this structure (see Figures 4 and 5).
Therefore, we selected VIP structure.

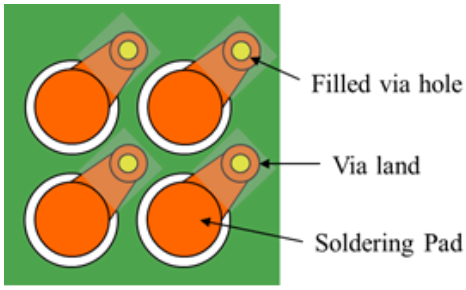

Figure 3. Fan out Pad

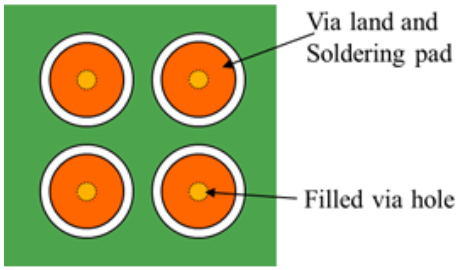

Figure 4. Via-in-Pad

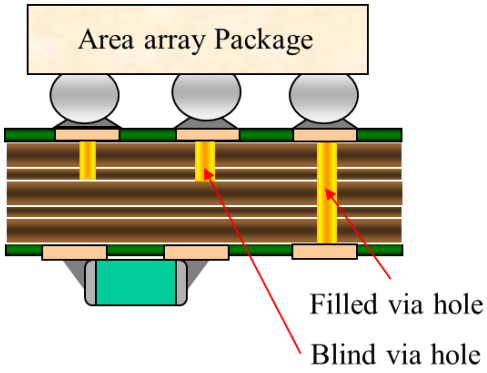

Figure 5. Cross-section of Via-in-Pad

Issue of VIP is the technique for via filling and adhesion of pad (Cap plating) to via filler.
We use particular type of resin for via filling.
General issues of via filling are void of resin (see Figure 6) and dimple of cap plating (see Figure 7).

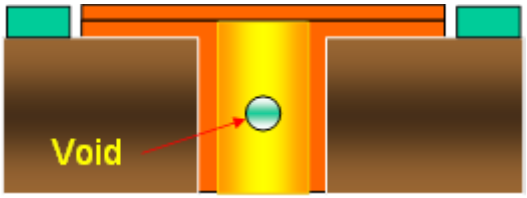

Figure 6. Void of Via fill

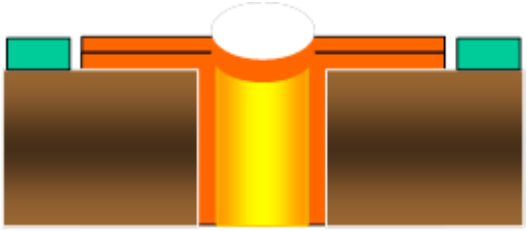
Figure 7. Dimple of Cap plating

To solve this issues, we filled the via under reduced pressure.
Our finished filled via is void-free (see Figure 8) and flat cap plating (see Figure 9).


Figure 8. Cross section of 0.2mm Dia. PTH


Figure 9. Cross-section of cap plating

Adhesion of cap plating to filled via has a close relation to the drilled hole diameter and thickness of cap plating.
We have determined the optimum condition for the great adhesion by performing a comprehensive

evaluation.
The identified optimum condition is that the drilled hole diameter of 0.2mm and the minimum thickness of cap plating of 25um.

2.3. Qualification Test

We passed the Qualification Test under JAXA-QTS-2140 Appendix G.
A part of QT is as follows;

- Thermal cycling: -30 to +125 deg.C, 1,000 cycles
- Solder bath float: 288 deg.C , 10 seconds
- Hot oil dip Resistance: 260deg.C, 10seconds, 10 cycles
- Humidity and Insulation Resistance : 25 to 65deg.C, 90~98%RH, less than 500M ohm
- Dielectric Withstanding Voltage : 500Vdc, 30 seconds
- Radiation Hardness : 1E+4Gy, less than 500M ohm

2.4. Specification

Table 1 shows specification of PCBs for area array packaging.

Table 1. Specification of PCBs for area array packaging

Item		Specification	
Pad	Pitch	1.0mm	
	Structure	Fan-Out Pad	Via-in-Pad
Drilled hole diameter		0.20mm	
Conductor (External)	Width	0.13mm	
	Spacing	0.15mm	
Conductor (Internal)	Width	0.08mm	
	Spacing	0.08mm	
Number of Layers	Total	14	
	Blind via	6	
Board thickness	Modified Polyimide	2.1mm	
	HTg FR-4	2.3mm	
Surface finish		HASL	

3. TREND

In the near future, most of the devices will be downsized and the device pitch is expected to be 0.8mm. To correspond to the reduced sizes and the pitch, the future PCBs will need to have the conductor width and conductor spacing of 50um and 22 layers or more.
High Density Interconnect structure (Microvia) will be required for some parts.
For high frequency application, organic PCBs will be replaced by PTFE or Ceramic PCBs due to the improvement of material properties.
For metal core PCBs, CFRP, etc. will be replaced by Copper-Inver-Copper for heat sink and low coefficient of thermal expansion.
Clock Frequency of CPU will be 1GHz or more.
PCB will require low transmission loss and characteristic impedance control.

We are currently developing" PCBs for high speed digital signal", and we report these next.

3.1. PCBs for high speed digital signal

Feature of this PCBs is as follows;

- Low dielectric constant (Dk) and Low dielectric tangent (Df) material
- Low profile copper foil
- Fine pattern

We decided on the specifications of Qualification Test Sample as shown Table 2.

Table 2. Specification of PCBs for high speed digital signal

Item		Specification	
Base Material	Dk (εr) (1GHz)	3.65	
	Df (tan δ) (1GHz)	0.002	
Pad	Pitch	1.0mm	
	Structure	Fan-out of Pad	Via-in-Pad
Drilled hole diameter		0.20mm	
Conductor (External)	Width	0.12mm	
	Spacing	0.14mm	
Conductor (Internal)	Width	0.07mm	
	Spacing	0.08mm	

We will be performing the Qualification Test up to October, 2014.

4. SUMMARY

The future PCBs require downsizing and high speed.
We developed PCBs for area array packaging which are qualified by JAXA and are currently developing PCBs for High Speed digital signal.
We expect that the future PCBs will be developed for each function (e.g. PCBs for high heat sink, PCBs for low CTE, etc.).