

Qualification of Class Y Flip Chip CGA Package Technology for Space

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Solution-Minded



Performance-Driven



Customer-Focused



- ▼ **MIL-PRF-38535 Revision K**
- ▼ **UT1752FC Class Y Package**
- ▼ **Package Integrity Demonstration Test Plans (PIDTP)**
 - **Flip Chip Assembly**
 - **Large Die Flip Chip**
 - **Solder Column Attach**
 - **Heat Sink Attach**
 - **Chip Cap Attach**
- ▼ **Conclusions**

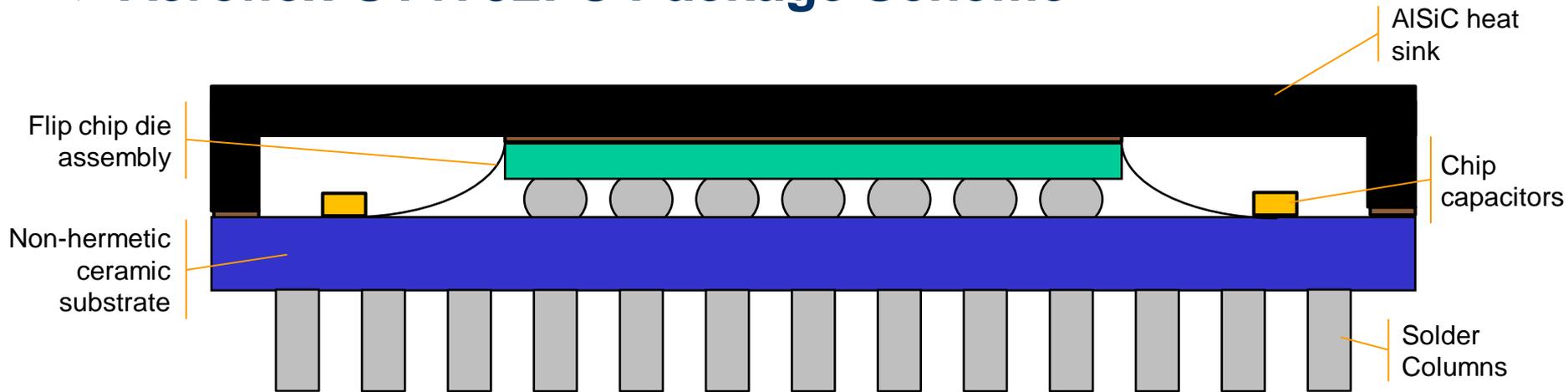
- ▼ **Rev. K defines for the first time Class Y requirements**
 - Rev. K was released in December 2013
 - Class Y defined as ceramic “non-hermetic” package for space
 - Aeroflex was active participant in JEDEC Class Y Task Group
 - Aeroflex is now implementing Rev. K requirements
- ▼ **Rev. K stipulates that a PIDTP be performed for all new package technologies**
 - Package Integrity Demonstration Test Plan (PIDTP)
 - PIDTP addresses the manufacturability, test, quality and reliability issues associated with non-traditional package and assembly technologies

- ▼ **Aeroflex has adopted a 2-part qualification approach for new package technologies**
 1. **Complete the PIDTP reliability assessment for any new package and assembly technologies**
 2. **Execute a product qualification plan utilizing the new package and assembly technologies**

- ▼ **Aeroflex PIDTP evaluations in support of the UT1752FC package technology**
 - **Flip chip assembly**
 - **Solder column attach**
 - **Heat sink attach**
 - **Chip cap attach**

UT1752FC Class Y Package

▼ Aeroflex UT1752FC Package Scheme



- Non-hermetic flip chip technology
- MIL-PRF-38535 Class Y qualified
- 1,752 Package I/O on a 1.00mm pitch
- 45x45mm package footprint
- Ceramic substrate technology
- Land Grid Array (LGA) or solder Column Grid Array (CGA) format options
- Aeroflex UT90nHBD die
- Eutectic 63Sn/37Pb wafer bumping
- Aeroflex flip chip assembly
- Aeroflex chip cap attach
- AlSiC heat sink lid technology
- Six Sigma solder column attach

▼ Package Integrity Demonstration Test Plan

- Based on Failure Mode and Effects Analysis (FMEA) of flip chip assembly processes
- Initial PIDTP completed and presented to JEDEC Class Y Task Group in October 2011
- 90nm flip chip package PIDTP completed in October 2013

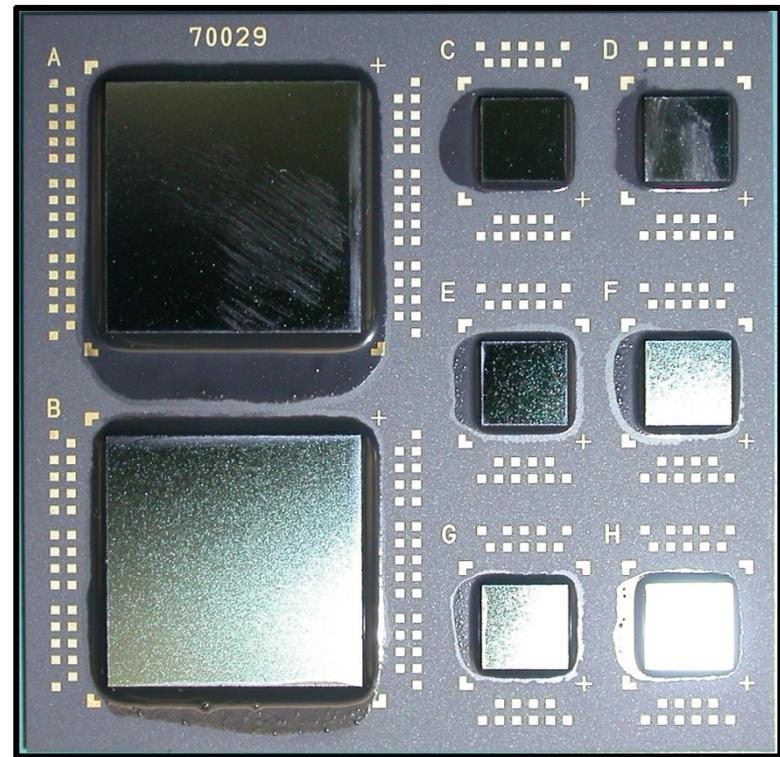
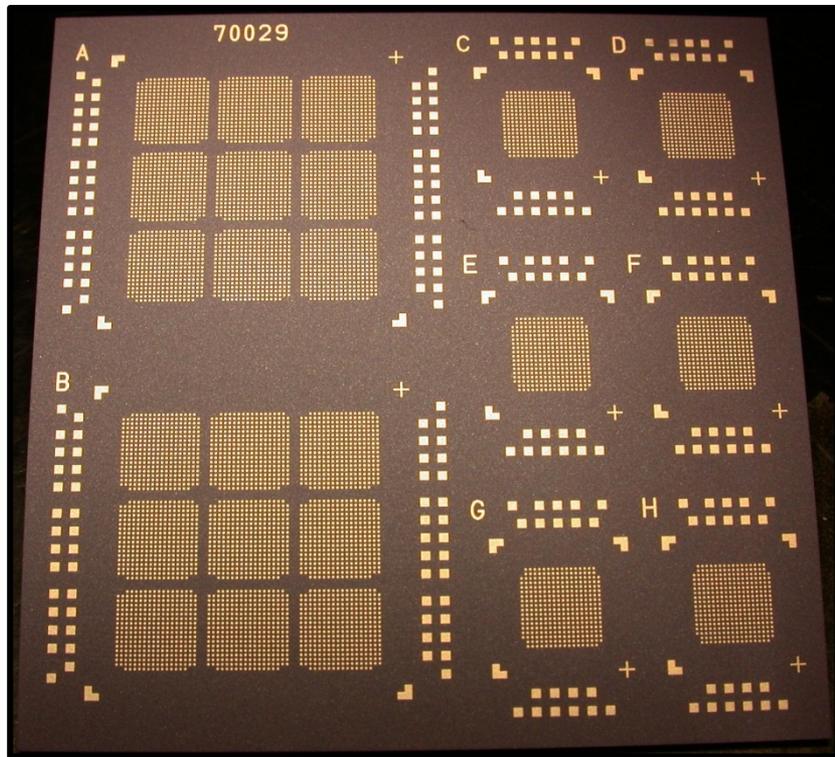
▼ QML Qualification

- 90nm ASIC technology QML-V qualification plan is in progress using “hermetic” flip chip assembly of a library test chip (LTC)
- 90nm Class Y package qualification plan is underway using the same LTC flip chip test vehicle but in a “non-hermetic” format

Flip Chip Assembly

▼ Daisy Chain Test Vehicle Assembly

- 1x1 die format: 5x 5mm die size with 317 I/O
- 3x3 die format: 15x15mm die size with 2,853 I/O



Flip Chip Assembly – 5x5mm and 15x15mm



▼ Flip Chip PIDTP Summary

Test Type	Test Method	Criteria	Status
Wafer Level Acceptance	Bump Yield Bump Height Bump Shear	Bump defect rate < 200 ppm Nominal +/- 15 µm Minimum load of 3 mg/µm ²	Pass
Die Shear Assembly Monitor	TM 2011, Condition F • Pre underfill	Minimum load of 5 gr/bump.	Pass
X-Ray Assembly Monitor	TM 2012 • Post underfill	Solder joint voids < 25% of bump diameter	Pass
CSAM Assembly Monitor	TM 2030 • Post underfill	Underfill void content < 10% of die area	Pass
Cross Section Assembly Monitor	IAW Aeroflex specification 49210 • Post underfill	0 defects allowed related to solder joints or underfill	Pass
Temperature Cycle	TM1010, Condition B • 250 cycle endpoints, or as appropriate • Test to failure, or 3000 cycles, whichever occurs first	Continuity endpoint testing; >15% increase in daisy chain resistance	Pass

Test Type	Test Method	Criteria	Status
CSAM Failure Analysis	TM 2030 • Post temperature cycle testing	Failure mode confirmation	Complete
Cross Section Failure Analysis	IAW Aeroflex specification 49210 • Post temperature cycle testing	Failure mode confirmation	Complete
125°C High Temperature Storage	JESD22-A103C • High temperature storage at 125°C and 150°C	Minimum load of 5 gr/bump	Pass
150°C High Temperature Storage	• Endpoints at 0, 250, 500, 750, 1500 and 2000 hours TM 2011, Condition F • Die shear at each endpoint • 6 die per endpoint; no underfill		
Multiple Reflow	JESD22-A113-B • Multiple reflows • Endpoints at 0, 1, 5, 10, 15 and 20 reflows TM 2011, Condition F • Die shear at each endpoint • 6 die per endpoint; no underfill	Minimum load of 5 gr/bump	Pass

▼ Objectives

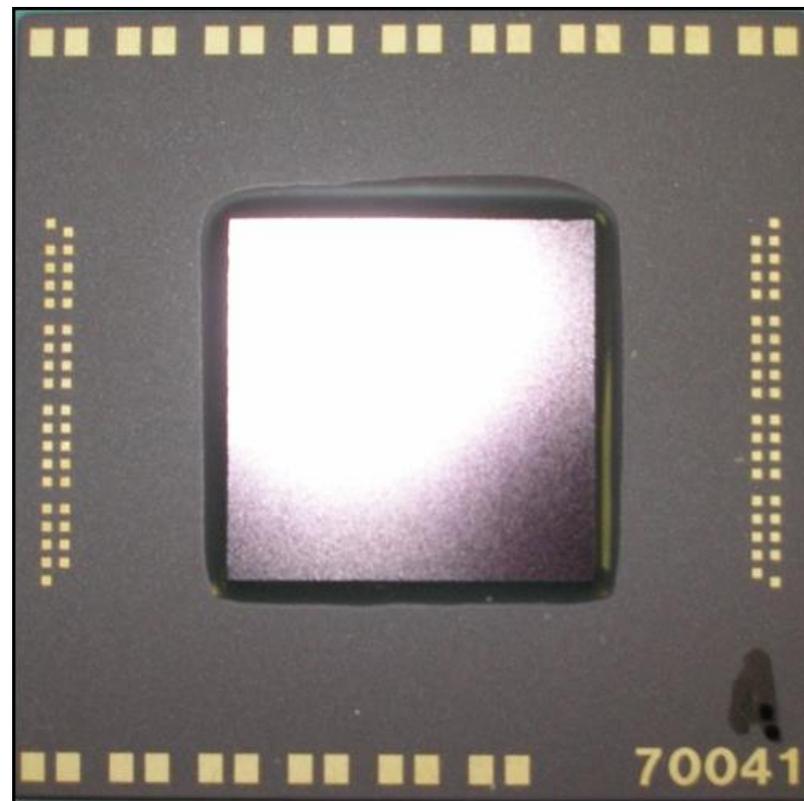
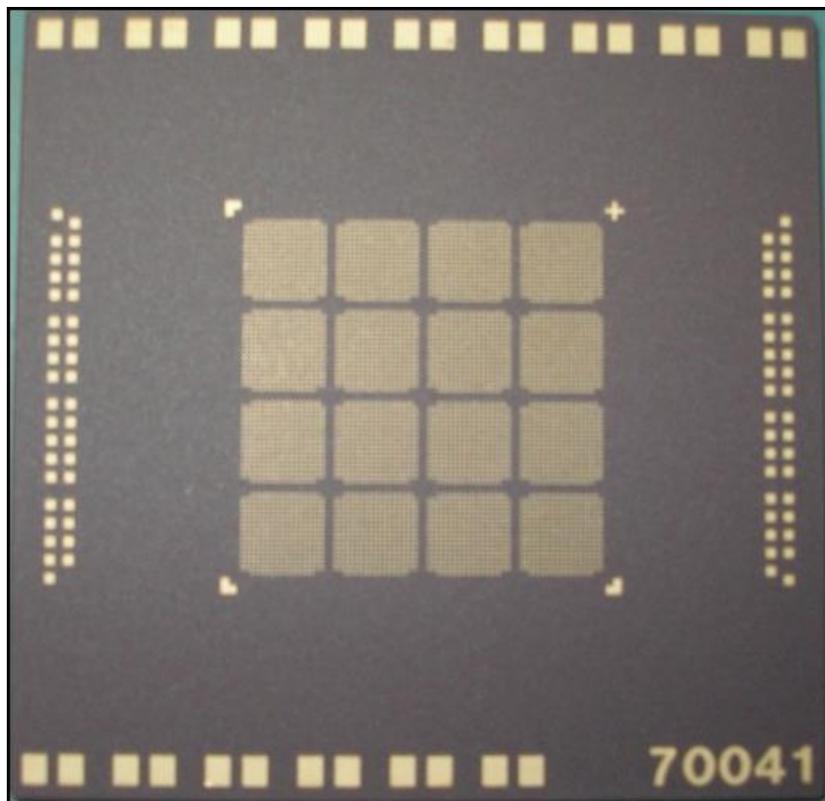
- Perform a reliability assessment on a large die flip chip test vehicle format
- Retire risk associated with large die flip chip assembly
- Increase the flip chip PIDTP envelope with respect to die size from 15x15mm to 20x20mm

▼ Test Vehicle

- 4x4 die format: 20x20mm die size with 5,072 I/O
- Single layer ceramic test substrate
- Same assembly process and material set as used in previous flip chip reliability assessments

Large Die Flip Chip – 20x20mm

▼ Large Die Daisy Chain Test Vehicle Assembly



Large Die Flip Chip – 20x20mm



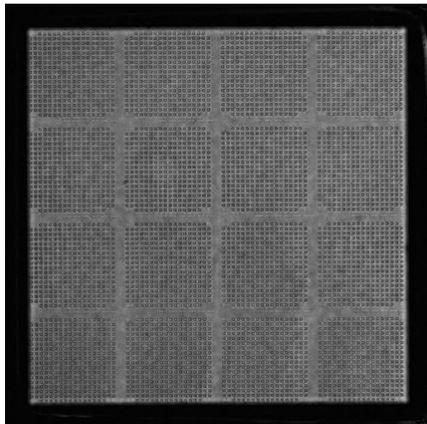
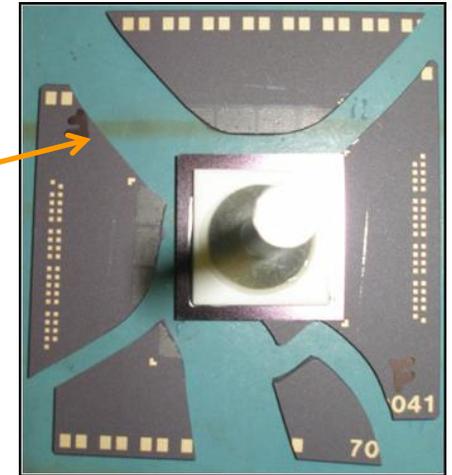
▼ Large Die Flip Chip PIDTP Summary

Test Type	Test Method	Criteria	Status
Flip Chip Pull-Off Test	TM 2031 • Pre underfill	Minimum load of 32kg	Pass
CSAM Assembly Monitor	TM 2030 • Post underfill	Underfill void content < 10% of die area	Pass
Stud Pull Test	TM 2027 • Post underfill	Minimum load of 11.4kg	Pass
Cross Section Assembly Monitor	IAW Aeroflex specification 49210 • Post underfill	0 defects allowed related to solder joints or underfill	Pass
Temperature Cycle	TM1010, Condition B • 250 cycle endpoints, or as appropriate • Test to failure, or 3000 cycles, whichever occurs first	Continuity endpoint testing; >15% increase in daisy chain resistance	Pass

Large Die Flip Chip – 20x20mm

▼ Stud Pull Assembly Monitor (Pass)

- Stud Pull performed per MIL-STD-883
- 3 parts tested pre and post underfill
- Pre underfill: 93 kg avg load (substrate fracture)
- Post underfill: 225 kg load cell limit without failure

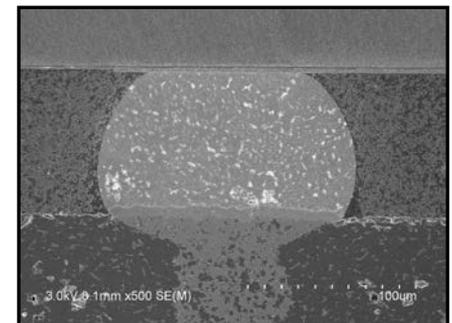


▼ CSAM Assembly Monitor (Pass)

- Performed on 4x4 FA10 assemblies
- No significant underfill voids detected

▼ Cross Section Assembly Monitor (Pass)

- No underfill or solder joint defects detected
- No underfill settling of silica particles



- ▼ **Condition B Temperature Cycling (Pass)**
 - 20 assemblies under test
 - Endpoint continuity testing every 250 cycles
 - Zero hour yield is 100%
 - 3000 cycle endpoint completed; no failures observed
 - Extended testing is in progress
 - ▼ We will continue to test until failure

Solder Column Attach

▼ Solder Column Attach PIDTP

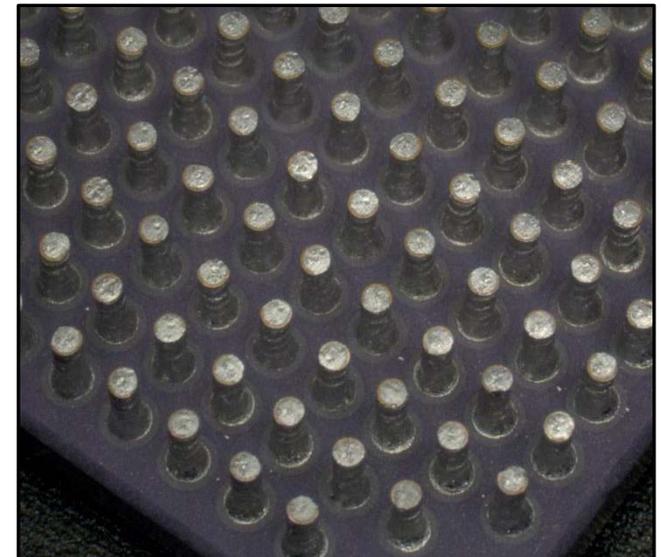
- Solder column attach PIDTP completed in October 2012
- Based on package level testing of Six Sigma columns

▼ Solder Column Attach QML Qualification

- Aeroflex QML qualification approval for use of Six Sigma solder column attach received February 2013
- Aeroflex completed implementation of QML flows in May 2013

▼ MIL-STD-883 TM2038

- Aeroflex authored the new MIL-STD-883 TM2038, Column Grid Array Package Destructive Lead Pull Test
 - ▼ To be included in next revision of MIL-STD-883



472 Ceramic CGA Test Vehicle

Solder Column Test Vehicle

1.27mm pitch

20 and 22mil diameter columns

▼ Solder Column Attach PIDTP Summary

Test Type	Test Method	Notes	Status
Visual Inspection	TM 2009. • Sample x-ray inspection	100% (visual) 2 parts (x-ray)	Pass
Solderability	Per J-STD-002C. • Surface mount simulation	1 standard part	Pass
Column Pull	Per proposed TM 2038 • 15 columns/part	3 standard parts 1 reworked part	Pass
Temperature Cycle	TM 1011 and 1010 • 15 cycles, Cond B per TM 1011 • 100, 500, 1000 cycle endpoints; Cond C per TM 1010 • Column pull per TM 2038	Per endpoint: 3 standard parts 1 reworked part	Pass

Test Type	Test Method	Notes	Status
125°C High Temperature Storage	Per JESD22-A103 • 125°C storage. • 100, 500, 1000 hour endpoints • Column pull per TM 2038	Per endpoint: 3 standard parts	Pass
150°C High Temperature Storage	Per JESD22-A103 • 150°C storage. • 100, 500, 1000 hour endpoints • Column pull per TM 2038	Per endpoint: 3 standard parts 1 reworked part	Pass
Multiple Reflow	JESD22-A113-B • Multiple reflows; eutectic profile • 1, 2, 3, 4 reflow endpoints • Column pull per TM 2038	Per endpoint: 1 standard part	Pass
Long Term Storage	Per J-STD-002C • Aged 2.5 and 7 years	1 standard part; pass solderability requirements	Pass

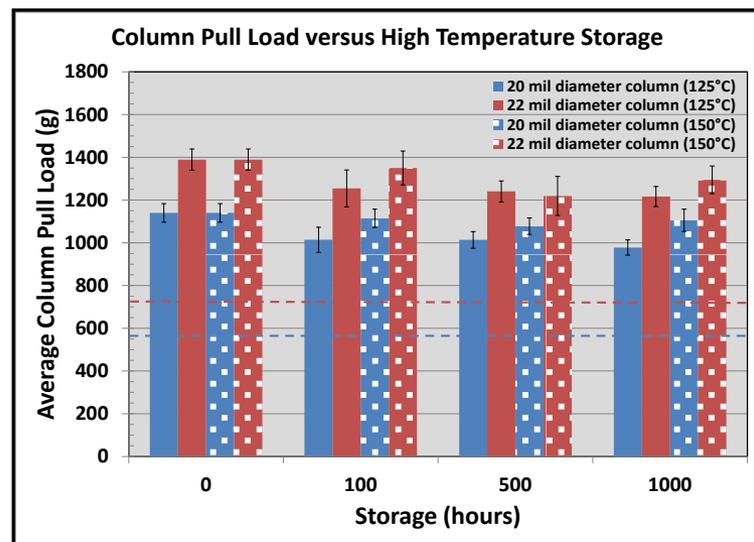
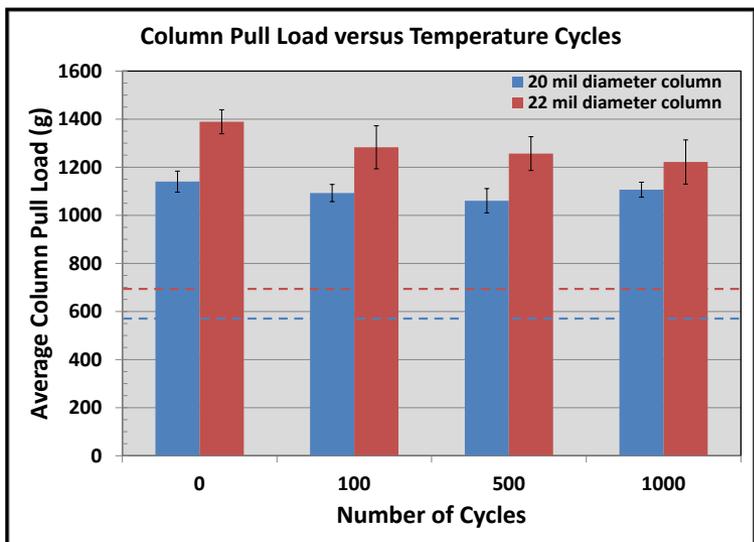
Notes:

- **Test Methods (TM)** refer to MIL-STD-883.
- **Duplicated** for both the 20 and 22 mil diameter column types.
- **All tests performed at the package level.**

Solder Column Attach



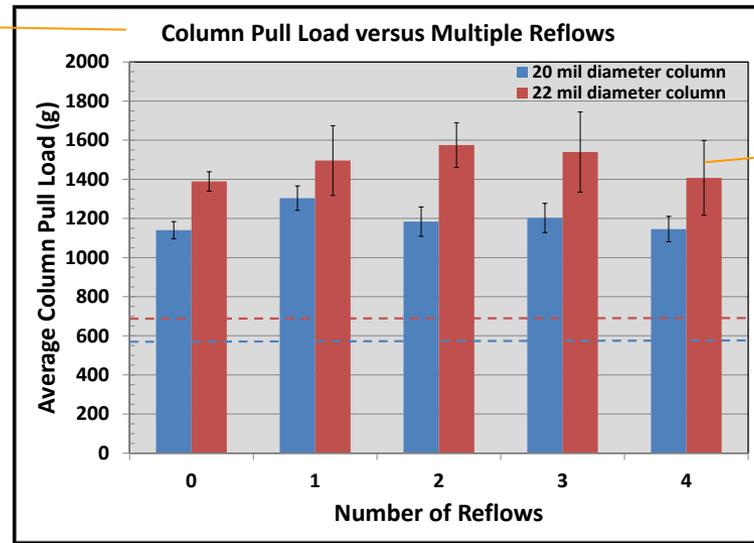
-65/150°C Temp Cycle



High Temperature Storage

Column Pull testing based upon new TM2038

Multiple Reflows



Std Dev

Lower spec limits for each column diameter

▼ Heat Sink Technology

- **AlSiC heat sink material in a “non-hermetic” lid configuration**
- **Heat sink staked to package corners**
- **Options to ground heat sink through package and/or die**

▼ Heat Sink Attach PIDTP

- **Design and procurement of test vehicle is in progress**
- **Execution of reliability assessments**
 1. **Temperature cycle, high temperature storage**
 2. **Monitor continuity of flip chip interconnects**
 3. **Monitor integrity of heat sink attach**

▼ Chip Cap Attach Technology

- Chip caps will be screened to MIL-PRF-123 requirements (per MIL-PRF-38535)
- The smallest available MIL-PRF-123 cap size is 0805
 - ▼ 80 x 50 x 55mils, 1pF to 18nF (Kemet)
- Assembly via eutectic Sn/Pb solder attach
- Underfill option to be evaluated

▼ Chip Cap Attach PIDTP

- Will utilize heat sink attach test vehicle
- Execution of reliability assessments
 1. Temperature cycle, high temperature storage
 2. Monitor continuity of chip cap connections
 3. Monitor integrity of chip cap attach via cap shear

- ▼ **Qualification of Class Y Flip Chip CGA package technology entails two basic components**
 1. **Completion of Package Integrity Demonstration Test Plans**
 2. **Execution of 90nm qualifications (QML-V and Class Y)**
- ▼ **Aeroflex is executing a MIL-PRF-38535 compliant Class Y qualification plan for its UT1752FC package**
 - **PIDTP plans have been completed for flip chip and CGA package technologies**
 - **PIDTP plans are in progress for chip cap attach and heat sink attach technologies**
 - **Execution of 90nm qualification plans are in progress**