QUALIFICATION OF CLASS Y FLIP CHIP CGA PACKAGE TECHNOLOGY FOR SPACE

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ABSTRACT

With the recent release of MIL-PRF-38535 Revision K, requirements have been defined for the use of ceramic non-hermetic packages in space applications, designated as Class Y. One of the requirements is the execution of a Package Integrity Demonstration Test Plan (PIDTP) for each new package technology.

The paper herein describes the UT1752FC Class Y flip chip column grid array package scheme under qualification by Aeroflex Microelectronic Solutions-HiRel in support of productization and qualification of its 90nm ASIC technology node and library. The paper further describes results from recently completed flip chip and solder column PIDTP reliability assessments, along with descriptions of ongoing assessments for heat sink attach and decoupling capacitor attach technologies.

1. INTRODUCTON

The December 2013 release of MIL-PRF-38535 Revision K defines for the first time a Class Y designation for the use of ceramic non-hermetic packages in space applications. Among other things, the Class Y designation allows for the use of non-hermetic flip chip package technology, which in turn enables heat sink attach directly to the backside of the ASIC die. In conjunction with solder column second level interconnects, this ceramic flip chip column grid array (CGA) package technology will drive the proliferation of ASIC large signal pin count, high speed applications for space.

MIL-PRF-38535 Revision K specifically requires a Package Integrity Development Test Plan (PIDTP) be executed for each non-traditional package assembly technology, including flip chip assembly, solder termination (i.e., solder columns), heat sink attach and decoupling capacitor attach technologies. These PIDTP reliability assessments are thus a prerequisite for an ASIC product qualification utilizing Class Y package technology.

Aeroflex Microelectronic Solutions-HiRel (Aeroflex) is in the process of developing and qualifying a Class Y 1752 I/O package in support of productization and qualification of its 90nm ASIC technology node and library. Designated UT1752FC, this package scheme utilizes the aforementioned technologies of flip chip, solder column, heat sink and decoupling capacitors, and hence requires corresponding PIDTP reliability assessments.

The flip chip PIDTP was performed utilizing a daisy chain test vehicle bumped by Flip Chip International [1] using their eutectic 63Sn/37Pb Standard Flip Chip wafer bumping process. The test vehicle was assembled to a ceramic test substrate in both 5x5mm and 15x15mm die configurations. Reliability assessments were then completed for temperature cycling, high temperature storage and multiple reflow testing. In order to increase the die size envelope, subsequent PIDTP assessments were performed on a 20x20mm die configuration.

Solder column PIDTP assessments were performed on solder columns attached to ceramic land grid array (LGA) packages by Six Sigma [2]. Temperature cycling, high temperature storage and multiple reflow testing were performed at the package level, with solder column pull testing utilized as a monitor to detect any degradation in column attach integrity.

Ultimately the results of the flip chip and solder column PIDTP assessments demonstrate the high reliability of the first and second level interconnects of the Aeroflex Class Y ceramic flip chip CGA package scheme. The paper closes with descriptions and status of ongoing PIDTP assessments for heat sink and decoupling capacitor attach package technologies.

2. UT1752FC CLASS Y PACKAGE

Fig. 1 shows a schematic of the Class Y package scheme designated UT1752FC. This 1752 I/O package utilizes flip chip die attach technology with solder column I/O terminations. A non-hermetic heat sink lid is attached directly to the die backside for efficient heat removal, and is also staked at the package corners for

robust mechanical stability and grounding. The lid design also mechanically protects the die and decoupling capacitors (i.e., chip caps).

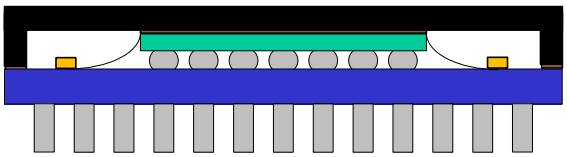

Figure 1. UT1752FC Class Y package scheme.

A summary of the UT1752FC Class Y package scheme is as follows.

- 1752 package I/O on a 1.00mm pitch
- 45x45mm package footprint
- Ceramic substrate technology
- LGA or CGA format
- Aeroflex UT90nHBD die
- Eutectic 63Sn/37Pb wafer bumping
- Aeroflex flip chip assembly
- Aeroflex chip cap attach
- AlSiC heat sink lid technology
- Six Sigma solder column attach
- MIL-PRF-38535 Class Y qualified

Per MIL-PRF-38535 Revision K, PIDTP assessments have been performed on the flip chip assembly and solder column attach technologies. Heat sink and chip cap attach PIDTP assessments are in progress. Status for all PIDTP assessments is provided in the following sections.

3. FLIP CHIP ASSEMBLY PIDTP

Aeroflex completed internal flip chip reliability assessments in 2010 that are summarized in [3,4]. A failure mode effects analysis (FMEA) has since been completed, and combined with the reliability assessments, constitutes the preliminary flip chip PIDTP completed in 2011, results of which were presented to the JEDEC Class Y G-12 Task Group [5]. The flip chip PIDTP has recently been expanded to include large die reliability assessments in order to increase the die size envelope.

The flip chip PIDTP and large die PIDTP assessments are described in the following sections.

3.1. FA10 Flip Chip Test Vehicle

The test vehicle employed for the flip chip PIDTP is the FA10 daisy chain vehicle described in detail in [3]. The FA10 test die contains bumped flip chip I/O on a 254µm pitch. In its 5x5mm format, there are 317 flip chip I/O. Diced into its 15x15mm format (i.e., a 3x3 array of the 5x5mm format), there are 2,853 I/O.

The FA10 test substrate is a single layer, single sided ceramic substrate, 1.0mm thick and 45x45mm in size. It contains six sites for the 5x5mm FA10 die and two sites for the 15x15mm FA10. Landing pad sizes are 127µm in diameter and plated with an electroless nickel/immersion gold (ENIG) pad finish. The flip chip I/O are daisy chained in pairs through the FA10 test substrate.

The FA10 wafers were bumped by Flip Chip International (FCI) using their Standard Flip Chip (SFC) wafer bumping process [1]. The wafers were bumped with eutectic 63Sn/37Pb solder alloy and the standard FCI Al/NiV/Cu under bump metallurgy (UBM).

Flip chip assembly was performed by Aeroflex using their proprietary assembly processes and material set. Parts were assembled with and without underfill, depending on the target reliability assessment.

Fig. 2 shows a schematic of the FA10 die in its 5x5mm format, as well as 5x5mm and 15x15mm die assembled to the FA10 ceramic test substrate.

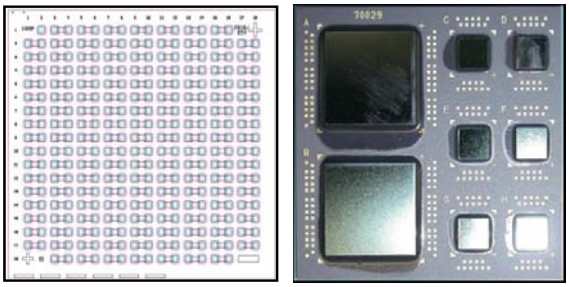

Figure 2. FA10 flip chip test vehicle [3,4].

3.2. Flip Chip Assembly PIDTP Results

Tab. 1 summarizes the results for the flip chip PIDTP. Details on wafer level acceptance results can be found in [3,4,5]. Bump height average across 10 wafers averaged 106µm with an average deviation of 1.9 µm. The bump defect rate across 10 wafers was 31 ppm. And the bump shear resulted in a normalized load of 4.0mg/ μm^2, well above the limit of 3.0mg/ μm^2. In short, the bump height, yield and shear data all passed wafer level acceptance requirements.

Similarly, details on results for die shear, CSAM and X-ray and cross section assembly monitors can also be found in [3,4,5]. Die shear is performed pre underfill so as to monitor the solder interconnect reflow process. CSAM is performed post underfill in order to detect voids or delamination. Die shear test results easily meet limits defined in MIL-PRF-883 Test Method 2011. And the CSAM analysis detected no evidence of voids or delamination. Likewise, X-ray and cross section analysis showed no solder joint defects, nor any issues

with the underfill process.

Table 1. Flip chip assembly PIDTP summary.

Test Type	Details	Status
Wafer Level Acceptance	Bump Height, Bump Yield, Bump Shear	**Pass**
Die Shear	TM2011, Condition F (pre underfill)	**Pass**
CSAM	TM2030 (post underfill)	**Pass**
Assembly Monitors	X-ray, TM2012 Cross Section	**Pass**
Temperature Cycle	TM1010, Condition B	**Pass**
Failure Analysis	CSAM, TM2030 Cross Section	**Pass**
125°C High Temp Storage	JESD22-A103 TM2011, Condition F	**Pass**
150°C High Temp Storage	JESD22-A103 TM2011, Condition F	**Pass**
Multiple Reflow	JESD22-A113-B TM2011, Condition F	**Pass**

1. Test Methods (TM) refer to MIL-STD-883.
2. HTS and MR response is die shear of six 5x5mm die at each endpoint (without underfill).

Temperature cycling was completed per the Test Method 1010 Condition B profile, with minimum and maximum temperatures of -55°C and 125°C, respectively. Per the test method, transition rates between the two extremes are relatively fast, and mimic a thermal shock type of profile, as opposed to slower transition rates associated with a thermal cycle condition found in typical use conditions. The effect of transition rate is described in detail in [3,4], with the high transition rate resulting in an underfill breakdown failure mechanism, as opposed to solder fatigue of the flip chip interconnects [6,7].

Nonetheless, temperature cycle results for the 5x5mm and 15x15mm FA10 die easily pass the minimum requirement of 1,000 cycles, and extended temperature cycle minimum of 2,000 cycles. In fact, the 5x5mm FA10 flip chip assemblies completed 12,000 cycles without a single failure (failure defined as a 15% or greater increase in daisy chain resistance). The 15x15mm FA10 flip chip assemblies were tested to failure, resulting in a Weibull life of 3,576 cycles.

CSAM and cross section failure analysis confirmed that underfill breakdown was indeed the failure mechanism leading to open solder joints. As described in [3,4], the high transition rates lead to the formation of cracks within the underfill fillets. These cracks eventually propagate to the die/underfill interface, and run through solder interconnects, leading to an open failure.

UBM consumption is the complete conversion of the UBM metallization into intermetallic compounds, and is typically excited via high temperature storage testing. Hence high temperature storage testing was performed on 5x5mm FA10 assemblies at 125°C and 150°C. Parts were assembled with no underfill so as to isolate the effect of any UBM consumption. At each endpoint of 0, 250, 500, 750, 1500 and 2000 hours, test substrates populated with six die were removed for die shear testing. A significant drop in subsequent die shear load would indicate catastrophic UBM consumption.

Fig. 3 shows the high temperature storage die shear results for 125°C and 150°C. The lower spec limit is based on TM 2011 Condition F, which stipulates a minimum of 5 grams per solder interconnect for flip chip die shear. For the 317 I/O count of the 5x5mm FA10 die configuration, the lower spec limit is then calculated to be 1.585kg.

The results in Fig. 3 show a slight degradation in shear load due to initial grain coarsening of the solder. This is expected for all Sn/Pb solder connections and typically results in a drop in shear load of approximately 15 percent. However, even after 2,000 hours of high temperature storage at 125°C the shear loads are well above the lower spec limit defined by TM 2011, indicating no critical UBM consumption has occurred. Indeed, corresponding C_{pk} values for the shear data of Fig. 3 are all well above the 1.33 minimum industry standard.

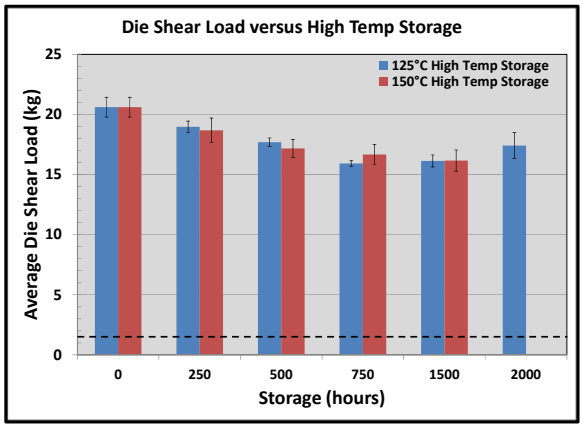

Figure 3. Flip chip high temperature storage results.

UBM dissolution is the complete dissolution of UBM metallization into molten solder, and is typically excited via multiple reflow testing. Hence multiple reflow testing was performed on 5x5mm FA10 assemblies. Similar to the high temperature storage testing flow, parts were assembled without underfill so as to isolate the effect of any UBM dissolution, and then subjected to multiple eutectic Sn/Pb solder reflows. At each endpoint of 0, 1, 5, 10, 15 and 20 reflows, test substrates populated with six die were removed for die shear testing. A significant drop in subsequent die shear load would indicate catastrophic UBM dissolution.

Fig. 4 shows the multiple reflow die shear results, with the lower spec limit again defined by TM 2011 as 1.585kg. As can be seen, the die shear loads are well above the lower spec limit, with corresponding C_{pk} values well above the 1.33 minimum. The slight dip in die shear load at the 15 reflow endpoint is due to the elapsed time between reflow and die shear test. For this endpoint, the parts sat at room temperature for approximately 72 hours, allowing for grain coarsening of the solder. For the other reflow endpoints, die shear was performed within 12 hours, resulting in more consistent, and higher, die shear loads. Again, this phenomenon is an artifact of Sn/Pb solder, and not an indication of any critical level of UBM dissolution.

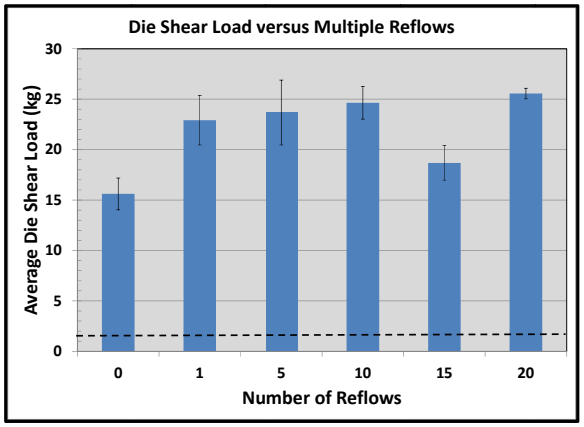

Figure 4. Flip chip multiple reflow results.

3.3. Large Die Flip Chip PIDTP

Thus far, the largest flip chip die evaluated has been the 15x15mm FA10 format described above. In order to increase the flip chip die size envelope, and in turn the PIDTP, a 4x4 array of the FA10 die has since been evaluated. The 4x4 array results in a die size of 20x20mm, and a flip chip I/O count of 5,072. Fig. 5 shows the corresponding 20x20mm FA10 test substrate and flip chip assembly. Note that assembly was performed using the same flow and material set as for the 5x5mm and 15x15mm FA10 assemblies described above. Tab. 2, in turn, summarizes the results for the 20x20mm FA10 (i.e., large die) flip chip PIDTP assessments.

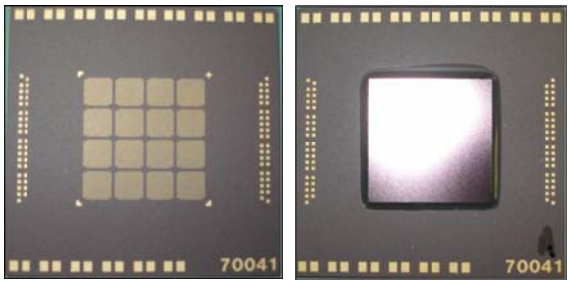

Figure 5. 20x20mm FA10 flip chip test vehicle.

Table 2. Large die flip chip PIDTP summary.

Test Type	Details	Status
Flip Chip Pull-Off Test	TM2031 (pre underfill)	**Pass**
CSAM	TM2030 (post underfill)	**Pass**
Stud Pull Test	TM2027 (post underfill)	**Pass**
Assembly Monitor	Cross Section	**Pass**
Temperature Cycle	TM1010, Condition B	**Pass**

1. Test Methods (TM) refer to MIL-STD-883.

Due to die size and load cell limitations, flip chip pull-off testing per TM 2031 was performed instead of die shear. Note that this pre underfill assembly monitor option exists per MIL-PRF-38535 Revision K. The average pull test load was 93kg, well above the lower spec limit of 32kg defined by TM 2031. The failure mode was substrate fracture, as shown in Fig 6.

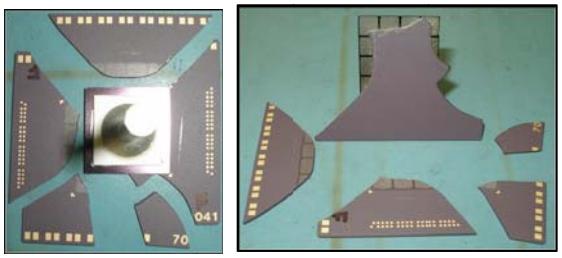

Figure 6. 20x20mm FA10 stud pull failure mode.

Stud pull tests were performed post underfill per TM 2027 (again, an option per MIL-PRF-38535). In this

case, the test substrate was reinforced prior to stud pull so as to prevent substrate fracture. For all three parts tested, the load cell limit of 225kg was reached prior to any failure. This limit is well above the lower spec limit defined in TM 2027.

CSAM analysis was performed to detect any underfill void content. This is especially critical as die size is increased, as voiding is more apt to occur. However, as Fig. 7 show, no significant underfill voiding was detected for the 20x20mm FA10 assemblies.

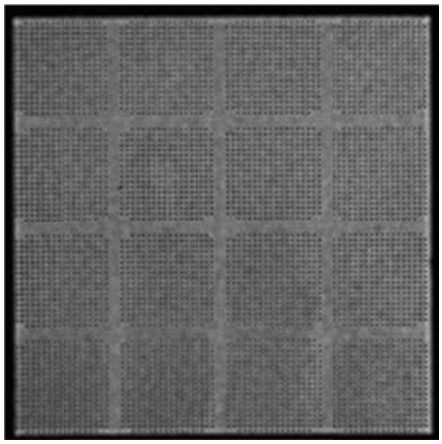

Figure 7. 20x20mm FA10 underfill CSAM analysis.

Similarly, cross section analysis showed no assembly anomalies. Fig. 8 shows cross sections of flip chip interconnects moving from left, to center, to right die edge. Note the effect that the thermal expansion mismatch between the die and substrate has on the formation of the flip chip interconnects at this large a die size. As of this writing, however, the large die 20x20mm FA10 flip chip assemblies have been subjected to 3,000 Condition B thermal cycles with no failure detected. Temperature cycling will continue to failure, and results will be reported at a future date.

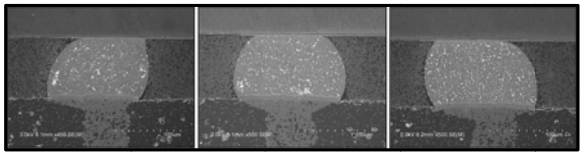

Figure 8. 20x20mm FA10 assembly cross section.

4. SOLDER COLUMN PIDTP

Six Sigma offers a solder column attach process, QML certified by the Defense Logistics Agency (DLA), that converts land grid array packages into solder column grid array packages. The reader is directed towards [2] for details on the Six Sigma solder column construction and attach process.

In an effort to qualify Six Sigma solder columns for QML package configurations (QML-V and Class Y), Aeroflex has completed a PIDTP assessment at the package level evaluating the robustness of the Six Sigma solder column attach integrity. Tab. 3 summarizes the solder column attach PIDTP results. Note that each test listed in Tab. 3 was duplicated for both 20mil (0.51mm) and 22mil (0.55mm) diameter columns.

Table 3. Solder column attach PIDTP summary.

Test Type	Description	Status
Visual Inspection	TM2009	**Pass**
Solderability	J-STD-002C	**Pass**
Column Pull	TM2038	**Pass**
Temperature Cycle	TM1011, Condition B TM1010, Condition C TM2038, Column Pull	**Pass**
125°C High Temp Storage	JESD22-A103 TM2038, Column Pull	**Pass**
150°C High Temp Storage	JESD22-A103 TM2038, Column Pull	**Pass**
Multiple Reflow	JESD22-A113-B TM2038, Column Pull	**Pass**
Long Term Storage	J-STD-002C, Solderability	**Pass**

1. Test Methods (TM) refer to MIL-STD-883.
2. Tests duplicated for both 22 and 20 mil diameter columns.
3. All tests performed at the package level.

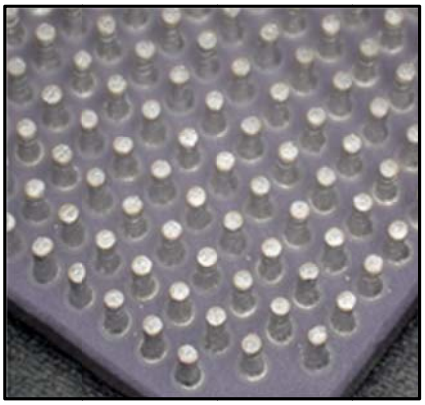

Figure 9. 472 ceramic CGA solder column test vehicle.

The test vehicle used for the package level PIDTP evaluations is a 472 LGA package (1.27mm I/O pitch) with solder columns attached by Six Sigma using their standard QML process flow. A representative picture of this test vehicle is shown in Fig. 9. These parts passed visual inspection to TM 2009, as well as solderability testing to JEDEC standard J-STD-002C.

The temperature cycle, high temperature storage and multiple reflow tests listed in Tab. 3 all rely on column pull testing as a response. Column pull testing is based on the newly created Test Method 2038, to be included in the next revision of MIL-STD-883. This test method was created in part from the PIDTP work completed by Aeroflex.

For the temperature cycle testing, three parts each with 20 and 22mil diameter columns attached were subjected to 15 cycles of Condition B (-55/125°C) thermal shock pre-condition per TM 1011, followed by Condition C temperature cycling (-65/150°C) per TM 1010. Endpoints were defined at 0, 100, 500 and 1,000 temperature cycles. At each endpoint, column pull tests were performed on 15 columns per part.

Fig. 10 shows the average solder column pull results as a function of number of temperature cycles. The error bars represent the standard deviation. Note that there are separate lower spec limits for each column diameter, as shown in the figure. The 22mil diameter columns pull at a higher load than the 20 mil diameter columns, proportional to the difference in cross sectional area. For both column diameters, no degradation in pull load is observed after 1,000 cycles. Further, the average loads are well above the lower spec limits. Indeed, corresponding C_{pk} values are above 1.33 in all cases.

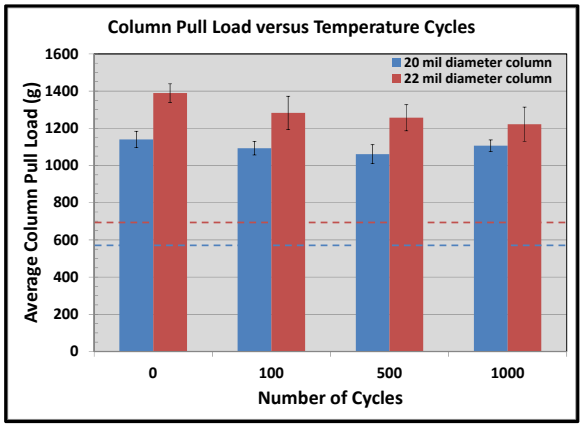

Figure 10. Solder column temperature cycle results.

For the high temperature storage testing, separate groups of three parts each with 20 and 22mil diameter columns attached were subjected to 125°C and 150°C storage. Endpoints were defined at 0, 100, 500 and 1,000 hours. At each endpoint, column pull tests were performed on 15 columns per part.

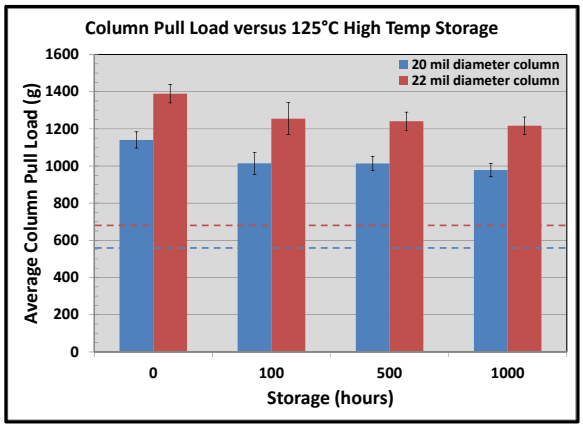

Figure 11. Solder column 125°C HTS results.

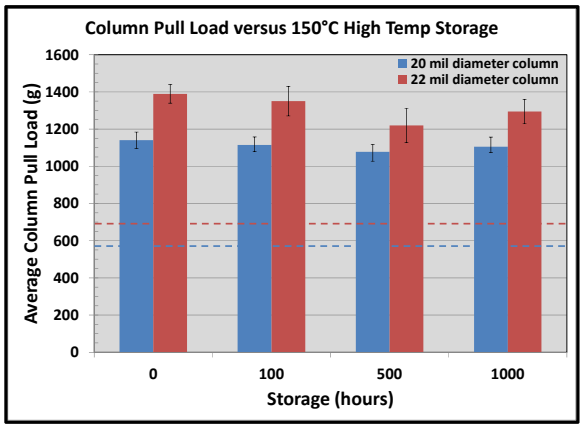

Figure 12. Solder column 150°C HTS results.

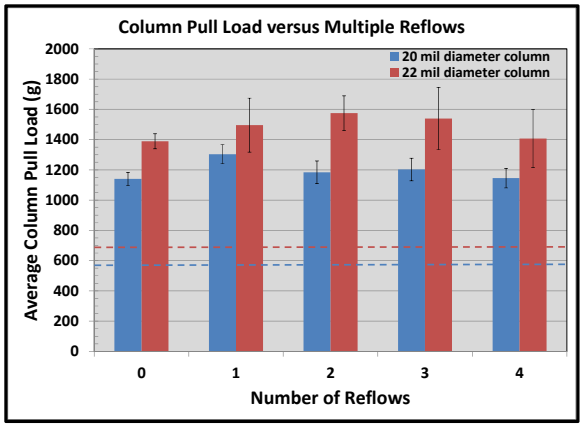

Figure 13. Solder column multiple reflow results.

Figs. 11 and 12 show average column pull results as a function of high temperature storage at 125°C and 150°C, respectively. As with the temperature cycle results, no degradation in column pull load is observed

after 1,000 hours of high temperature storage. Average loads are well above the lower spec limits, and C_{pk} values above 1.33.

For the multiple reflow testing, one part each with 20 and 22mil columns attached were subjected to four cumulative eutectic reflows profiles. The reflow profile used mimics that for a 63Sn/37Pb board level assembly process. After each reflow, column pull tests were performed on 15 columns per part.

Fig. 13 shows column pull results as a function of number of reflows. For both column diameters, no degradation in pull load is observed after four reflow exposures.

In order to evaluate solder column shelf life, solderability tests were performed on parts from three groups aged at room temperature conditions in ambient air (i.e., a non-nitrogen environment). Specifically, 20 and 22mil diameter column parts were aged for 2.5 years, while a separate lot of 22 mil diameter column parts was aged for 7 years.

Solderability tests were performed in accordance with JEDEC standard J-STD-002C, following the surface mount process simulation test protocol for eutectic solder. Three parts from each of the three groups were tested (nine parts total), encompassing all solder columns from each part. Visual inspection of the parts per J-STD-002C deemed the parts to have passed solderability test requirements. Based on this successful solderability testing, shelf life is defined as up to 7 years stored at room temperature and ambient air conditions.

Aeroflex has successfully completed the solder column attach PIDTP evaluations, and has since completed a product qualification plan that has led to QML certification for the use of Six Sigma solder column attach to Aeroflex LGA packages.

5. HEAT SINK ATTACH PIDTP

The UT1752FC heat sink approach is to utilize AlSiC heat sink material in a lid configuration (refer to Fig. 1). The coefficient of thermal expansion (CTE) of AlSiC (9ppm/°C) is a better match to ceramic (6ppm/°C) and silicon (3ppm/°C) compared to copper (17ppm/°C), thus minimizing thermal stresses among these adjoined materials. Further, AlSiC provides a high level of thermal conductivity (185W/m-K) in a relatively light weight format (density 3g/cm3). Ultimately, AlSiC provides the optimum combination for reliability, thermal performance and weight.

The heat sink lid configuration was chosen in large part for two general reasons. First, it provides physical protection for the decoupling capacitors. Second, it allows for grounding of the heat sink directly to the package instead of through the die, through the use of both conductive and non-conductive thermal interface heat sink attach materials.

Aeroflex is in the process of designing and procuring test vehicles with which to perform PIDTP assessments for heat sink attach technologies. Once these test vehicles are assembled they will be subjected to accelerated testing, such as high temperature storage and temperature cycling. Results from these evaluations will be presented as they become available.

6. CHIP CAP ATTACH PIDTP

In 2007 Aeroflex qualified a chip capacitor attach process for assembly of 1210 chip caps to the package exterior. This process was certified for use on QML-V package formats. However, this 1210 chip cap attach technology is not compatible with the Class Y scheme of the UT1752FC package due to size constraints. Hence a new chip cap attach technology must be qualified, and hence requires a corresponding PIDTP.

MIL-PRF-38535 specifies that capacitors be screened to meet or exceed MIL-PRF-123 requirements in order to be used for Class Y applications. The smallest available chip capacitor commercially available and screened to MIL-PRF-123 is the 0805 cap size. Thus Aeroflex has initiated the development of an 0805 chip cap attach assembly process for use in its UT1752FC package.

Aeroflex intends to use the same test vehicles targeted for heat sink attach PIDTP evaluations for its chip cap attach PIDTP evaluations. Again, results from these evaluations will be presented as they become available.

7. CONCLUSIONS

The release of MIL-PRF-38535 Revision K has officially enabled the use of ceramic non-hermetic package technology for space applications. However, this Class Y technology advancement requires upfront diligence in the form of Package Integrity Demonstration Test Plan evaluations that ensure equivalent reliability to existing hermetic QML-V package technologies (e.g., silver-glass die attach, aluminium wedge wirebond and solder lid attach in a leaded package format). As such, Aeroflex has successfully completed PIDTP evaluations for flip chip assembly and solder column attach technologies in support of development and qualification of their UT1752FC package scheme. This package technology will in turn support productization and qualification of its 90nm ASIC technology node and library.

The qualification of Class Y ceramic flip chip CGA package technology entails, in part, two basic components. The first is to complete PIDTP reliability

evaluations as described above. The second is to execute product qualification plans that demonstrate and certify the reliability of these technologies for use in QML package formats. Aeroflex has successfully completed product qualifications that have certified the use of solder columns in a QML column grid array package format. In addition, 90nm qualification plans are currently being executed that will certify the use of flip chip assembly technology in Class Y formats.

To enhance thermal and performance capability of its Class Y package configuration, Aeroflex is also executing PIDTP evaluations for heat sink and decoupling capacitor attach technologies. Once completed, and corresponding product qualifications are completed, these technologies will also be certified as suitable for Class Y applications.

The results of the flip chip and solder column PIDTP assessments demonstrate the high reliability of the first and second level interconnects of the Aeroflex Class Y UT1752FC package technology scheme. Moreover, they demonstrate the feasibility and potential (i.e., the validity) of using non-hermetic Class Y technology in space applications.

8. REFERENCES

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