ENEPIG FINISH: AN ALTERNATIVE SOLUTION FOR SPACE PRINTED CIRCUIT BOARDS

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ABSTRACT

PCBs with fused tin/lead are qualified, manufactured, procured and used for Space applications. However, fused tin/lead is a non-planar finish which is not ideal for fine-pitch applications. Therefore, other finishes are provided by the PCB manufacturers for high reliability applications such as avionics or railway transportation. Another advantage of these finishes is that they meet the European legislation directive banishing lead in electronic equipment. The choice of PCB surface finish is a very important decision. It impacts assembly capability, PCB shelf life, solder joint reliability, cost and on-time delivery performance.
In this context, selecting a lead-free alternative surface finish in order to meet future requirements becomes a real challenge for Space industry. The current need in terms of finishes is mainly to keep the same level of reliability with minor impact on process. Future needs are mainly linked to pad size reduction and footprints planarity.
ENEPIG (Electroless Nickel/Electroless Palladium/ Immersion Gold) is emerging as a finish offering technical benefits for users and assemblers. The ENEPIG finish is an interesting alternative to ENIG (Electroless Nickel/Immersion Gold). In contrast to ENIG, ENEPIG is claimed to not be inclined to the "black pad" defect. In ENEPIG, electroless palladium is deposited onto the nickel phosphorus layer and is then finished with immersion gold.
In this study, a selection and analysis of ENEPIG bare boards is first performed which is then followed by a full reliability evaluation of assembled test vehicles. The performance of the assembled boards will be compared with fused tin/lead boards considering:

- tin/lead process and tin/lead packages
- two PCB suppliers
- two different ENEPIG chemistries
- various package types (CCGA, SMD, LCC, CQFP, resistors and other critical devices)
- different assembly processes (automatic, semi-automatic and manual)
- two OEM processes

The objective with this paper is to give a first status on ENEPIG as an alternative to fused tin/lead used for Space applications.

Key words: Surface Finish, PCB, ENEPIG, Space

1. BACKGROUND

Decrease of component pitch (CCGA up to 1500 I/Os with 1 mm pitch, small leadless chips and active components) highlights the need to have flat pads in order to allow accurate placement of components. Furthermore, the European legislation directive, banishing lead from electronic equipment, has driven the need for new PCB surface finishes even if Space industry is not directly affected by this directive.
Therefore, PCBs with fused tin/lead are still today qualified, manufactured, procured and used for Space applications. However, other finishes (immersion tin, immersion silver, ASIG, ENIG and ENEPIG) are provided by the PCB manufacturers for high reliability applications such as railway transportation and avionics. In order to meet future needs for Space applications in terms of PCB finishes, alternatives to reflowed tin/lead shall be evaluated.
The choice of PCB surface finish is a very important decision. It impacts assembly capability, PCB shelf life, solder joint reliability, cost and on-time delivery performance.
In this context, selecting a lead-free alternative surface finish becomes a real challenge for Space industry. The current need in terms of finishes is mainly to keep the same level of reliability with minor impact on manufacturing processes. Regarding the future, needs is mainly linked to pad size reduction and footprints planarity.

2. STATE-OF-THE-ART

When selecting a surface finish on PCB, there are several factors to consider:

- Fine pitch requirements
- Higher soldering temperatures and longer times for lead free soldering
- Compatibility with new lead-free regulations
- Multiple assembly operations
- Ability to rework if necessary
- Corrosion concerns
- Shelf life of the coating
- Overall end-user reliability requirements
- Cost to produce the boards, including the overall final finish cost

ENIG finish is widely used in the electronic industry. The main drawback of this finish is its inclination to form the black pad defect. This defect stays a low level defect but it cannot be detected prior to or after assembly without using destructive analyses. Thus, this defect can be critical for equipments. Therefore it has been Space position not to use ENIG.

ENEPIG was developed in the mid-1990s as a finish for PCBs. It did then never reach widespread use due to reliability problems when soldering using SnPb solder, maybe due to a too thick Pd layer. However, there has been a renewed interest for the finish during the last 10 years, but then mainly on substrates for plastic BGA components with wire-bonded chips. Since ENEPIG is both solderable and bondable, it is an ideal finish for BGA substrates and has often been described as the "universal finish". That is not entirely true since the Pd thickness needed to achieve good bondability is too thick for achieving reliable solder joints. Another often claimed advantage with ENEPIG is that it is not inclined to form black pad [1].

When soldering to ENEPIG, both the Au and Pd layers are completely dissolved in the solder and the solder joint is formed to the underlying Ni. Excellent solder joint reliability has been reported for SnAgCu (SAC) solder joints to ENEPIG [1, 2]. The IMC layer formed with SAC solder is quite thin consisting of $(Cu,Ni)_6Sn_5$ and/or $(Ni,Cu)_4Sn_3$. As for ENIG, the uppermost part of the Ni(P) layer is depleted of Ni leaving a layer with Ni_3P. Since the time for dissolving the Au and Pd layers will decrease the time the Ni is exposed to the melted solder, the Ni_3P will normally be thinner compared to when soldering to ENIG. This is believed to contribute to the better reliability compared to solder joints to ENIG. As for ENIG, a thin layer (50-100 nm) of Ni-Sn-P is formed on top of the Ni_3P layer [2].

The growth rate of the IMC layer formed using SAC solder is quite low at high use temperatures [2, 3]. This is also believed to contribute to the high reliability of SAC solder joints to ENEPIG.

In contrast to solder joints with SAC solder, the IMC layer formed with SnPb and SnAg solders are quite thick and irregular [2, 3]. Sometimes, the IMC layer may more or less completely spall off. Furthermore, the growth rate of the IMC layer is rather high at high use temperatures [2]. Several studies have shown that SnPb and SnAg solder joints are quite prone to brittle fractures in the solder joints, especially after aging at high temperatures. The irregular IMC layers, and especially spalled-off IMC layers, are believed to cause the formation of a thicker Ni_3P layer that reduces the integrity of the solder joints.

It has been shown that addition of about 1% Cu to SnPb solder results in an IMC layer similar to the IMC layer formed with SnAgCu solder [3]. Thus, Cu in the solder seems to be essential for forming a thin IMC layer that does not spall off.

In order to achieve reliable solder joints, it is essentially that the Pd layer is not too thick. When using SAC solder, it is generally recommended that the thickness of the Pd should be less than 0.1-0.2 µm [3, 4]. Maybe the Pd layer should be even thinner to achieve reliable solder joints with SnPb solder. The thickness of the Au layer has less impact on the reliability of the solder joint.

The thicknesses of the Pd and Au layers are usually determined using X-Ray Fluorescence (XRF) measurements. The committee responsible for the IPC standard IPC-4566 specifying requirements for ENEPIG performed an extensive round robin testing of XRF equipment capability to accurately measure the thicknesses of the Pd and Au layers [5]. The results showed a number of critical issues with equipment, set-up, measuring protocols and reference standards. It was concluded that it is imperative to demonstrate measurement capability in order to meet specified thickness requirements.

3. NI/PD/AU THICKNESS REQUIREMENTS

The IPC standard-4556 defines thickness requirements for the different layers of finishes [5]. This document does not differentiate thickness according to the assembly process (tin-lead or SAC). Required values are the following:

Ni layer: 3-6 µm
Pd layer: 0.05-0.30 µm
Au layer: >0.030 µm

Based on optical inspections and shear tests on BGAs, certain ENEPIG suppliers rather recommend reducing Pd thickness to 0.05 µm or even below for SnPb assembly process. Gold layers thicknesses could also be increased up to 0.15 µm.

4. TEST BOARDS DESCRIPTION

In Phase 1 of the project, positive results were demonstrated after procurements and analysis of ENEPIG bare boards, based on the ECSS-Q-ST-10C qualification. The ENEPIG finishes manufactured by two different suppliers showed very cosmetic appearances with homogeneous thicknesses. The only observed disadvantage with ENEPIG was its poor compatibility with one particular solder mask process. Not well controlled, it could induce electrochemical migration and poor wettability. Thus it affects PCB reliability even more than palladium chemistry differences between manufacturers.

The Phase 2 of the study focuses on the reliability of assembled ENEPIG boards and after assembly plus environmental tests.

The set-up is to:

- test two different ENEPIG chemistries provided by 2 finishes manufacturers
- compare ENEPIG versus reflowed SnPb solutions,
- evaluate ENEPIG finishes for different kind of packages (small SMDs and CCGA for ex.),

- estimate the impact of assembly processes on the reliability of the ENEPIG solution (vapour phase soldering from two different OEMs)
- submit test vehicles to different kinds of environments representative of storage or fatigue behaviours and perform analyses (mainly at Swerea IVF for comparison needs).

5. TEST BOARDS DEFINITION

Standard test vehicles representative of flight boards were designed by both OEMs to test the assembly of various SMD packages on ENEPIG PCBs. Boards mainly include footprints for: small/large chip resistors and capacitors, LCC3 and LCC6, SMD0.5, JLCC84, FP14, diodes, CQFP256 and connectors SUB-D.
Other PCBs (one in HDI technology and one with a sequential multi-layers stack-up) were dedicated to 6-Sigma CCGA 625 packages assembly on ENEPIG. This package type is characterized by a high standoff distance between the component and the board. Moreover, redundant connections are created by the copper ribbon within the solder column in order to reduce the risk for electrical opens.

6. PCB INCOMING INSPECTION

Incoming inspection was performed on all PCBs to evaluate the quality of the ENEPIG surface finishes. The objective of this inspection was to detect evident defects which could induce premature mortality and to be used as reference for analyses performed after the ageing tests. The coverage shall be complete and the finish shall be uniform on plated surfaces.
Very similar observations were made for the external layers of the various PCBs before assembly.

- Patterns looked clean before ageing and were compliant with IPC-4556.
- ENEPIG finishes had a rough golden appearance.
- The coverage was complete. Pads were more flat than with fused SnPb and the finish was uniform on the plated surfaces. No shortcuts were noticed.
- No differences between the finish suppliers were observed in the incoming inspection.

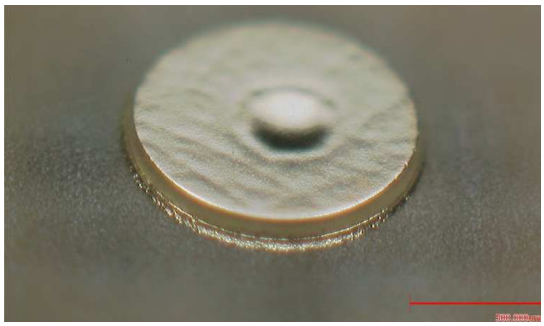

Figure 1. Dimple on a via observed on ENEPIG board

The only defects observed were minor and local. The roughness of the finish and the dimples (Fig. 1) are reflections of the original copper surface, i.e. to the PCB manufacturing processes rather than to the finish itself. With fused SnPb, such defects are masked.

7. ENEPIG PROCESS CONTROL

The usual method to control electroless nickel plating is to keep the bath parameters constant and assume constant reaction rates. An effective control of electroless bath (agitation, pH, Ni/Pd concentrations, etc.) is then the key to achieve a reliable process.
As metal in the electroless nickel bath is consumed, it has to be replaced. When the total additions of replaced metal are equal to the total amount of metal originally in the bath, that is one metal turn over (MTO). The reason the term is important is that in addition to consuming metal, the process generates spent reducing agent (by-products) and other contaminants that eventually affect the bath so badly that you cannot continue to use it and must dump it. An important property of an electroless process is how many turnovers you can do before replacement is necessary. An MTO of 4 is recommended to assure the quality level of Ni and Pd layers. Nevertheless, some impact on the reliability can be seen already at an MTO of 3.5. According to Kwon et al., the thickness of the IMC layer increases from 1.07 to 1.30 µm with a changed MTO from 0 to 3.5 [6]. This was followed by an increased risk for brittle fractures in a drop test. The increased risk for brittle fractures was believed to be due to a thicker Ni-Sn-P layer with a higher level of nanovoids.

8. ENEPIG THICKNESS MEASUREMENTS

The thicknesses of the Au and Pd layers can impact the growth of the layer with intermetallic compounds (IMC) and consequently the reliability of assemblies. Two techniques were used here to measure the thicknesses of different layers: X-ray fluorescence (XRF) and scanning electron microscopy (SEM).
The main advantages of XRF are its non-destructive properties and that measurements can be performed without preparation of special samples. The rapidity of the measurement explains why ENEPIG PCBs are always delivered with XRF reports. However, the results are dependent on the programs and on the calibration parameters. This is especially true when the layers are very thin, as for ENEPIG. Until proof of the opposite, it is difficult to be fully confident with XRF data from suppliers of finishes.
In order to determine the true thicknesses of the Pd and Au layers, microsections were analysed using Field Emission SEM. The samples were prepared using broad band ion milling (Gatan Ilion+ Model 693) also called ionic polishing. Hence it was possible to visualize inter-layers, to measure thickness of Ni/Pd/Au layers and to compare values coming from various manufacturers of finishes.

Table 1 gives, for Manufacturer A, results from XRF and SEM measurements. It shows the poor repeatability of the thicknesses of the Pd and Au layers for both suppliers but also that XRF measurements may deviate 25% from the true value.

	SN1	SN2	SN3
Pd (µm) - SEM	0.122	0.055	0.120
Pd (µm) - XRF	0.132	0.044	0.089
Au (µm) - SEM	0.038	0.051	0.054
Au (µm) - XRF	0.039	0.049	0.048

Table 1. Pd and Au thicknesses for various PCBs from Manufacturer A / Chemistry A

On some samples manufactured with Chemistry B, "corrosion spikes" were observed in the Ni layer with an appearance typical for corrosion spikes associated with the black pad defect in ENIG finishes (Fig. 2). This indicates that ENEPIG may not be completely immune against the black pad defect. However, the number of corrosion spikes was small and it is not likely that they would affect the reliability of the solder joints.

Observations with a larger magnification show:

- A very thin dark band with inclusions of micro-voids detected at the Ni/Pd interface on PCB from supplier and chemistry B (standard and CCGA types). This dark band is only observed with a very large magnification (up to x 200 000). It has an appearance similar to the dark band formed between Au and Ni in ENIG finishes consisting of Ni_3P.
- A rather smooth interface between Pd and Ni, without any voids, is seen on PCB from supplier and chemistry A. Differences could be linked to the chemistries or to the process parameters (time and temperature).

Finishes defects on bare boards were rather few and were considered not likely to affect the reliability of solder joints. The boards were then all accepted for the assembly phase.

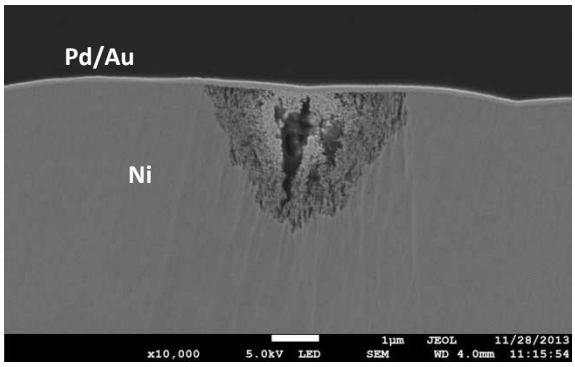

Figure 2. Corrosion spike in Ni at 10 000 times magnification – PCB SN5

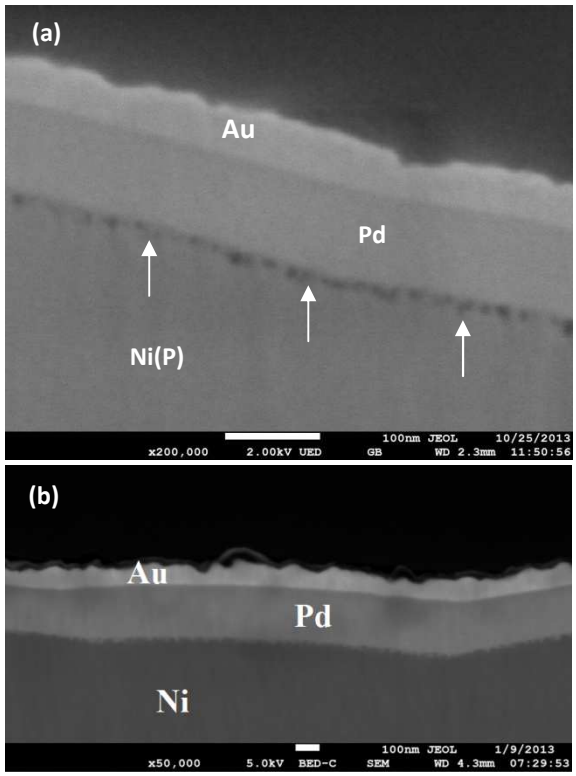

Figure 3. ENEPIG finish after ionic polishing – SEM observation. a) Dark band with micro-voids inclusions – Chemistry B and b) Smoother interface – Chemistry A.

9. BOARDS ASSEMBLY

The quality of PCB finishes impacts the planarity of the Cu pads (dimples observed before assembly, no bump as for SnPb) as well as the brightness of boards (yellow rather than grey) or the isolation between tracks. It could thus affect assembly process steps such as screen paste printing, component placement or final inspection. Prior to the assembly, the boards were submitted to one reflow soldering process in order to simulate the flight hardware standard manufacturing flow. The components were then mounted according to OEM PID using different assembly processes: vapour phase soldering, hot air process for CCGA 625 repair plus for some of the SMD0.5, and manual soldering for CQFP plus connectors. A soldered standard board is shown in Fig. 4.

Moreover, manual repairs were carried out on several components (mainly JLCC 84 mounted with vapour phase soldering) and thermal shocks have been applied on the pads at 270°C and 350°C.

No problem linked with ENEPIG finish was reported here during the assembly of test vehicles.

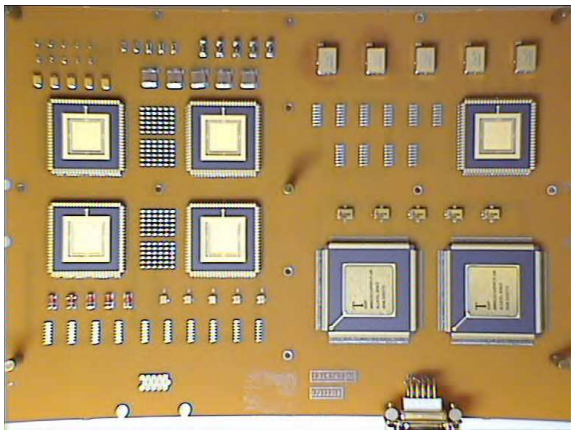

Figure 4. ENEPIG standard board

10. VISUAL INSPECTIONS AFTER ASSEMBLY OF BOARDS

After the assembly process, the components have been inspected with a binocular or a digital microscope Hirox KH-1300 in order to check the solder joints quality and to compare ENEPIG with fused SnPb. The main observations from visual inspections are the followings:

- No shortcut was noticed on standard boards during the inspection.
- The wettability of SnPb solders is easier to observe with ENEPIG finish thanks to the colour contrast between the alloy and the gold.
- No great differences have been noticed in the appearance between ENEPIG and fused SnPb finishes, neither for different packages. The only point to underline is a short reduction of stand-off. With ENEPIG, the stand-off is only due to solder paste deposition whereas with SnPb the solder on the fused lands contributes to the stand-off.
- No soldering defect (de-wetting, cold solder joint or solder balls) and no differences with fused SnPb were neither observed on CCGA boards.

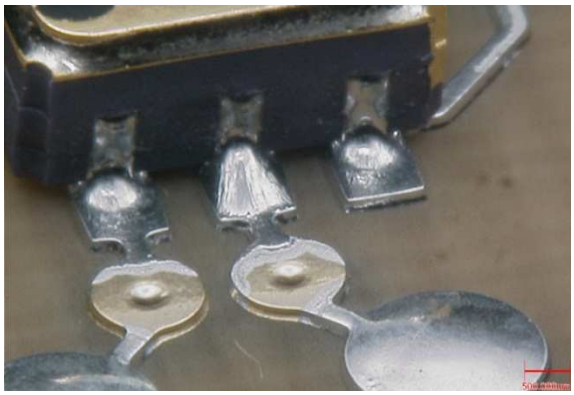

Figure 5. LCC6 after vapour phase soldering assembly

Electrical continuity tests at ambient temperature and X-rays inspections confirmed the quality of ENEPIG assemblies before the environmental tests.

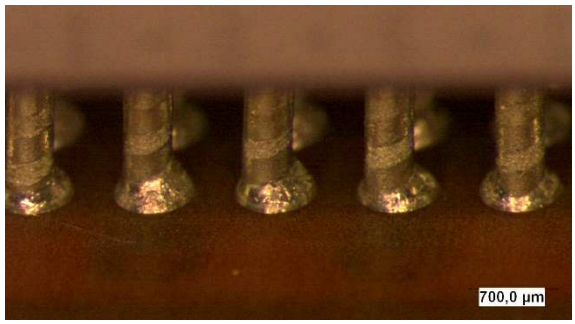

Figure 6. CCGA 625 Six-Sigma after automatic assembly on ENEPIG PCB.

11. MICROSECTIONS AFTER ASSEMBLY

Microsections were performed on as-soldered ENEPIG boards from supplier A. The objective was to identify IMCs formed after assembly and before environmental testing. The compositions of the various IMC phases have been estimated based on element mapping and on what has been reported in the literature.

The SEM/EDS investigation of a 2220 capacitor is shown in Fig. 7. The IMC layer had almost completely spalled off, as have been reported by others when using SnPb solder.

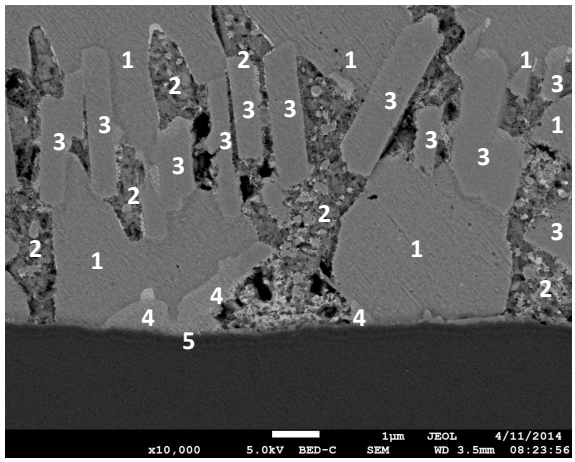

Figure 7. 2220 capacitor on ENEPIG from manufacturer A. 1) Sn, 2) Pb, 3) (Pd,Ni)Sn_4, 4) $AuSn_4$ and 5) Ni_3P

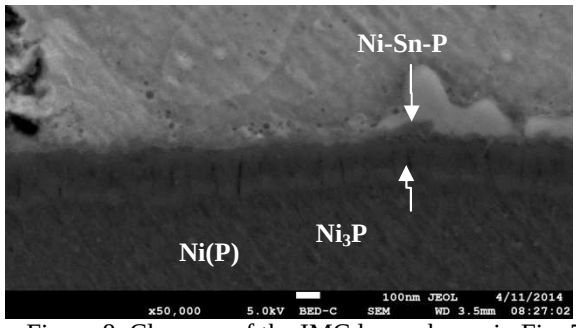

Figure 8. Close-up of the IMC layer shown in Fig. 7.

A layer of Ni_3P with a thickness of about 200 nm can be observed at the uppermost part of the Ni(P) layer (Fig.

8). On top of the Ni_3P layer, there is a thin layer (<50 nm) that consists of Ni, Sn and P, which probably is the nanocrystalline Ni-Sn-P layer reported by others. Besides some $AuSn_4$ at some locations, there is no other IMC layer on top of the Ni-Sn-P layer. Most of the other components on the reference board had a similar appearance of a spalled-off IMC layer.

When soldering to a Pd layer that is too thick to be completely dissolved, the IMC layer formed is reported to consist of $PdSn_4$ [7]. The IMC layer has a lamellar structure with the $PdSn_4$ lamellae grown perpendicular to the palladium surface. Therefore, what probably happens during the soldering to ENEPIG is that a lamellar $PdSn_4$ IMC layer is first formed. When the Pd layer has been completely consumed, the $PdSn_4$ layer with IMC crystals grown perpendicular to the surface is spalled off. That is in agreement with the spalled-off crystals in Figure 7.

The development of the IMC layers (composition, thickness and shape) and their impact on lifetime of solder joints are studied in phase 2 of this study, in which boards were subjected to the following accelerated environmental tests.

- Vibrations according to ECSS-Q-ST-70-38 standard levels on all boards,
- Higher levels of vibrations plus shocks for part of the CCGA625 assemblies,
- Thermal cycles (-55/+100°C, 15 min dwells, 10°C/min ramp) up to 500 cycles for standard boards and to 1500 cycles for CCGA boards,
- High temperature storage simulation (125°C for 500 h) to be equivalent to 1 year at ambient conditions.

Only the CCGA625 assemblies exposed to high levels of vibrations, shocks plus 500 thermal cycles have so far been micro-sectioned.

12. CCGA 625 ASSEMBLIES

For both ENEPIG PCB types (A and B), continuous electrical monitoring was carried out during thermal cycles up to 1500 cycles. Microsections were also performed at 500 cycles on one package of each assembly process (vapour phase and repair).

The assembly of the CCGA625 packages on board was successful equally for the two OEM. All the parts passed the cumulative qualification test flow up to 1500 cycles without any electrical failure. After vibrations (shocks) and 500 thermal cycles, diagonal microsections of packages confirmed the nominal and equivalent ageing of the solder joints (Fig. 9). They do not show critical defects likely to question the assembly of the columns on the package or on the board. No damage was either found at PCB level.

Further SEM/EDS analyses with higher magnification factors complement analyses on as-soldered assemblies on ENEPIG IMC. Fig. 10 shows the result after vibrations (shocks) and 500 thermal cycles for vapour phase soldered CCGA 525 components soldered at the two PCB manufacturers (A and B).

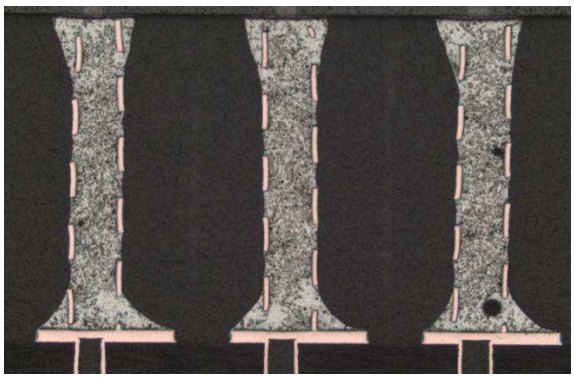

Figure 9. View after 500 cycles of a CCGA 625 Six-Sigma repaired on ENEPIG board from manufacturer A.

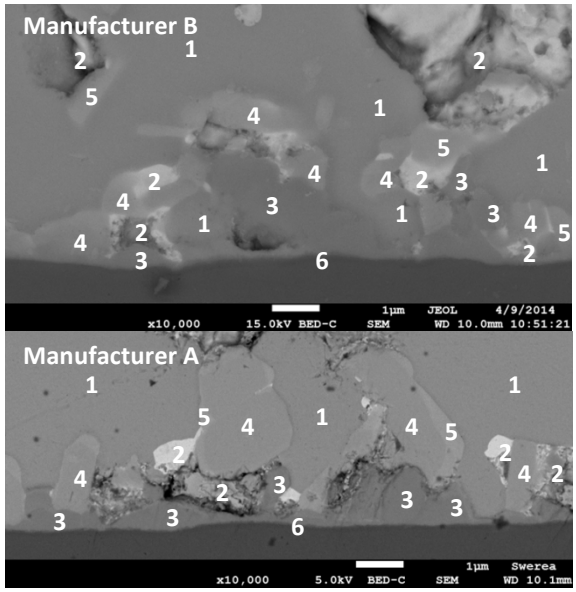

Figure 10: SEM/EDS analysis after 500 TC on CCGA 625 boards from manufacturers A and B. 1) Sn, 2) Pb, 3) $(Cu,Ni)_6Sn_5$, 4) $PdSn_4$, 5) $AuSn_4$ and 6) Ni_3P.

The results are very similar for the two components. The IMC layers consist of a complex mix of at least three IMC phases; $(Cu,Ni)_6Sn_5$, $PdSn_4$ and $AuSn_4$. Beneath these IMC layers with mixed IMC phases, there are also the Ni-Sn-P and Ni_3P layers. What may surprise is the $(Cu,Ni)_6Sn_5$ phase, which mainly can be found on top of the Ni-Sn-P layer. Since neither the solder nor the solder land contain Cu, it must come from the copper ribbons in the solder columns. Clearly, the Cu from the copper ribbons has prevented the spalling of the IMC layer that occurred for the other types of components. The $AuSn_4$ phase contained also some Pd and the $PdSn_4$ phase contained probably some Au.

The IMC layer for a repaired CCGA 625 that had been exposed to vibrations, shocks and 500 thermal cycles

had a quite different appearance (Fig. 11). Palladium and gold were almost completely missing in the IMC layer. The reason is that after demounting of the component, pads are first stripped of tin using a copper solder wick braid and then retinned with SnPb wires. This will effectively remove all Pd and Au. Another difference is that there are considerably more copper in the IMC layer on the repaired sample. Further analyses are in progress to determine if it originates from the copper ribbon within the solder column or from the copper solder wick braid used in the pads retinning process.

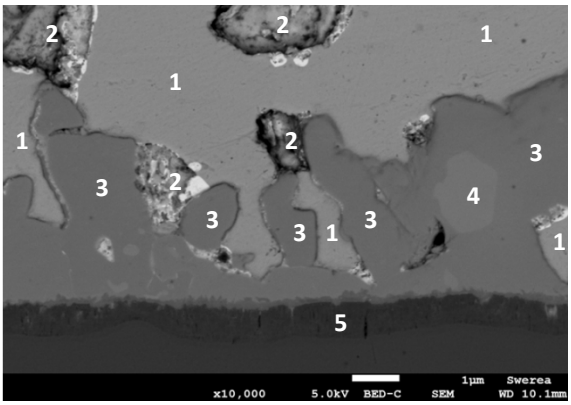

Figure 11. SEM/EDS analysis after 500 thermal cycles of repaired CCGA 625 board. 1) Sn, 2) Pb, 3) $(Cu,Ni)_6Sn_5$, 4) $(Ni,Cu)_3Sn_4$ and 6) Ni_3P.

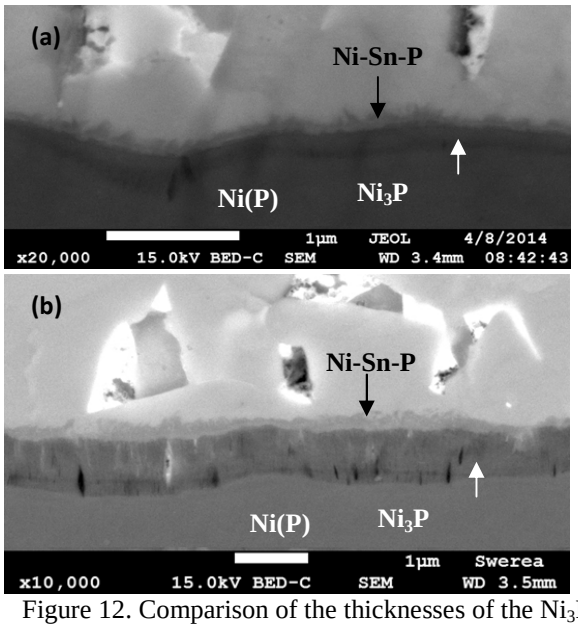

Figure 12. Comparison of the thicknesses of the Ni_3P and Ni-Sn-P layers on a) a non-repaired and b) a repaired CCGA 625 soldered by Manufacturer A.

Another difference between vapour phase soldered and repaired CCGA 625 components is that the Ni_3P and Ni-Sn-P layers are considerably thicker for the repaired CCGA 625 component (Fig. 13). Whereas the Ni_3P layer has a thickness of 100-200 nm for the non-repaired component, it is almost 1 µm thick for the repaired component. Furthermore, there are a lot of crevices between the columns in the Ni_3P layer for the repaired component, of which some are filled with Sn, but almost no crevices are observed in the Ni_3P layer for the non-repaired component. The Sn-Ni-P layer is also about twice as thick for the repaired component compared to the non-repaired component.

13. SNPB REFERENCE SAMPLE

The SEM investigation of the SnPb CCGA reference is finally given in Fig. 13 for vapour phase assembly process after 500 thermal cycles. As expected, the IMC layer consists of Cu_6Sn_5 and some Cu_3Sn closest to the copper.

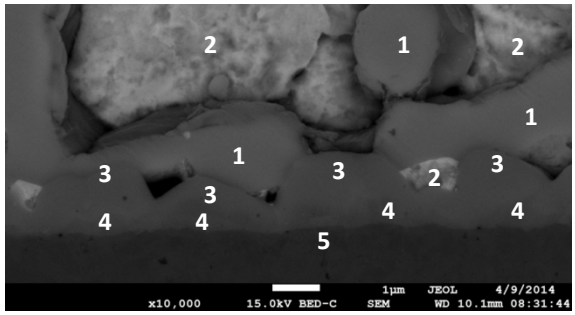

Figure 13: Comparison with CCGA 625 packages mounted on reflowed SnPb PCB after 500 TC. 1) Sn, 2) Pb, 3) Cu_6Sn_5, 4) Cu_3Sn and 5) Cu.

Detailed IMC analyses for Six Sigma CCGA 625 packages mounted on boards are thus coherent with assembly processes (ENEPIG versus reflowed tin-lead, repair versus vapour phase soldering). Moreover, they have demonstrated the same kind of interfaces for both manufacturers. No significant changes were seen after vibrations/shocks plus 500 thermal chocks and there is no risk of gold embrittlement of the solder joint. These positive points reinforce compliant electrical monitoring results up to 1500 thermal cycles.

14. CONCLUSIONS

When selecting a lead-free alternative surface finish for a PCB, the key parameters are: solderability, shelf life, high temperature stability, solder joint reliability and cost. ENIG finish is widely used in electronic industry. However, the main drawback of this finish is its inclination to form the black pad defect.

ENEPIG is a good alternative to fused SnPb with a very cosmetic appearance. The roughness of the finish and the dimples, masked with fused SnPb pads, are linked to Cu surface: to the PCB manufacturing process rather than to the finish itself. SEM/EDS observations have demonstrated inter-layers main characteristics and a low repeatability of layers thicknesses in different manufacturing lots. However, finishes defects on bare

boards were rather few and were considered not likely to affect the reliability of the solder joints. Nevertheless, one board showed a few "corrosion spikes" in the Ni layer indicating that ENEPIG may not be completely immune to the black pad defect.

In order to complete this first evaluation on lead-free alternative surface finishes for PCB assembly, the next step was then to evaluate ENEPIG boards after assembly with various package types (Six Sigma CCGA 625, QFP, resistors and connectors) and environmental tests dedicated to assemblies. No problem related to the ENEPIG finish was reported during the assembly of test vehicles with vapour phase, manual or repair process.

Optical and X-ray observations just after assembly were also fully compliant with ECSS-Q-ST-70-38C. They were complemented by SEM/EDS analyses of the IMC layers to evaluate the impact of ENEPIG finishes manufacturers as well as on assembly processes. After vapour phase soldering and for most of the component types, the IMC layer had almost completely spalled off, which have also been reported in the literature when using SnPb solder.

No $AuSn_4$ crystals were found in the bulk solder. Thus, the very low Au content in the bulk solder caused by the ENEPIG finish should not cause "gold embrittlement" of the solder joint.

Results after accelerated environmental tests are given here for 6-Sigma CCGA 625 packages. The assembly of the CCGA625 packages was successful equally for the two OEMs. All the parts passed the cumulative qualification test flow: vibrations, shocks and thermal cycles up to 1500 cycles without any electrical failures. After vibrations (shocks) plus 500 thermal cycles, diagonal microsections of CCGA packages confirmed the nominal and equivalent ageing of the solder joints. No critical defects likely to question the assembly of the columns on the package or on the board were observed. Neither were any damages found at PCB level.

Detailed IMC analyses for Six Sigma CCGA 625 packages mounted on boards and exposed to the environmental tests showed the same kind of interfaces for both manufacturers. The IMC layers had not spalled off as for the other component types. Instead, the IMC layers contained Cu and had a composition and appearance that is typically achieved when soldering using Cu containing solders. Thus, Cu dissolved from the Cu ribbon in the solder columns seems to have a very beneficial impact on the IMC layers formed preventing them from being spalled off.

Repair of CCGA components increases the thickness of the Ni_3P and Ni-Sn-P layers considerably and also the amount of crevices in the Ni_3P layer. It does not seem to have affected the reliability of the CCGA components but it might do that for components if the IMC layer is spalled off.

No significant changes were seen after vibrations plus 500 thermal cycles. These positive points then reinforce compliant electrical monitoring results up to 1500 TC.
The impact of the spalling of the IMC layers on the reliability during the environmental tests for the other component types than CCGA has not yet been evaluated but this evaluation is ongoing.

All the results given in this paper are going towards the qualification and the use of ENEPIG finishes for SnPb assembly process. One last point is nevertheless still to be confirmed. What will be the impact of long storage and multiple thermal heating of boards (caused by successive PCB baking and cleanings)? The consortium proposes here to enlarge this study to this last evaluation step. It would consist in re-manufacturing one PCB per ENEPIG types. Storage plus thermal heating should then be simulated before complementary SEM analyses and components assembly.

15. ACKNOWLEDGEMENTS

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