WAFER LEVEL PACKAGING –PROCESSES AND MANUFACTURING EQUIPMENT

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ABSTRACT

Increasing requirements in performance and functionality of electronics and the satellite payload while maintaining weight, volume and cost efficiency demand higher integration levels and die densities of the semiconductor devices as well as increased application of photonic devices. The paper presents selected manufacturing processes and equipment which have been developed for the production of such devices and are currently in the industrial implementation phase. Application areas range from mobile devices, LEDs to bio-sensing. These processes and equipment have the capacity to contribute to a number of space related issues like lightweight design and power consumption. These constraints are addressed by the thin wafer handling process and a specific chip to wafer stacking method. Nanoimprinting and embossing technologies address the development and production of optical components and structures for optoelectronic devices. Finally EVG equipment for R&D as well as small and medium size production is briefly outlined.

1. INTRODUCTION

Microelectronic applications tend towards more complex components with higher integration at the chip level, higher frequencies, more functionality and increased performance. 3D integration is a promising technology for advancing the performance of semiconductors since it can provide higher density, faster speed and better power efficiency in more lightweight and smaller devices. An increasing demand in data traffic and processing on board of satellites requires the implementation of such technologies, which are currently applied mostly in consumer devices. The throughput of next generation digital telecom satellites is expected to exceed terabits per second of data which have to be processed on board. To meet this goal an increased application of photonics interconnects and optoelectronic devices can be expected.

However, the space environment sets very challenging requirements on the robustness and reliability of all components due to mechanical vibrations and shocks during the launch sequence and due to continuous temperature cycling and ionizing radiation during the long lifetime of the satellite.

EVG has developed dedicated manufacturing equipment for a number of processes for wafer level packaging, 3D integration and wafer level optics. This paper shall give an outline on EVG technologies, products and process services for the manufacturing, integration and assembly of electronic and photonic devices, which can have a positive impact on space specific issues and challenges.

2. THIN WAFER HANDLING

Thin wafer handling is a widely acknowledged technology for the processing of thinner dies and for Through Silicon Via (TSV) formation. TSVs usually result in higher bandwidth and speed, reduced power consumption and a better signal-to-noise ratio. Furthermore thin dies enable higher device performance for instance through more efficient cooling, which enables higher speed or higher currents and voltages. However, for consumer products, economical constraints require efficient material consumption and high speed manufacturing [1]. In order to minimize the via formation cost the via aspect ratio has to be kept within a certain range (pTSV:20µmX80um and iTSV:5µm X 20-50µm, for high density TSV devices: <20µm wafer thickness). A thinner wafer allows lower aspect ratio TSVs resulting in higher throughput. For a given aspect ratio thin wafer processing enables smaller pitch and higher density.

Processing of front- and backside of a thin wafer can be implemented by temporarily bonding the wafer to a carrier wafer. After back-thinning the backside of the device wafer, it can be processed using standard wafer fab equipment. The carrier wafer gives mechanical support and stability and protects the fragile wafer edge of the thin wafer. After processing the thin wafer is debonded from the carrier wafer and can be singulated for later chip-to-wafer stacking or bonded to another device wafer.

Adding two process steps, temporary bonding and debonding, enables to run thin wafers in existing fabs with existing equipment.

2.1. Temporary bonding

Figure 1 shows the generic process flow for thin wafer processing with temporary bonding to a carrier wafer. The product wafer which has gone through front end processing will be mounted onto a carrier wafer. The carrier wafer is coated with a temporary adhesive, which is usually deposited by spin coating processes. In

figure 1, the materials involved in the temporary bond consisting of the temporary adhesive and any optional layers that will facilitate later release of the carrier. Basically there are two options for the adhesive layers: Thermoplastic or crosslinking adhesives. Thermoplastic adhesives offer the advantage of having the option to perform solvent cleaning after debonding to remove adhesive residues. Crosslinking adhesives do not offer such wet chemical cleaning capability and will have to be mechanically peeled either during the debonding operation or after debonding in order to remove the adhesive from the product wafer.

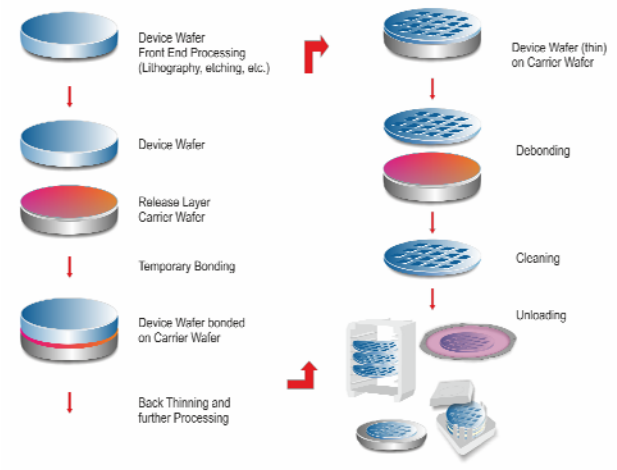


Figure 1: Process Flow

Both thermoplastic and thermoset adhesives have been evaluated during the past years. Depending on the debond method which is optimal for the device wafer, the adhesive has to be chosen or particularly tailored. Today adhesives with thermal stability of beyond 380°C are available.

An important point is also the choice of the carrier wafer. For silicon-based devices the recommended carrier is a standard silicon wafer. From a geometrical point of view, this enables the use of standard wafer processing equipment without modifications, whereas oversized carriers would require special wafer chucks and cassettes for the wafer stack. Even more important are the thermal properties of the bonded stack. With a silicon carrier the thermal expansion between device wafer and carrier is perfectly matched. Using a non-silicon carrier however can cause bow and warp due to thermal expansion mismatch. On the other hand CTE-matched glass carriers can result in metal ion contamination and it is not always possible to use these glass carriers in CMOS fabs.

EVG temporary bonding and debonding platforms are able to implement customer materials and processes. A number of adhesives and carrier materials have been qualified and are available for small and high volume manufacturing (Fig.2)

Figure 2: EVG®520IS Semi-automated Bonder and EVG®850XT Temporary Bonding/Debonding System

2.2. Debonding

For the above described adhesives and carriers different debonding technologies are offered:

- Solvent release debonding and laser assisted debonding require the use of glass carriers
- Thermal slide off debonding requires elevated temperatures
- Room temperature debonding methods
    - LowTemp™ Laser Debond
    - LowTemp™ Mechanical Debond
    - LowTemp™ ZoneBOND® (Fig.3)

ZoneBOND® is the favorable method. It can be applied on Si or glass carrier and works with easy thermoplastic adhesives.

Temporary bonding and debonding for thin wafer handling has been successfully processed through the complete TSV process line for 300mm wafers with a thickness of 30µm.

The major advantages of the described process flow is its compatibility with existing processing lines, processes and even with modified process flows.

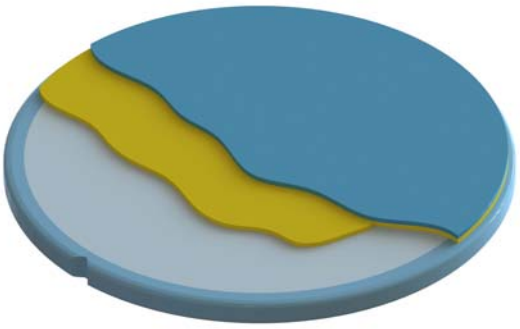


Figure 3: Basic principle of ZoneBOND® with selective treatment of edges zone and center

3. CHIP TO WAFER STACKING

The AC2W technology is a wafer level technology. This means that single components such as electronic die or odd-shaped components (either flipped in a face down orientation or face up) are mounted onto a complete, non-diced device wafer. The wafer-level approach lowers costs and allows for further wafer-level processing after chip bonding. Therefore modular sequences with two or more dies on each other are possible. The interconnect layer for bonding the die can be solder, polymers or other material depending on specific application needs. The basic idea behind AC2W technology is to split the complete process into two individual processes - an alignment and a pre-bonding process that defines the accuracy of the assembly and a permanent bonding process that forms the final interconnect. Permanent bonding is typically achieved by introducing temperature to the interconnect layer while maintaining force on the chip backside.

The decoupling of alignment and permanent bonding offers significant advantages in the production of AC2W assemblies. High throughput alignment can be performed at room temperature without the disturbing influence of process temperature and high force on placement accuracy.

In addition, existing and mature die bonding equipmentcan be used instead of highly customized, sophisticated tools necessary for in-situ processing. Permanent bonding is achieved in a second process step with a fully assembled bottom wafer. Through this batch fabrication, the time consuming interconnect formation is done for all devices on one wafer in parallel.

An advanced chip-to wafer-bonder (AC2W bonder) allows for careful control of processing parameters in terms of temperature, force and ambient gas. The AC2W bonder is provided in a vacuum chamber allowing for evacuation and controlled ambient gas. A uniform force can be applied across the whole wafer and thus to every chip even though the chips have different total heights.

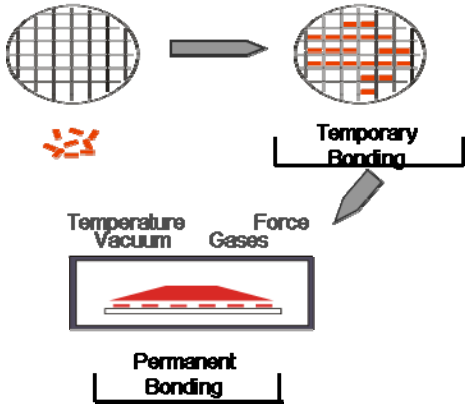


Figure 4: Principle AC2W process flow [3]

The key to separating the alignment and bonding steps is an effective tacking method to temporarily fix the die and allow safe transfer from the die bonder to the AC2W bonder without the need for dedicated clamping fixtures. Depending on the material composition of the opposite contact surfaces and the final application of the assembly a number of different tacking methods could be used. These methods include bonding with temporary adhesives and thermocompression bonding. Temporary adhesives can be used to fix the die in their preferred position in the flip chip bonder and prevent shifting of the top chips until the permanent bond is formed in the second process step. The temporary adhesive should either completely vaporize or be pushed away during the formation of the permanent bond.

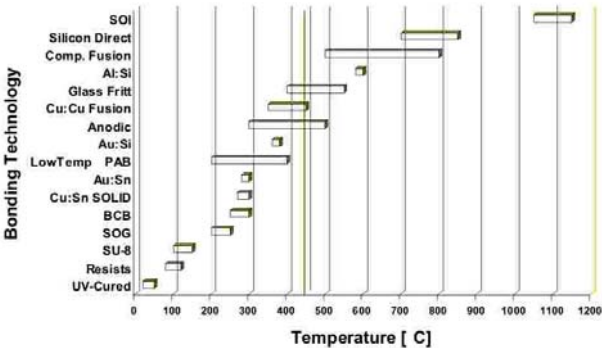


Figure 5: Overview of bonding temperatures for various interconnect materials.

The separation of the alignment and permanent bonding, along with the capabilities of the new AC2W bonder provide a high degree of flexibility to choose different interconnect methods for mechanical as well as electrical interconnection of 3D integrated components in different applications.

The key considerations for choosing the right

interconnect method are driven by various factors. These include the nature of the device (such as MEMS), requirements driven by the functional principle of the device (e.g. a hermetic seal) and requirements that are determined by the nature of the parts to be integrated (e.g. the integration of different CTE materials).

- Electrical Interconnect: Bonding is used to interconnect electrical components. Copper-to-Copper bonding, soldering (e.g. using a CuSn layer) and bonding using conductive adhesives are the main candidates for lead free electrical interconnect materials.
- Dielectrical Layer: For bonding applications that require electrical insulation in between the two parts, usually an intermediate layer is applied. A high performance low-k dielectric layer like BCB (Benzocyclobutene) can be either spin- or spray coated onto the substrate, and the bonding process is performed by applying a uniform force and temperature inside a vacuum chamber. Other possible materials include photo resists
- Bonding Temperature range: Fig. 5 shows an overview of the required bonding temperatures for different interconnect methods. The AC2W technology covers the range up to the yellow line.
- CMOS compatibility: The presence of Pb (glass fritt bonding), Na (Anodic bonding) or Au (thermal compression bonding) is a concern for CMOS wafers.
- Operational Condition of the device must be taken into account to maintain the expected functionality and life time.
- Optical Transparency: Optical sensors or optical devices require a transparent interface to the environment which has to withstand the bonding process.

Figure 6: EVG®540 AC2W Bonder

AC2W technology enables interconnect processes on the component level, ranging from adhesive bonding and soldering to interconnect methods previously restricted to wafer-to-wafer bonding approaches such as anodic bonding, fusion bonding or glass frit. Thus AC2W allows 3D vertical integration of IC's and hybrid integration of MEMS and IC's based on a broad range of different interconnect methods.
Permanent bonding is performed with EVG®540 AC2W Bonder applying controlled temperature, force and environmental conditions to the interconnect layer.

4. WAFER LEVEL OPTICS

The expanding throughput of telecom satellites due to more broadband communications strongly motivates the investigation and development of optoelectronics for space application. In the future photonic components could provide a generic high-speed medium supporting inter-chip, inter-board and inter-equipment communications in on-board processors. High data rates and mass savings are the major impact of an increasing use of photonic devices.
Two methods for the wafer level production of micro- and nano-scaled optical structures like lenses and diffraction gratings are implemented in EVG manufacturing tools.

4.1. Nanoimprint Lithography (NIL)

Applications of this technology are -amongst others - laser devices and photonic ICs for communication technology, photonics management for LED lighting, optical and image sensors, concentrated photovoltaic.

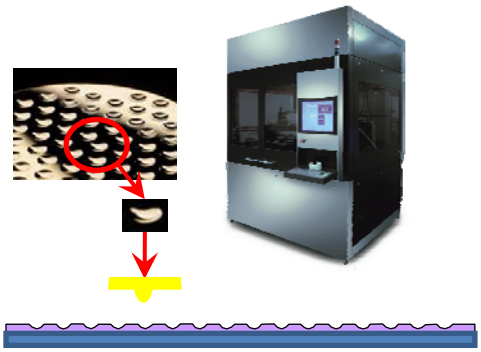
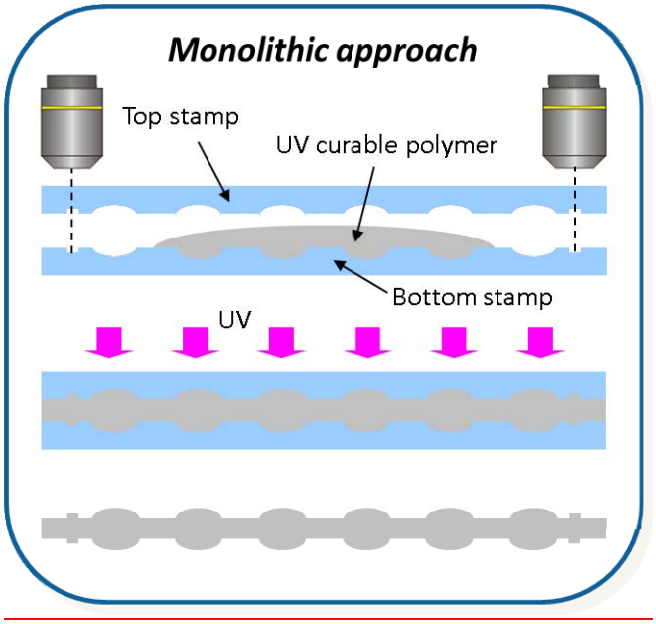


Figure 7: Schematics of single lens replication from master stamp with EVG®770 Gen II NIL Stepper

As a first step an imprint stamp has to manufactured. The procedure of replication lenses from a master stamp via a step and repeat process is shown in Fig.7. The EVG770 step and repeat system supports hard and soft UV-NIL for wafers up to 300mm. This technology is mostly useful for master stamp fabrication. The master can be used for imprinting wafers like shown in Fig.8.



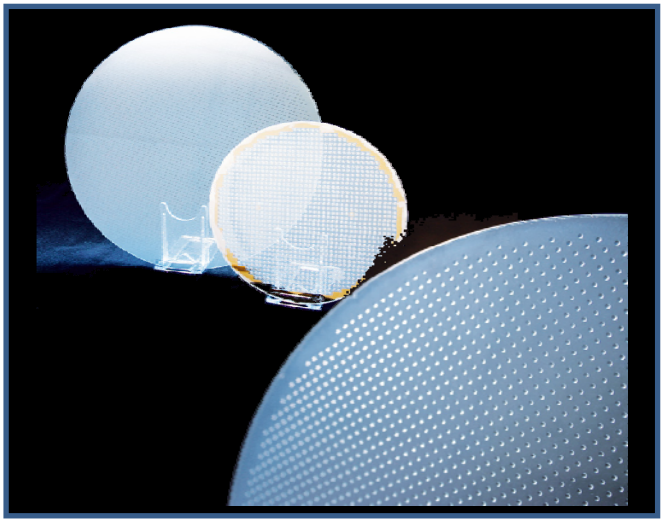


Figure 8: Monolithic Lens Moulding and Lens Wafers

4.2. Hot Embossing

Hot embossing enables the creation of two-dimensional and three-dimensional structures by applying elevated temperatures and high contact forces. Stamp and substrate are brought in contact inside an EVG500 Series vacuum chamber. A precisely controlled temperature profile (typically up to 250°C, the system supports up to 650°C) and contact force sequence (up to 360 kN) create an imprint of the stamp on the substrate. Imprint areas up to 200 mm in diameter with high resolution features down to 50 nm have been demonstrated on the EVG500 hot embossing systems. Typical stamps are made out of Si, SiO2 or metals (e.g. Ni). Substrates are typically polymer substrates or coated polymers on semiconductor wafers. The high temperature option enables imprinting into materials where elevated temperatures are needed. This is particularly important, as only high performance polymers are feasible in space applications and in many cases optical material for extreme conditions (UV, radiation) like glasses will be needed.

The hot embossing technique is mostly used for thermoplastic polymer sheets and spin-on polymers on substrates, as these materials can be processed at lower temperatures. With the EVG750 a fully automated hot embossing equipment is available. The process flow is shown below.

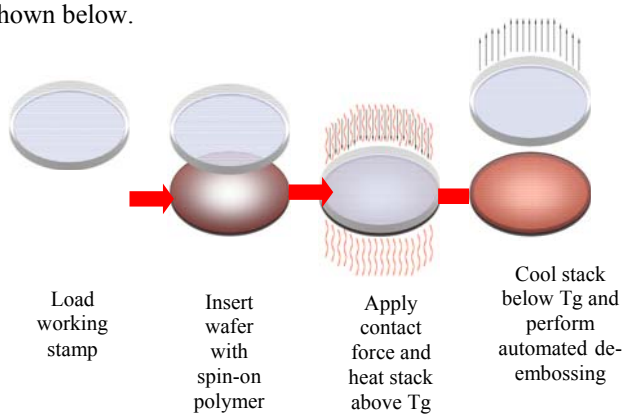


Figure 9: Hot embossing using soft working stamp

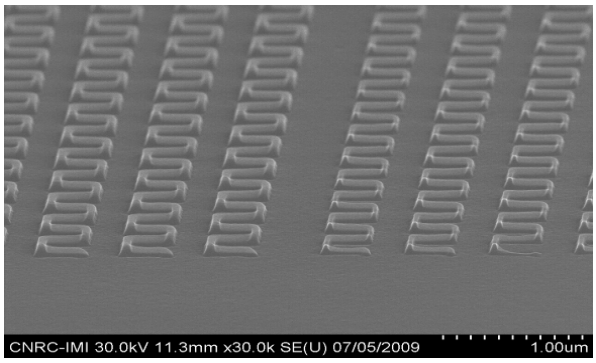


Figure 10: 50nm/100nm structures with a height of 100nm

Firstly soft stamps are fabricated out of the expensive master stamps and secondly multiple wafers with polymer layer are imprinted with these soft stamps [5]. The major advantages of using soft stamps are reduced cost and easier detaching of the stamps. The embossing temperatures however are limited by the T_g of the soft stamps, which limits the material classes to be processed to low T_g polymers. Features ranging from 30 to 300 µm with feature heights of up to 200 µm could be demonstrated with high pattern fidelity as well as imprinted spin-on layers with high resolution features down to 50 nm [Fig. 10].

5. CONCLUSIONS

Though targeting mainly high volume markets in micro- and nanofabrication certain EVG processes and manufacturing equipment has strong potential for serving special needs of future space electronics and photonic components. In particular the R&D equipment, the process services for small volume manufacturing and R&D cooperation with potential customers can contribute to the implementation of successful terrestrial technologies in satellite applications.

6. REFERENCES

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