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Xilinx Space Grade Packaging Development Updates

for 2014 EMPPS

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May 21, 2014

Virtex-4 and Virtex-5 QV FPGA Package Re-Qualification

- **Xilinx CF Package supplier IBM, is shutting down its Ceramic Flip Chip assembly line including column attach of the Ceramic Column Grid Array (CCGA) in late 2014**
- **Affected package devices are:**
  - Virtex-5 QV (XQR5Vxxxx) and Virtex-4 QV (XQR4Vxxxx)
  - CF Daisy Chains (XQDaisy-CFxxxx and XCDaisy-CFxxxx)
- **Xilinx issued PCN in February, 2013 to discontinue all IBM CF packages, and will rollout new packages**
- **Xilinx is in the process of qualifying Kyocera at San Diego, CA. as new Packaging supplier**
  - New packages assembled at Kyocera are designated as CN Packages
  - Kyocera is QML Class V certified for Flip Chip assembly
  - CN package qualification on track to complete before the end of 2014

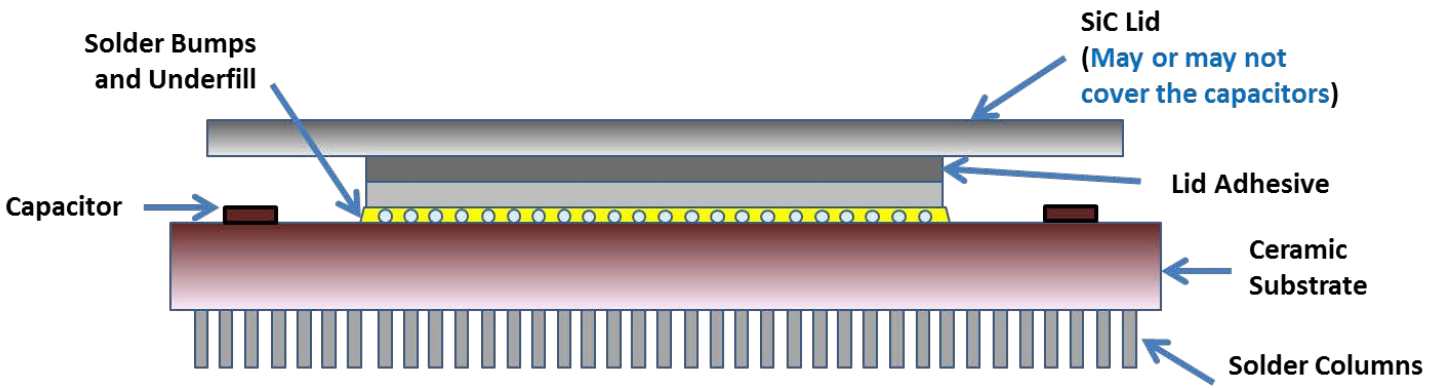
CN Package Qualification Update

- **Status on Assembly qualification for Kyocera San Diego**
  - Multiple engineering builds for process optimizations and pre-qual reliability tests complete
  - Pre-Qual XQDaisy-CN1752 parts build completed in early April (LGA)
  - Official qualification lot builds in progress
    - First qualification lot at class V/Y level screening test now
- **New Changes for CN Packages**
  - CN Package was initially to be Land Grid Array (LGA) packages
  - Based on customer-feedbacks, Xilinx has decided to add solder columns to CN packages
  - Solder columns attachment will be done by 6-Sigma in Milpitas, CA
    - Most customers have ample experience with 6-Sigma columns already
  - Process optimization development in progress

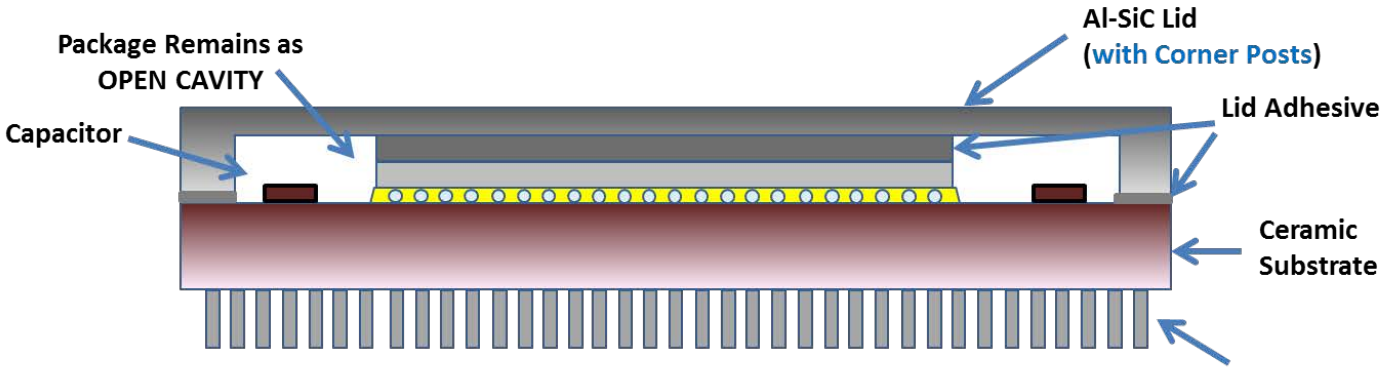
Comparison between IBM (CF) and Kyocera (CN) Packages

Original IBM CF Package	New Kyocera CN Package
Silicon and Substrate Remain the Same	
All design tools and timing files remain the same	
Package pin assignment and PCB layout are preserved	
BME capacitors used remain the same parts (Tin-Lead Terminals)	
Assembly Related Changes	
Assembled at IBM at Bromont Canada	Assembled at Kyocera at San Diego
Ceramic Column Grid Array (CGA-90/10)	Ceramic Column Grid Array (CGA-80/20)
High Lead Flip Chip Solder Bum High Lead Solder for Capacitor Attach	Eutectic Flip Chip Solder Bump Eutectic Solder for Capacitor Attach
SiC Lid (Electrically Non-Conductive)	Al-SiC Lid (Electrically Conductive)
TIM and Underfill Material (IBM Specific)	TIM and Underfill Material (Kyocera)

CF (IBM) vs CN (Kyocera) Packages



CF Package (IBM)
(Drawing Not to Scale)

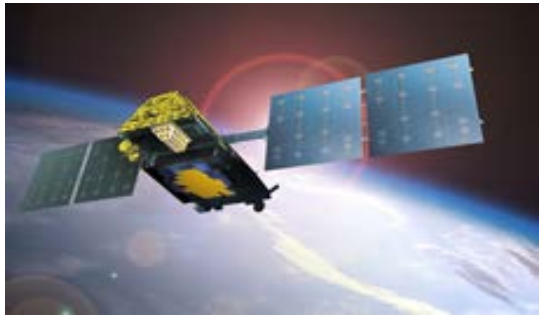


CN Package (Kyocera)
(Drawing Not to Scale)

CN Package Qualification Plan

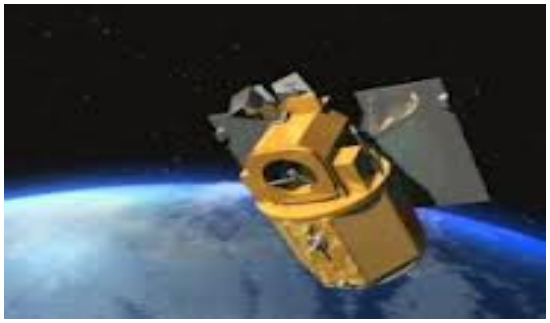
- **Virtex-5QV is the qualification vehicle**
  - Has the largest die, the largest package, the most solder bumps, and the highest pin counts among all Virtex-4QV and Virtex-5QV packages
  - 3 assembly lots built from 3 wafer lots are required for qualification
  - All lots will be processed per Mil-PRF-38535 requirement
- **Major qualification tests include:**
  - Group A
  - Group B
  - Group C
  - Group D
  - Group E
  - Additional Temperature Cycles with CSAM
  - Biased HAST
- **CN Qualification data will be utilized for MIL-PRF-38535 class Y certification**

Missions with Virtex-5QV



Iridium Next (66+6)
(2015 Launch)

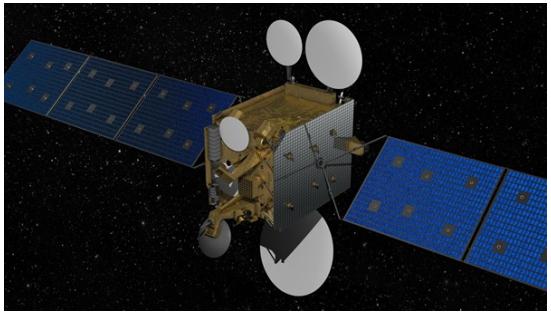
Glonass-K
(2015 Launch)



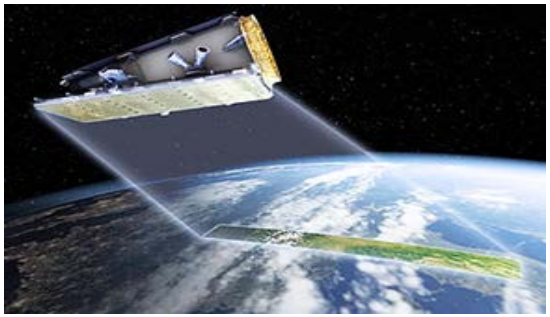
Formosat-5
(2015 Launches)

OSIRIS-REx
(2016 Launch)

LCRD
(2017 Launch)

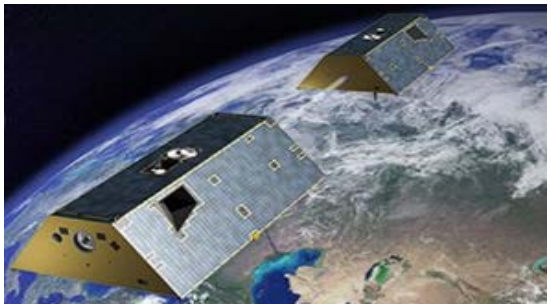


DLR H2 Comm. Sat.
(2017 Launch)



NovaSAR

Orion



Grace Follow-On

Xilinx QML Class Y Certification Plan

- **MIL-PRF-38535 Revision K was released in December 2013**
  - Result of a multi-year (2009 – 2013) effort by Space grade microcircuit suppliers like Xilinx, TI, Honeywell, etc. and users like Boeing, GD, etc. (all JC-13 & G-12 members) and US Government agencies like DLA-LM, Aerospace Corp., NASA/JPL, etc.
- **Xilinx is working with DLA-LM on the class Y certification process for Virtex-5QV**
  - DLA-LM (formerly DSCC) is the owner of QML system and SMD documents and drives the certification process
    - NASA/JPL and Aerospace Corp. will also participate in certification process
  - Xilinx has started arranging for supplier audits
  - Xilinx is developing Qualification Document Package for certification
  - Current Kyocera_6-Sigma built CN package qualification result will be utilized to establish class Y SMD for the Virtex-5QV device
  - Certification process is likely to take at least 2 years

Xilinx Space-Grade Roadmap

V4 Release

10k Hr Lifetest

V5 Design, Qual., & Release

10k Hr Lifetest

ADQ Flow

38535 Class Y (JC13/G12)

V5 Radiation Characterization (XRTC & NASA/GSFC)

QML

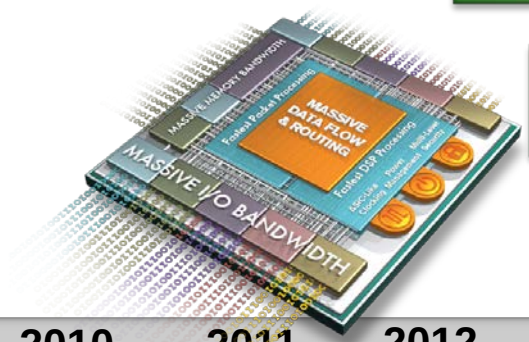
V5QV class Y SMD Certification

CN Pkg Qual

Next Gen. FPGAs

Rad. Char. on 7-Series (XRTC)

on UltraScale (XRTC)



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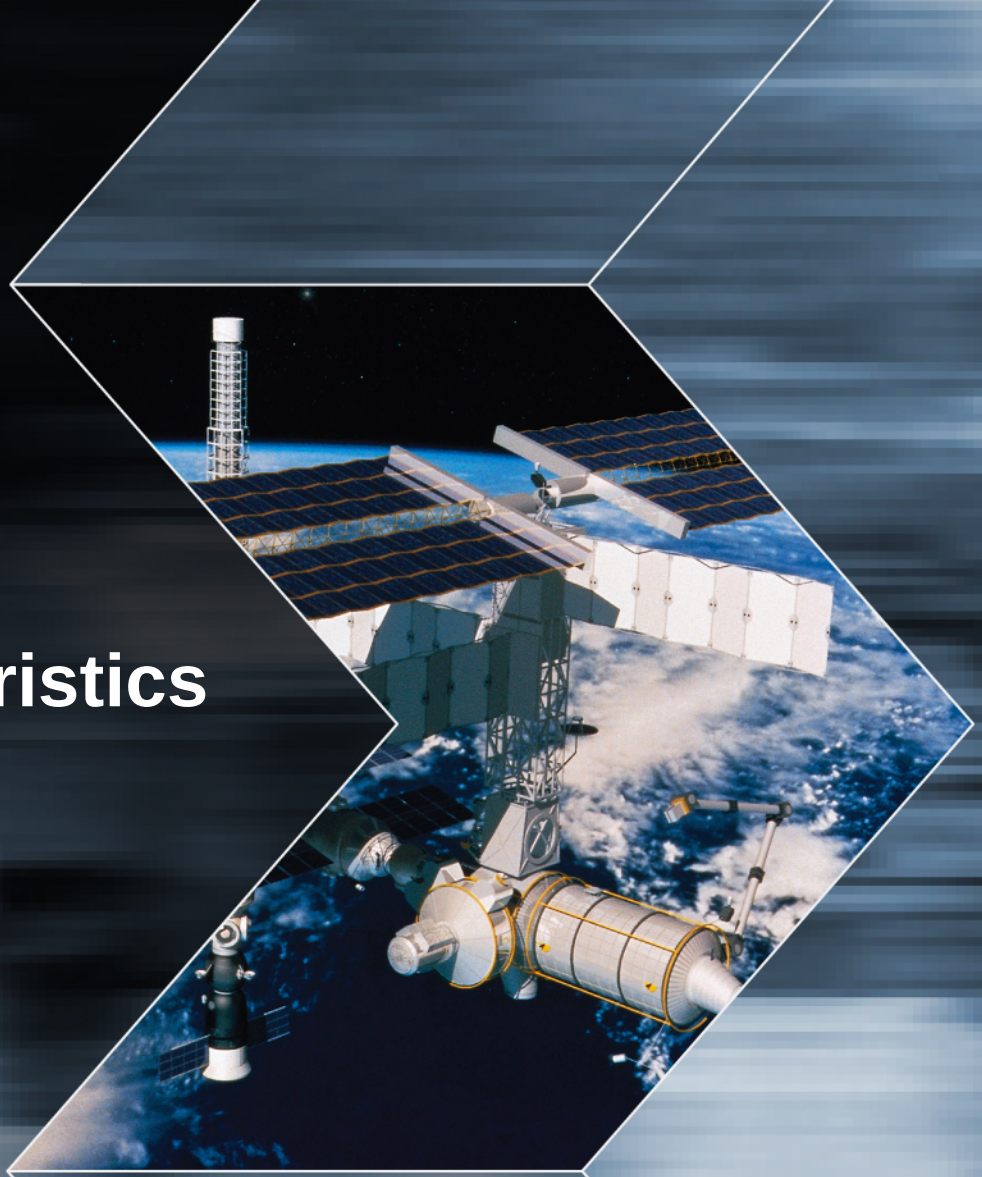
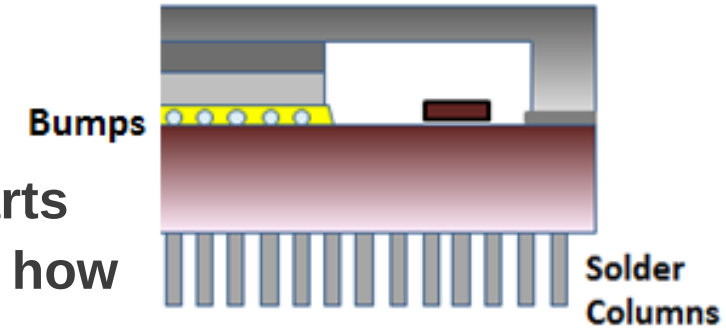


CN Package Characteristics

Construction of Daisy Chain Parts



- **Customers wonders why Daisy Chain parts have no connection through silicon, and how can Xilinx qualify the bumps without it?**

- **There are two package level interconnections (bumps and solder columns) that are qualified separately**
  - First level flip chip interconnect will be qualified by Temperature Cycles at the component level with real silicon device
  - Second level solder column to PCB interconnect (Board Level Reliability Test - BLR) is qualified by Temperature Cycles at the Circuit Board level
    - Daisy chain parts are only needed for BLR qualification
    - Solder bump interconnects already qualified at first level interconnect qualification

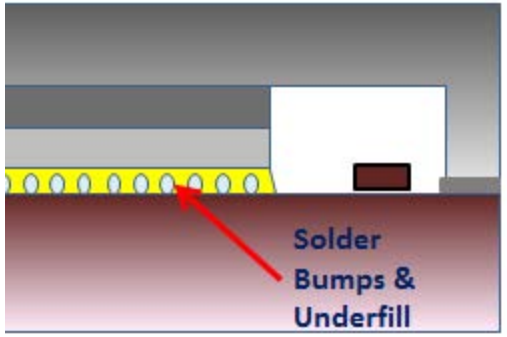
Temperature Cycle (T/C) at Component Level (TM1010) and Board Level (BLR)

- **Flip chip interconnect is qualified with Temperature Cycle tests per MIL-STD-883, TM1010, Condition B or C**
  - Temperature Cycling range is -55ºC to +125ºC for Condition B
  - First 1,000 cycles is required for qualification to pass
  - Second 1,000 cycles is done to collect reliability data
  - Total cycle counts is reduced when Condition C is used (-65ºC~ +150ºC)
- **Board level interconnect qualification tests (BLR) generally follows IPC-9701**
  - Typical Temperature Cycling range is 0ºC to +100ºC
- **Acceleration Factors (Af) calculated based on Coffin-Manson equation for eutectic solder material**
  - Af = 3.8 for TM1010, Cond. B (-55ºC to +125ºC) vs. BLR (0ºC to +100ºC)
  - TM1010, Cond. B for 1,000 cycles is equivalent to 3,800 cycles of BLR
    TM1010, Cond. B for 2,000 cycles is equivalent to 7,600 cycles of BLR

Temperature Cycle (T/C) at Component Level (TM1010) and Board Level (BLR)

- **Fully functional silicon devices are used for TM1010 Temp. Cycle**
  - Qualification parts are tested at maximum clock frequency
    - Fmax =360 MHz
    - Fgtxmax = 4.25 Gb/s
  - Degradation at flip chip interconnect will be caught with high speed ATE
  - Flip chip interconnects can be verified much faster than doing BLR (3.8x faster) and easier
- **Using through silicon/bump daisy chain with Board level T/C is unlikely to catch flip chip failures**
  - BLR test equipment has limited sensitivity and only pick up gross degradation through resistance test
  - Daisy chain with silicon Interconnect cannot address high frequency interconnect sensitivity
  - BLR failures occur much earlier and likely to mask out bump failures

Changes on Solder Composition

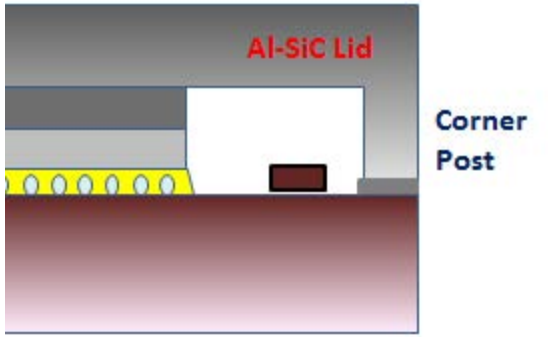


- **Reason for changing solder composition**
  - Supply of high lead (90% Lead) bumps is discontinuing in 2~3 years, Xilinx decided to change it now with CN package qualification
  - Solder paste for capacitors also changed to maintain process integrity
- **Eutectic solder bumps are proven to be highly reliable**
  - Since 2000 with Virtex-II, Xilinx uses flip chip packaging with eutectic solder bumps for most XC (Commercial) and XQ (HiRel) FPGAs
    - IBM captive process uses high lead bumps for more than 30 years
    - Majority of semiconductor industry use eutectic solder bumps
  - All products are qualified with Lead-Free BGA to meet RoHS requirement
    - Reflow profile require higher peak temperature than eutectic solders
    - No solder bump interconnect failures ever found in flip chip packages
  - Mission critical applications that demand high reliability have long accepted eutectic solder bumps with no issues

Eutectic Solder Flip Chip Qualifications

- **Difference between Eutectic and Pb-Free solder reflow profiles**
  - Eutectic Solder: Melt at 185°C, Reflow Peak at 200°C-235°C (Body)
  - Pb-Free Solder: Melt at 217°C, Reflow Peak at 245°C-260°C (Body)
- **Qualification for Pb-Free Packages**
  - Plastic Pb-Free package qualifications are done with pre-conditioning by subjecting parts through 3x reflow with peak temperature of 245°C–260°C prior to package qualification tests
  - Reliability verified by life test, temp. cycles, etc.
    - Flip chip bump reliability verified with high speed electrical tests, CSAMs and XSEMs
  - 14 years' worth of reliability test summary reported in UG116
- **Ceramic packages see less stress than Pb-Free packages**
  - Lower peak temperature for eutectic solder
  - Smaller CTE miss-match between silicon and ceramic substrate

Lid Change for CN Packages



- **Why change from Silicon Carbide (SiC) to Aluminum-Silicon Carbide (Al-SiC)**
  - SiC lid is IBM proprietary and difficult to source.
  - Xilinx already using Al-SiC lids and have an established source.
- **Adding corner posts to improve mechanical integrity**
  - packages remain Open-Cavity and Non-Hermetic
- **Difference for thermal conductivity is minimum**
  - Thermal conductivity for SiC = ~200 and Al-SiC = ~180
  - SiC lid is 2 mm thick and Al-SiC is 1 mm thick
- **Al-SiC lid has Nickel plated lid finish**
- **The electrically conductive Al-Sic lid is not grounded, need to be connected to ground plane to avoid collecting charges in Space**
  - Need to use electrically conductive epoxy (like silver filled epoxy) when attaching heat spreader on the lid

Board Level Reliability Test (BLR)

- **Xilinx had already completed BLR test with the CF packages**
- **BLR for CN packages with 6-Sigma columns will be conducted**
  - BLR will not gate the CN qualification and production release
- **Xilinx BLR test condition is worse than Space applications**
  - Xilinx BLR test is based on IPC-9701A requirement and used FR-4 boards
  - The CTE miss-match between CGA to FR-4 PCB is worse than typical board material used by Space community
- **IBM 90/10 and 6-Sigma 80/20 columns are very similar**
  - Same diameter, same length, same pad layout rules
  - Both are attached to substrates with eutectic solder
  - IBM column is 90%-Pb and 10%-Sn
  - 6-Sigma is 80%-Pb and 20%-Sn plus wrapped copper ribbon
- **Users' prior experience with either columns are still valid**

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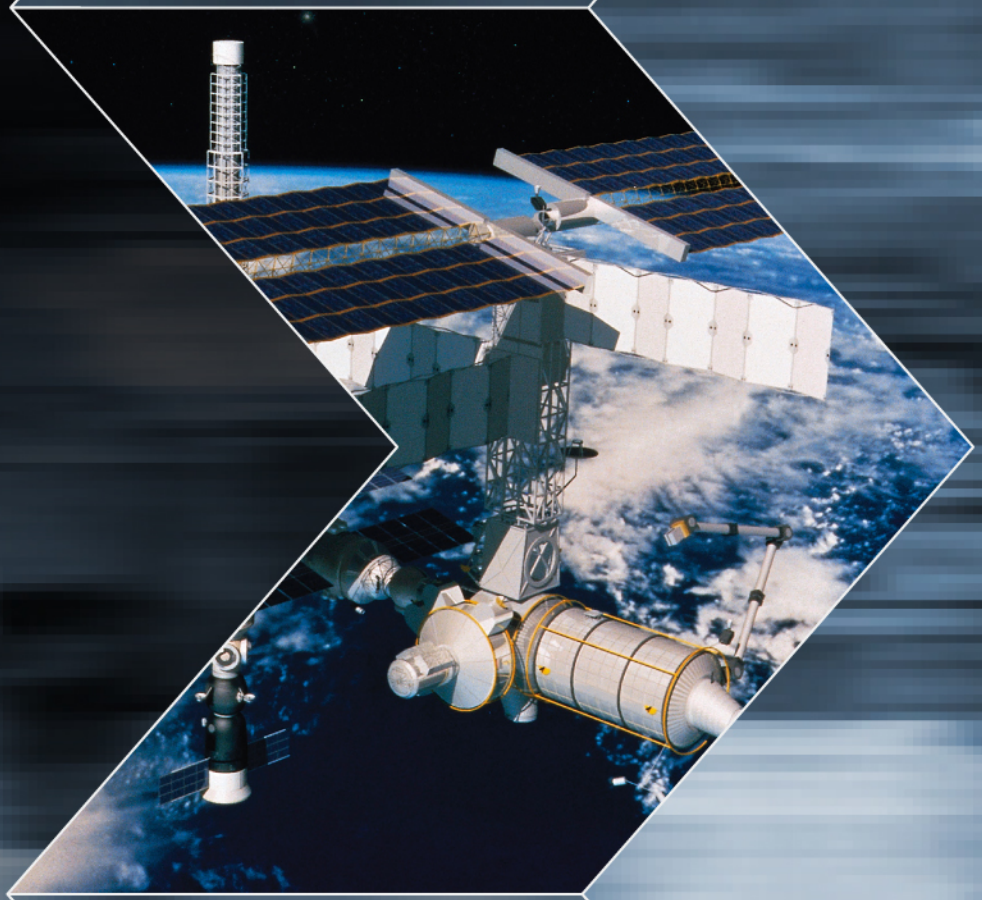

Thanks