1964-2014

→ SERVING EUROPEAN COOPERATION AND INNOVATION

esa

Latent short circuit failure in high-rel PCB caused by lack of cleanliness of PCB processes and base materials

Stan Heltzel
European Space Agency

Outline

1. **Problem description**
    a. Latent short circuit failure
    b. Failure mechanism
    c. Contamination
    d. IR testing

2. **Risk mitigations**
    a. Design
    b. Manufacture
    c. Base material supply

PCB/SMT WG

Space Agencies

esa cnes

PCB manufacturers ESA qualified

SYSTRONIC

TESAT SPACECOM

invotec

Printca GRAPHIC

Leading European OEMs

AIRBUS DEFENCE & SPACE

ThalesAlenia Space
A Thales / Finmeccanica Company

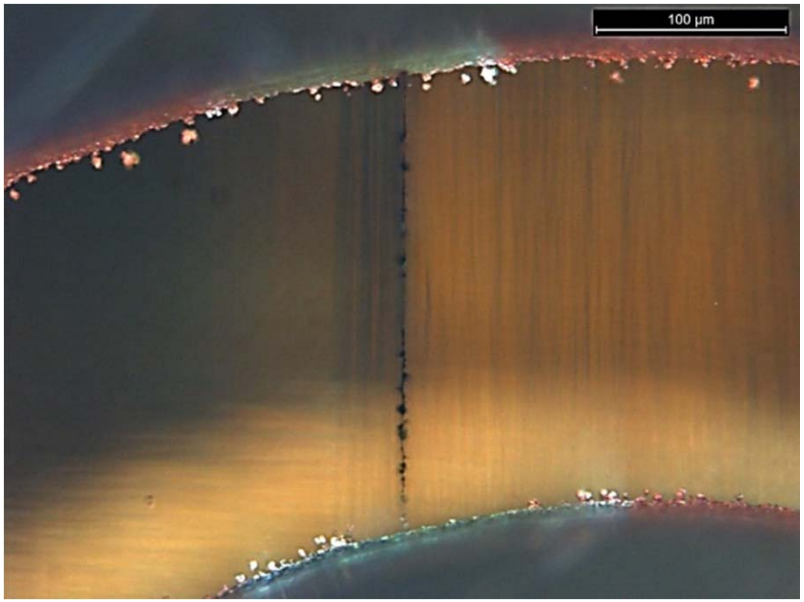
RUAG

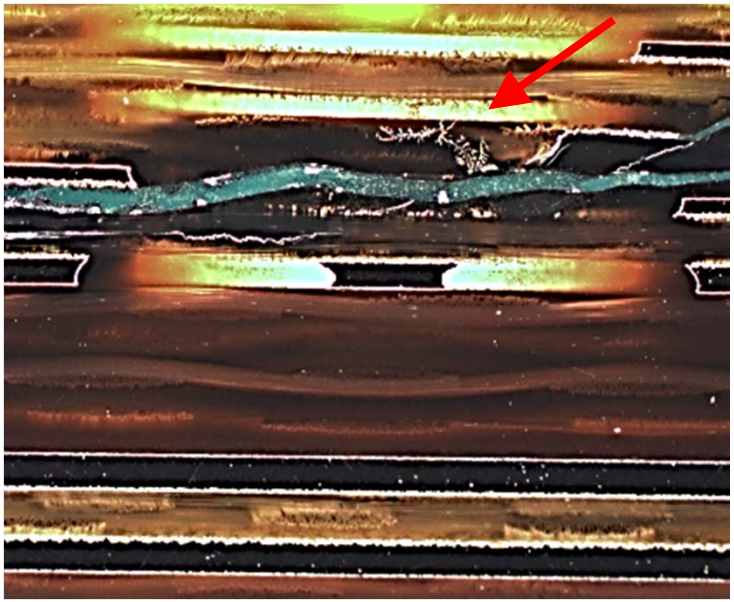
1. Latent short circuit - Introduction

Short circuit failure occurred in PCBs for power distribution

after prolonged functional testing

in ambient lab environment or after thermal vacuum cycles.



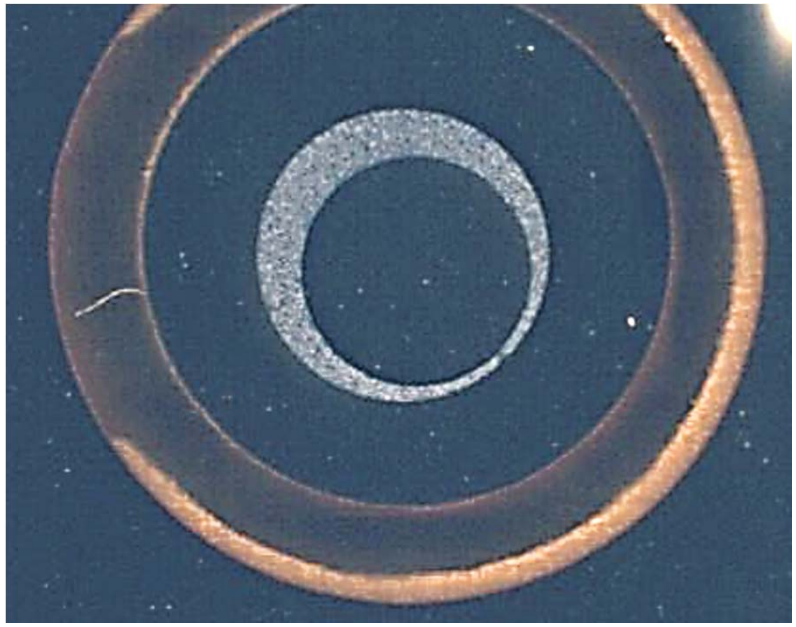


1. Latent short circuit - Failure Mechanism

Electromigration caused by:

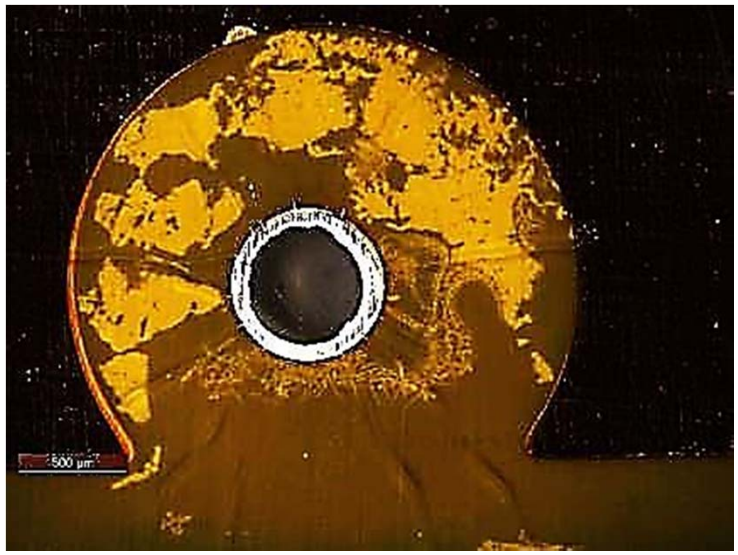
- **Pathway**
- Electrolyte
- Bias voltage

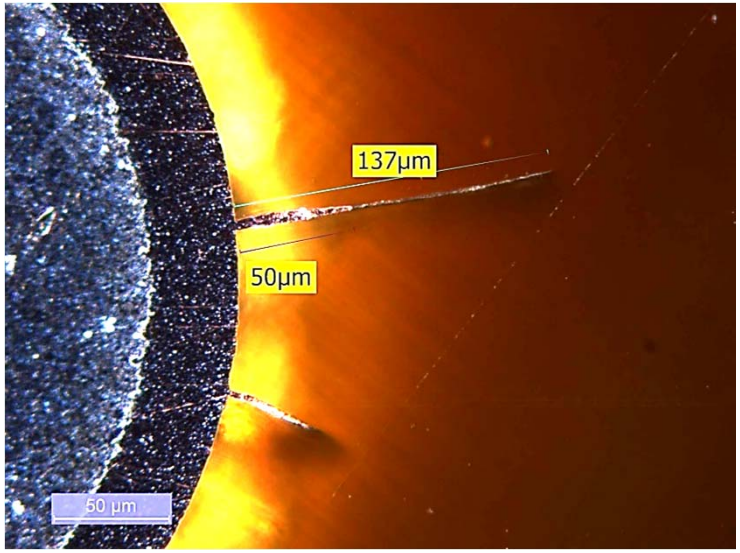
➢ Dendritic growth (SIR)
➢ Conductive Anodic Filament



1. Latent short circuit - Pathway

- Resin-glass interface
  Hollow glass fibers
- Congolmerated flame retardant
  or fillers
- Delamination
  Voids
- Cracks [EA-2010-MAT-12B]
- **Contamination** by foreign material





1. Latent short circuit - Contamination

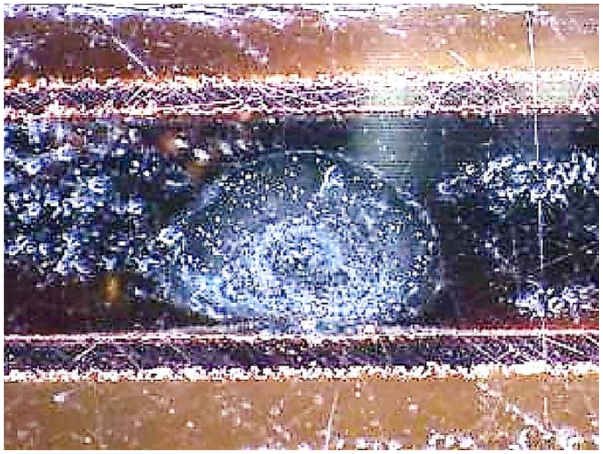
Sources:

- PCB manufacturing processes
- Base material supply

Types:

- Cl-bearing particles
- Metallic debris
- Organic residue
- Dust
- Fibers
- FR4 resin dust in polyimide

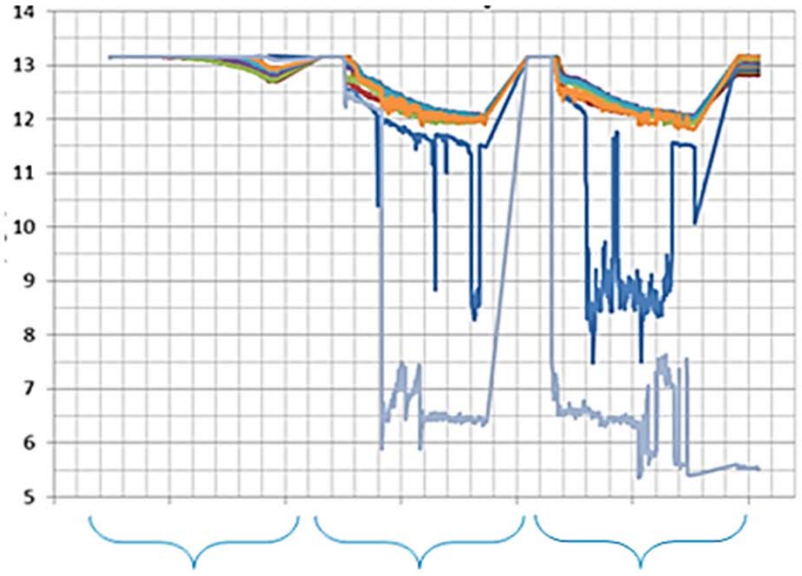
etc



1. Latent short circuit – IR test

http://www.ipcoutlook.org/pdf/insulation_resistance_dieelectric_materials_ipc.pdf

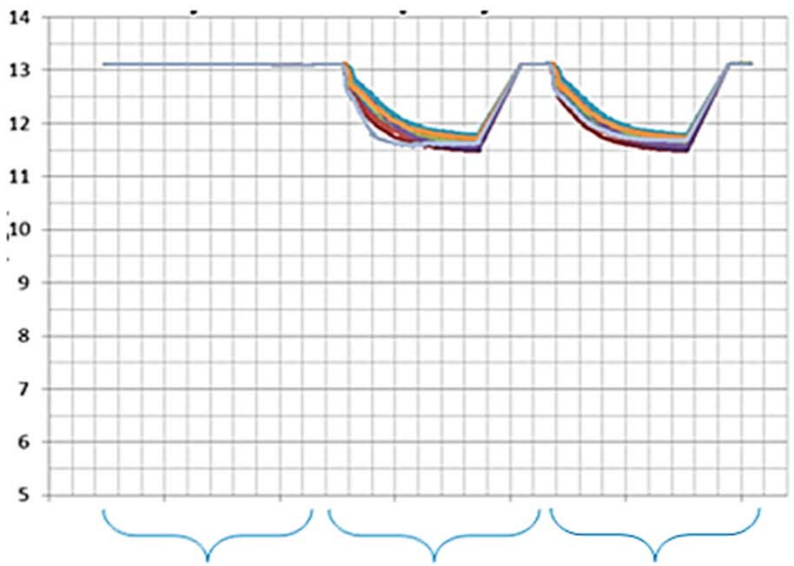
fiber contaminated



T0 **after 200TC** **after 500TC**

breach of insulation after TC

no contamination observed



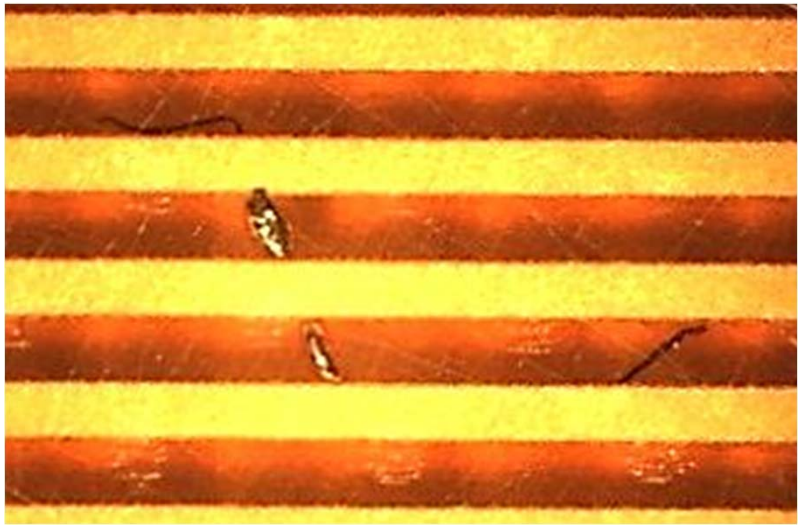
T0 **after 200TC** **after 500TC**

No failures

1. Latent short circuit – IR test conclusions

- 1 kV/mm provide adequate insulation after TC in absence of contamination
- Fiber contamination provides pathway for electromigration

- In this case, PCB manufacturing is the origin of fiber contamination.



2. Risk mitigation – PCB design

www.ecss.nl

IPC-2221

ECSS-Q-ST-70-12 *"Space product assurance – PCB design"*

Example: 4 mil laminate with 2 oz Cu can have a min projected peak-to-peak dielectric thickness of 68 µm.

- Take account of tolerances in dielectric thickness
- Take account of etching tolerances for in-plane clearances
- Margin for double insulation of critical signals
- Presence of non-functional pads
- 2 sheets of glass reinforcement between copper layers

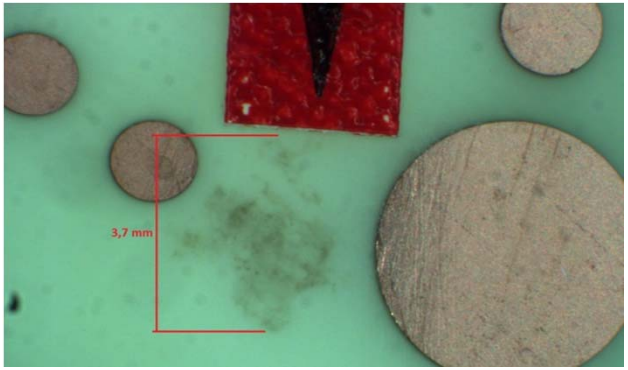
2. Risk mitigation – PCB manufacturer

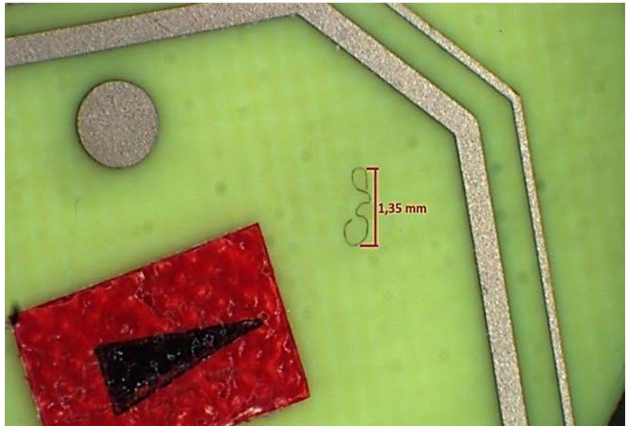
a) Incoming sample inspection on base laminate

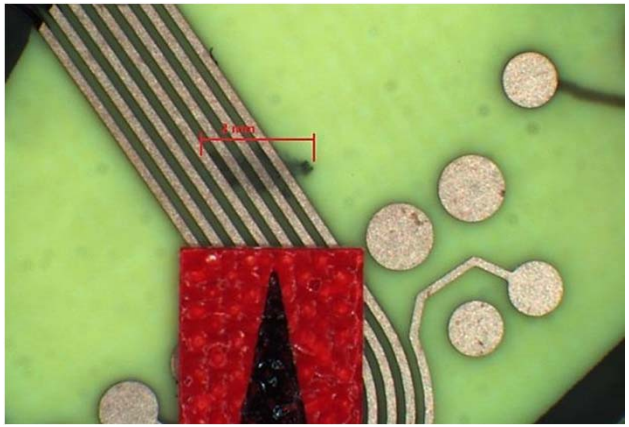
2. Risk mitigation – PCB manufacturer

b) Inspection on etched inner layers:

100% visual inspection on light table



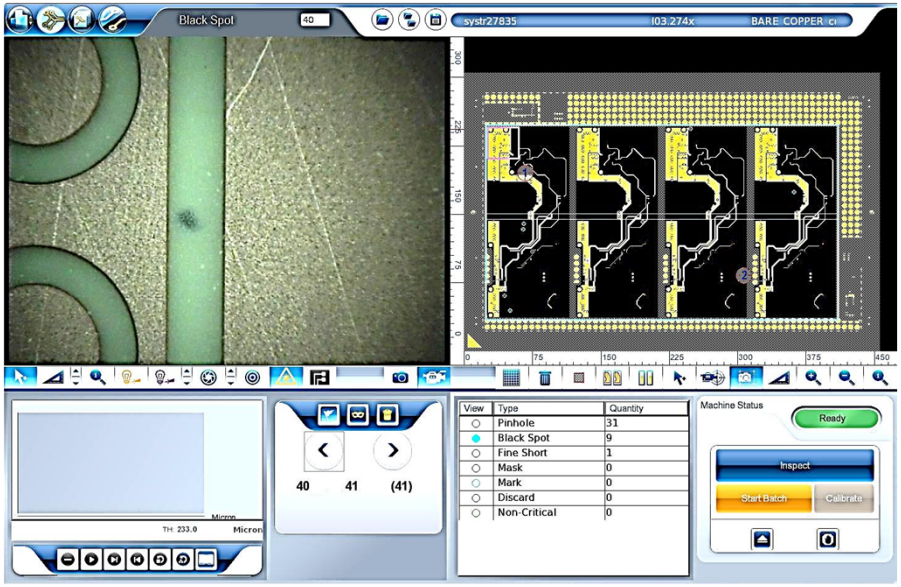


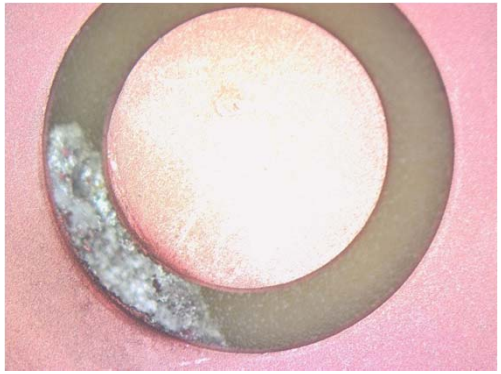


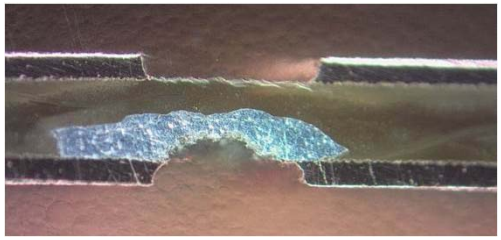
2. Risk mitigation – PCB manufacturer

b) Inspection on etched inner layers:

AOI







2. Risk mitigation – PCB manufacturer

c) Cleanliness control plan

QT/2013/730/SH
www.escies.org/pcb/

Recommendations:

- Cleanliness control between Cu oxidation and lay-up
- Restrictions on the use of materials that show static charging
- Class 100‘000 cleanroom in lay-up area
- Class 1‘000 cleanroom on flow bench
- De-ionisation equipment at lay-up

2. Risk mitigation – PCB manufacturer

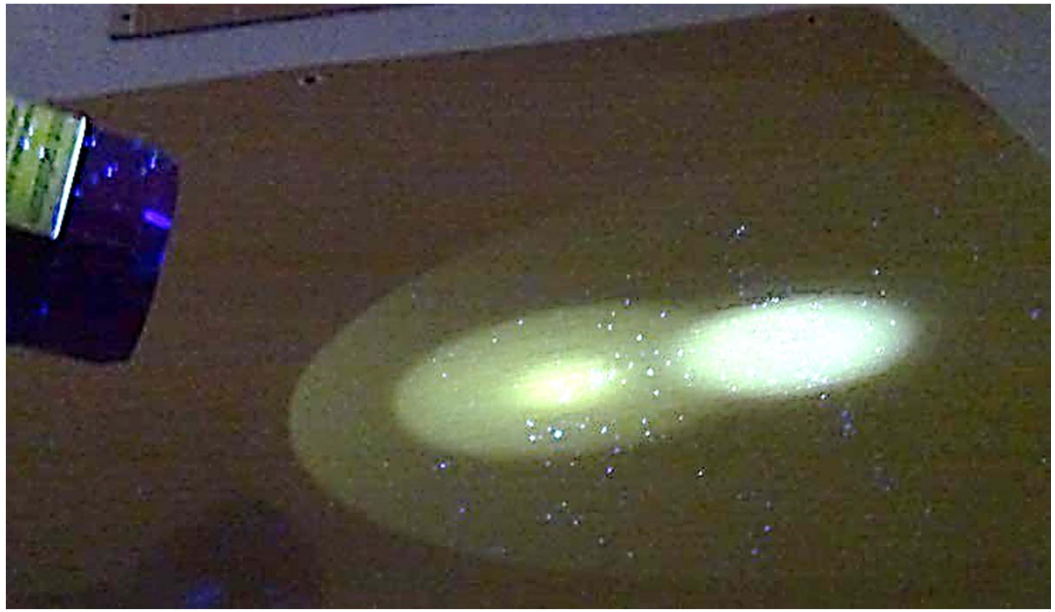
d) Cleaning and inspection of ecthed inner layers and prepreg

Clean

- ‘tacky‘ roller
- vacuum hovering

Inspect

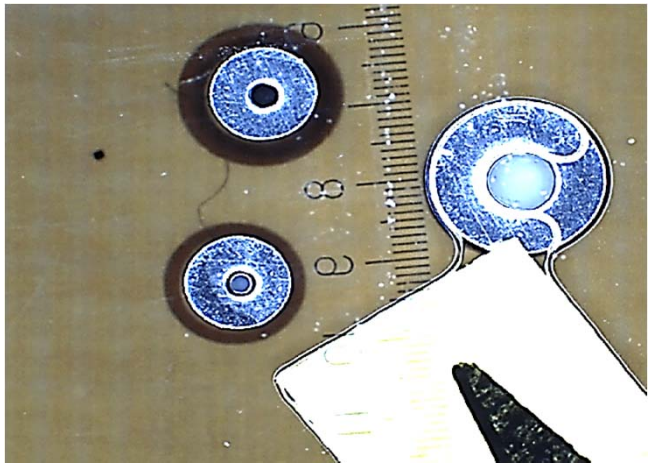
- UV fluorescence
- bright light

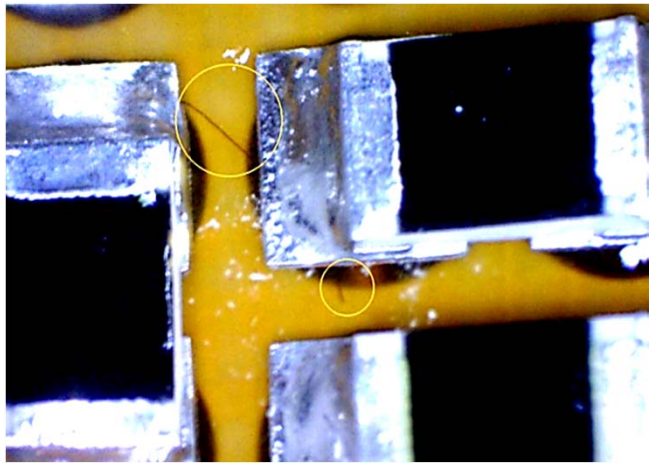


2. Risk mitigation – PCB manufacturer

e) Inspection on external layers

Note: these are laminates, not prepreg





2. Risk mitigation – PCB manufacturer

f) High resistance electrical testing

www.escies.org/pcb/

IPC-9252	IPC6012 class 3/a	QT/2013/681/SH
10 V	250 V	250 V
10 MΩ	100 MΩ	1 GΩ

- V drop during ramp up is a failure
- Direct resistive testing
- 1.27 mm adjacency

2. Risk mitigation – Base material supply

- Incoming sample screening of laminates
- Inspection on prepreg

o Claims accepted if non-compliant to IPC-4101

o Other claims mostly also accepted.

✓ Collaboration with key suppliers to raise awareness, improve understanding, define test and inspection and to define new procurement spec.

2. Risk mitigation – IPC-4101 base laminate

- Test frequency
- Pass/fail criteria
- Consequences of failure

3.8.3.1.6 Surface and Subsurface Imperfections

e. The foreign inclusions are translucent.

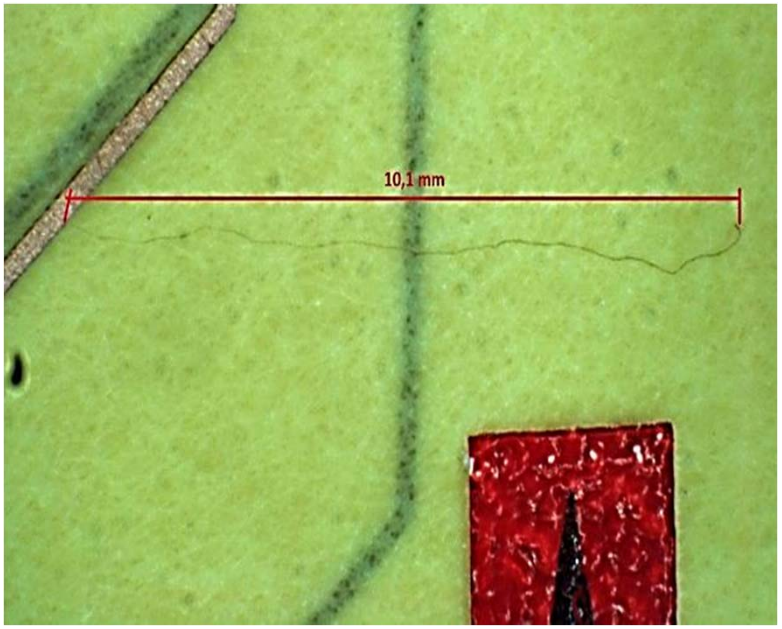
f. Opaque foreign fibers are ≤13 mm [0.512 in] in length and average no more than one per 300 mm x 300 mm [11.81 in x 11.81 in] inspected.

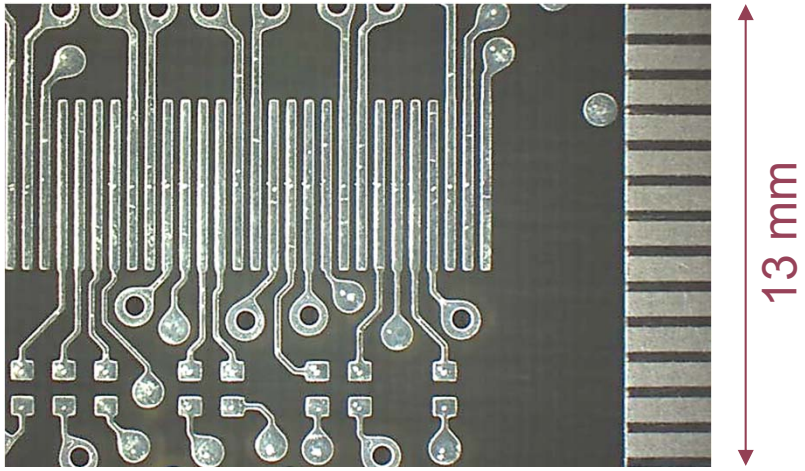
g. Opaque foreign matter other than fibers **shall not** exceed 0.50 mm [0.019 in]. Opaque foreign inclusions <0.13 mm [0.005 in] **shall not** be counted. Opaque foreign inclusions between 0.50 mm [0.019 in] and 0.13 mm [0.005 in] inclusive **shall** average no more than two spots per 300 mm x 300 mm [11.81 in x 11.81 in] inspected.

Table 3-1 Reference Information and Test Frequency of Laminate

Tests	Requirement Paragraph	Test[1] Method	Qualification Testing	Conformance Testing	Conformance Testing Frequency	Specimens per Sheet Sampled
General						
Visual Properties	3.8.3.1	2.1.5	✓	✓	Audit[2]	-
Surface Finishes	3.8.3.1.1 - 3.8.3.1.5	2.1.5 2.1.9	✓		Audit[2]	
Surface/Sub-Surface Imperfections	3.8.3.1.6		✓	✓	Lot	3

2. Risk mitigation – IPC-4101 base laminate





2. Risk mitigation – IPC-4101 base laminate

Proposal for cleaner class of base materials [QT/2013/378/SH]

- Prepreg delivered as b-stage cured sheets
- Prepreg for manufacture of laminate

⇒ Increase inspection frequency to 100%

- Laminate

⇒ Reduce permittable fibre length from 13 mm to 0.5 mm

⇒ Increase sample frequency to 2%

⇒ Reject entire lot if test is non-compliant

⇒ High-pot test on laminate AABUS

2. Risk mitigation – IPC-4101 base laminate

Proposed new specification does not describe an ideal material.
It is rather intended as a realistic compromise.

Currently under review by key base material suppliers.

Proposal was not included for rev D of IPC-4101.
Intended to be issued as European space procurement spec.

Conclusions

Contamination in dielectric is a problem:

- Latent short circuit failure has been observed
- IR test demonstrate electromigration along fiber contamination
- Poor yield late in manufacturing process and poor OTD

Risk mitigations specified in following areas:

- PCB design
- PCB manufacture
- Base material supply

Improve cleanliness of base materials:

- Procurement spec to be issued
- Specify cleaner class of base materials in IPC-4101

1964-2014

→ SERVING EUROPEAN COOPERATION AND INNOVATION

esa

Thank you for your attention!