PWB interconnect solutions inc.
IST testing systems and services

Establishing Effective Accelerated Testing Conditions and Criteria for Confirming Reliability for High Density Interconnect Circuits

Bill Birch
PWB Interconnect Solutions Inc.

PWB interconnect solutions inc.
IST testing systems and services

Introduction

• Increasing numbers of high reliability products are implementing High Density Interconnect (HDI) structures, due to reducing geometries of devices
• HDI structures experience different stresses and failure modes during operation in the end use environment.
• Traditional reliability screening has proven ineffective at identifying defects
• Manufacturing HDI structures requires specialized knowledge, chemistry, equipment and product conformance/failure analysis capability.
• Lead Free assembly is more stressful to HDI structures
• The PWB industry has only one standard for testing interconnect structures

• This presentation and submitted technical paper will discuss:

• Test vehicle designs that represent the product's interconnect structures
• Reliability testing with highly sensitive and continuous resistance monitoring
• Why changes to the present standard may be warranted

PWB interconnect solutions inc.
IST testing systems and services

History of 10% Criterion (Early 1960's to Today)

• Origins: IPC (TM650) and Mil Standard (55110)

• The criterion was based on oven testing of difunctional epoxy materials which had a Tg of 115-118°C

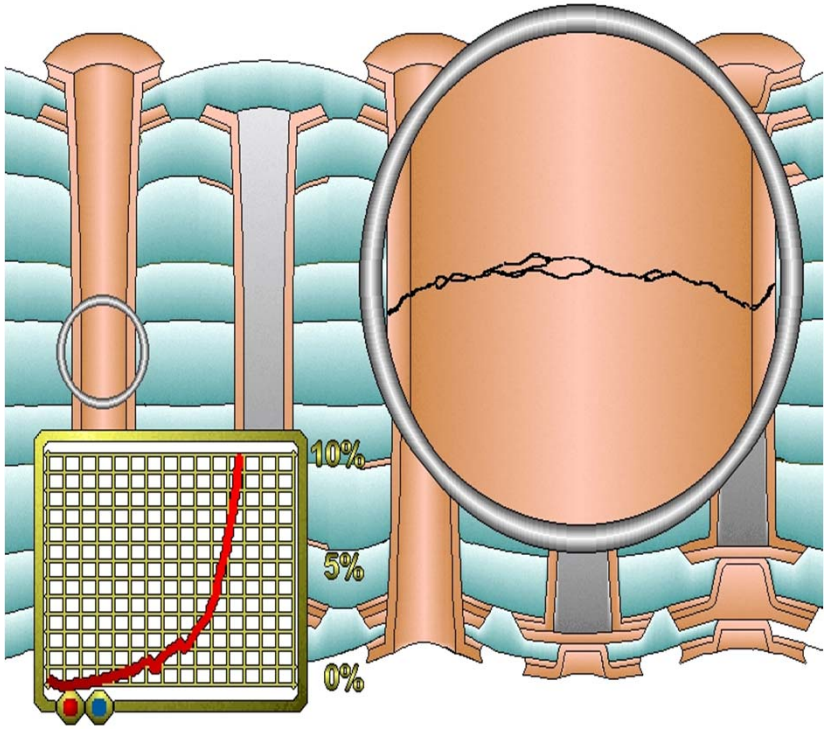
• Accelerated reliability testing was specified with an upper temperature of 125°C, just above the material Tg, applying higher levels of stresses associated to the resin systems beta CTE

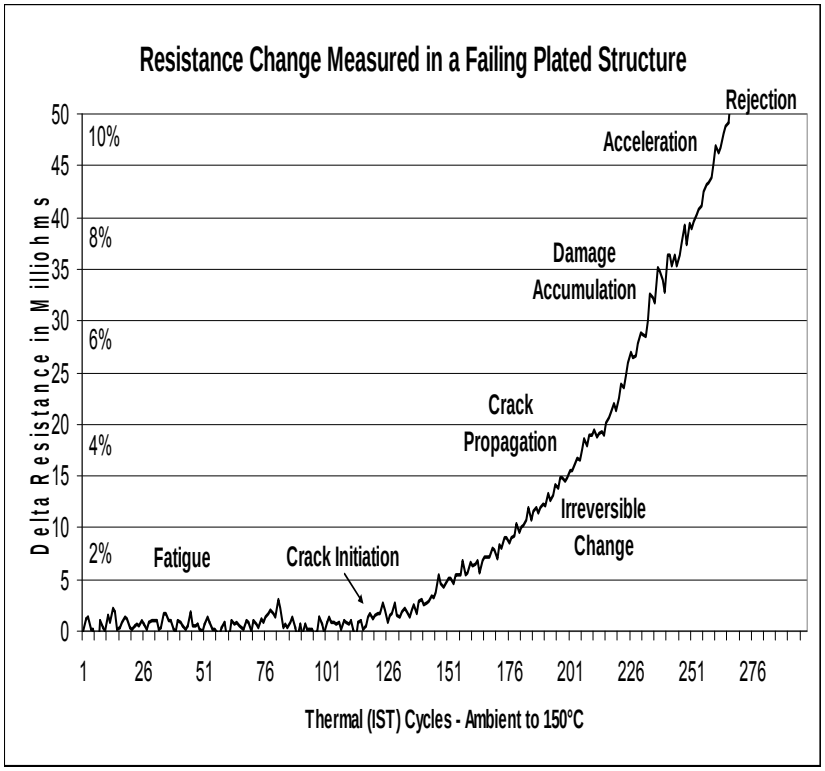
• The 10% criteria was based on the knowledge that a fully cylindrical crack had propagated around the plated through hole (PTH) barrel and that failure analysis could easily find root cause during failure (cross-sectional) analysis.

• Only PTH structures were tested, in the "non-assembled" state

PWB interconnect solutions inc.
IST testing systems and services

Expected Hierarchy of Failure – PTH Barrel Crack





PWB interconnect solutions inc.
IST testing systems and services

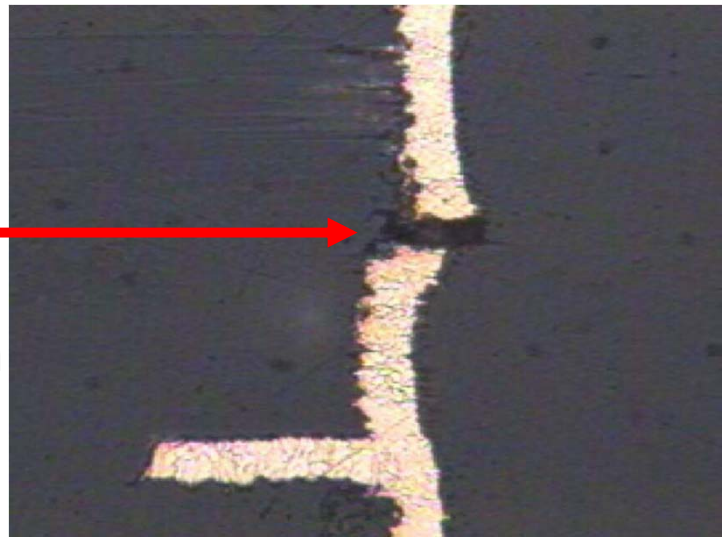
Historic Failure Modes

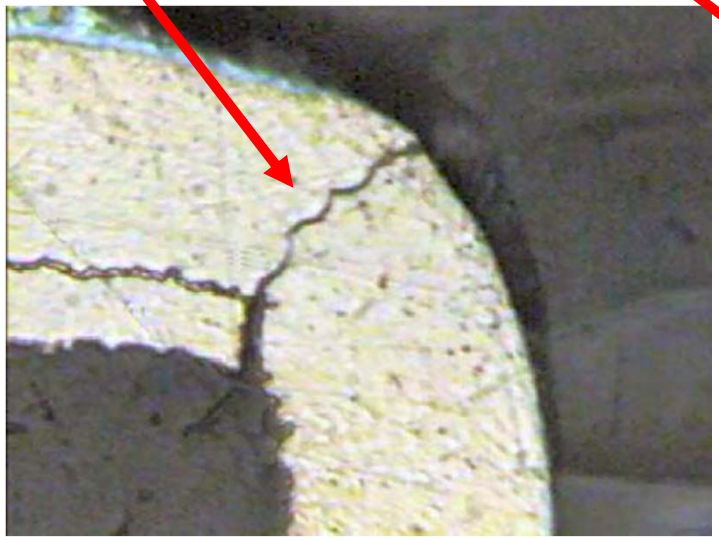
Traditional PTH failure modes

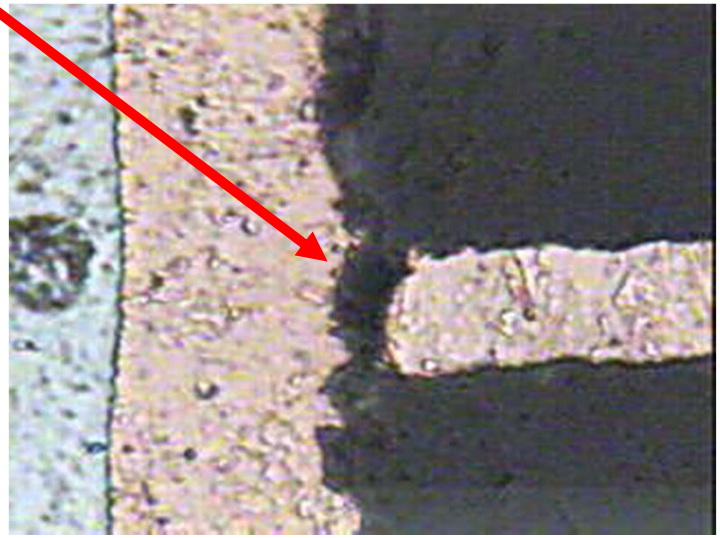
Barrel cracks

Interconnect separation

Knee crack





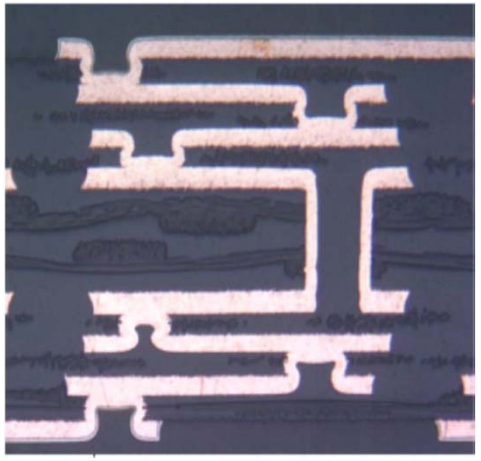


PWB interconnect solutions inc.
IST testing systems and services

HDI Technology - Today

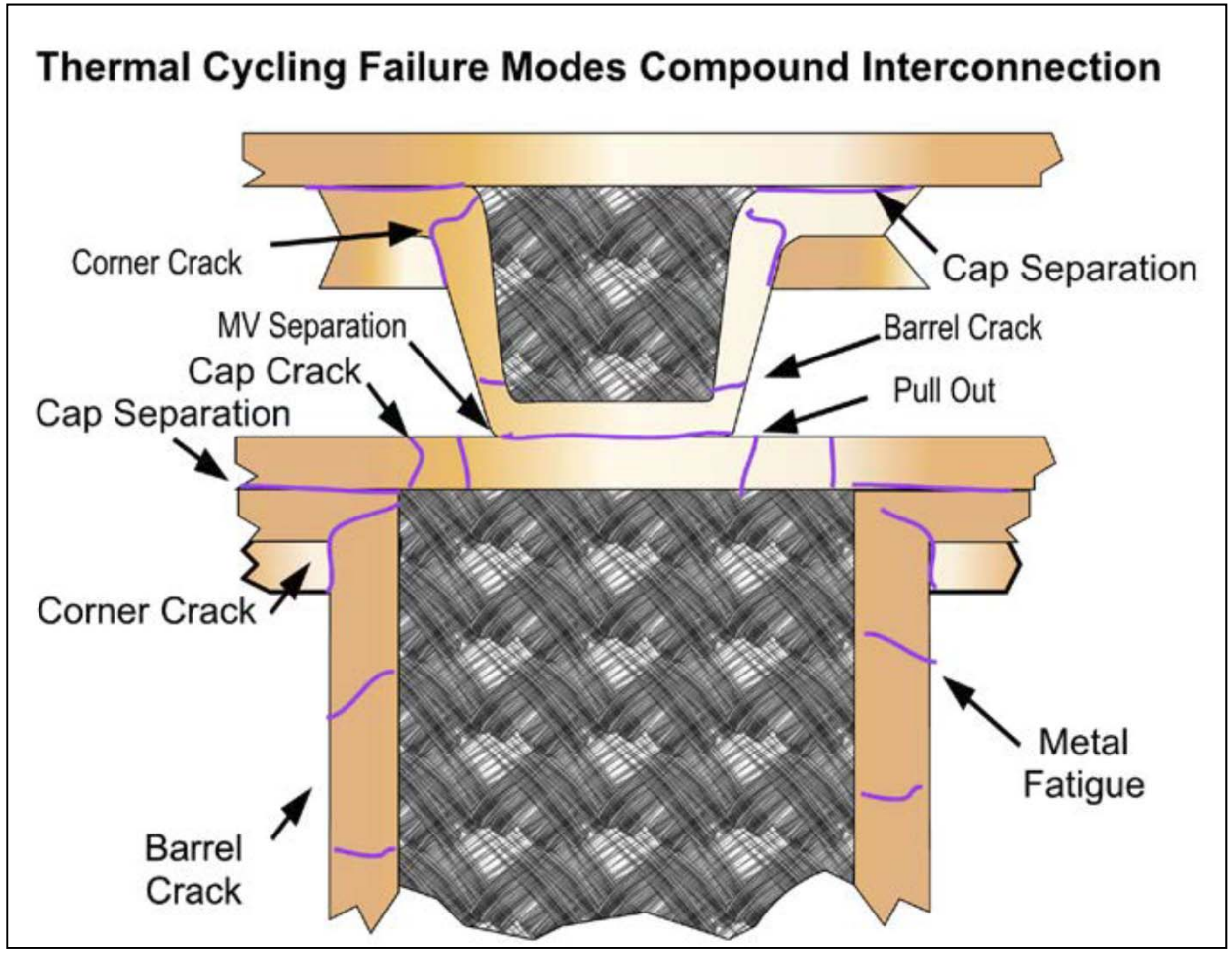
•Device densities drive reduced geometries in HDI - (designs combine blind, buried, stacked and staggered microvia structures)
•Increasingly zero PTH structures are included in product designs (full SMT)
•Sequentially laminated, thin dielectrics using FR4 / Polyimide resin systems with Tg's ranging between 150-250°C.
•Advanced measurement and monitoring equipments are available
•Assembly/rework conditions must be included in testing protocol

Example: 3-2-3
Sequential build-up



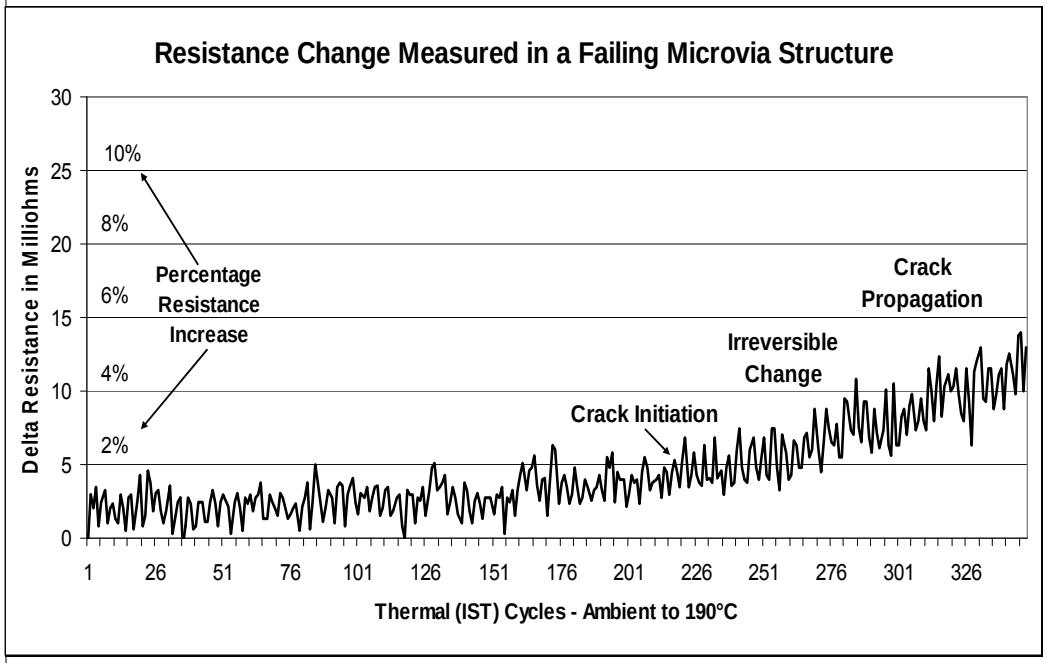
PWB interconnect solutions inc.
IST testing systems and services

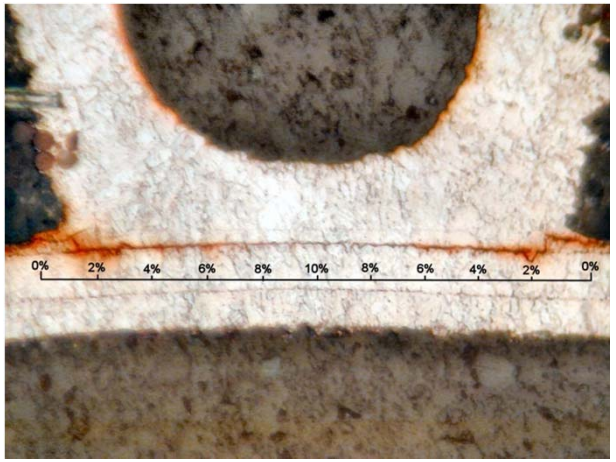
HDI Failure Modes

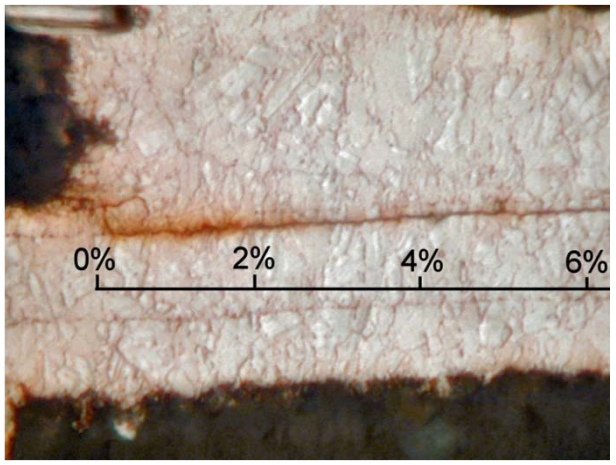


PWB interconnect solutions inc.
IST testing systems and services

Fatigue/Wear-out of an HDI Structure

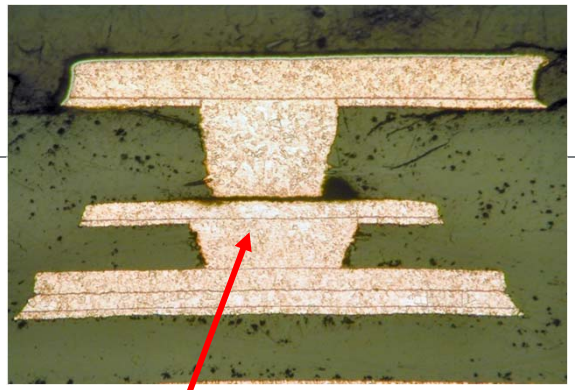


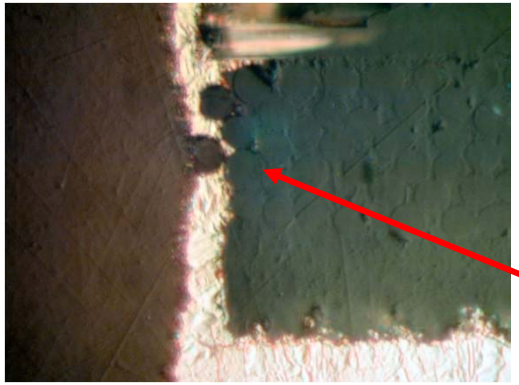




PWB interconnect solutions inc.
IST testing systems and services

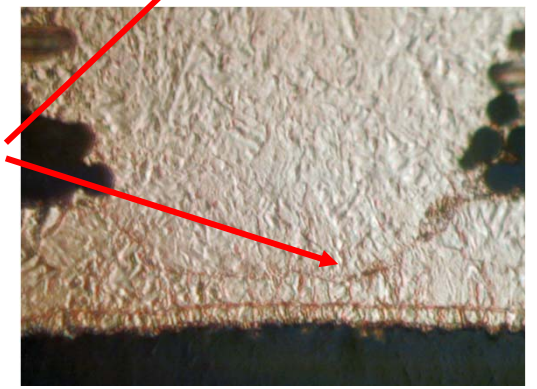
HDI Failure Modes



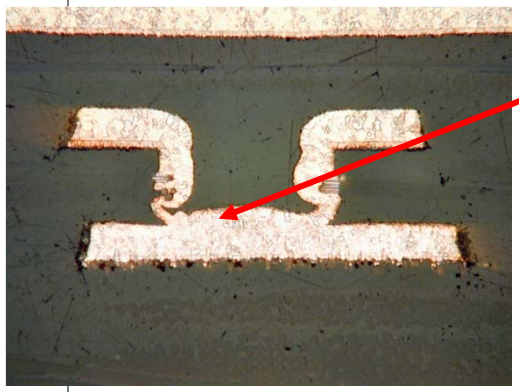


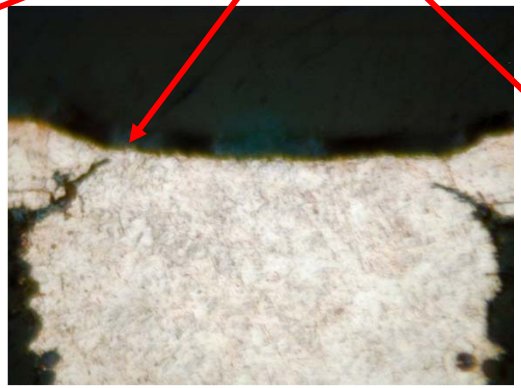
Microvia separation

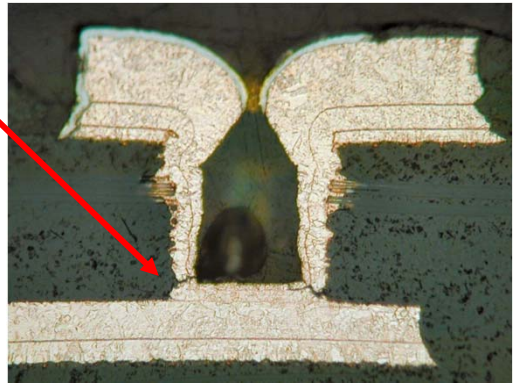
Interfacial separation



Copper fatigue

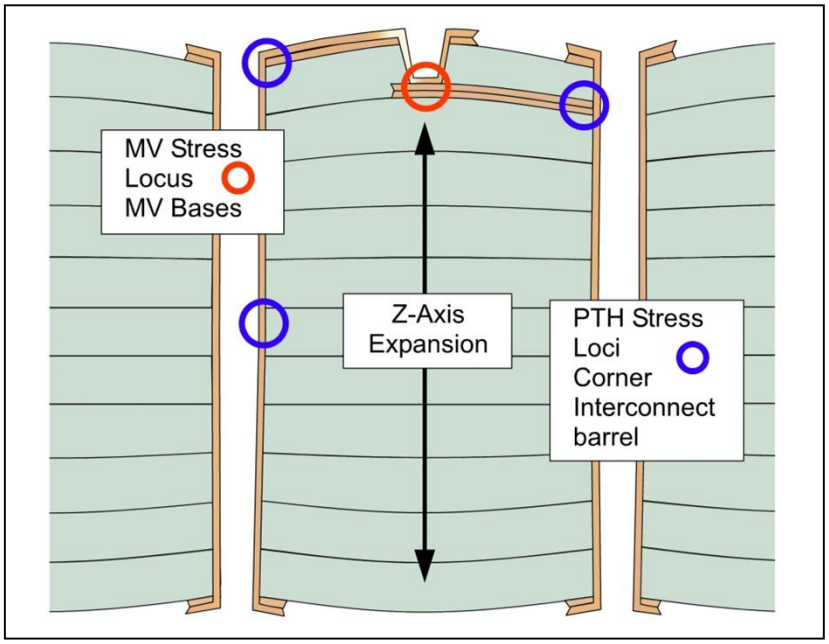


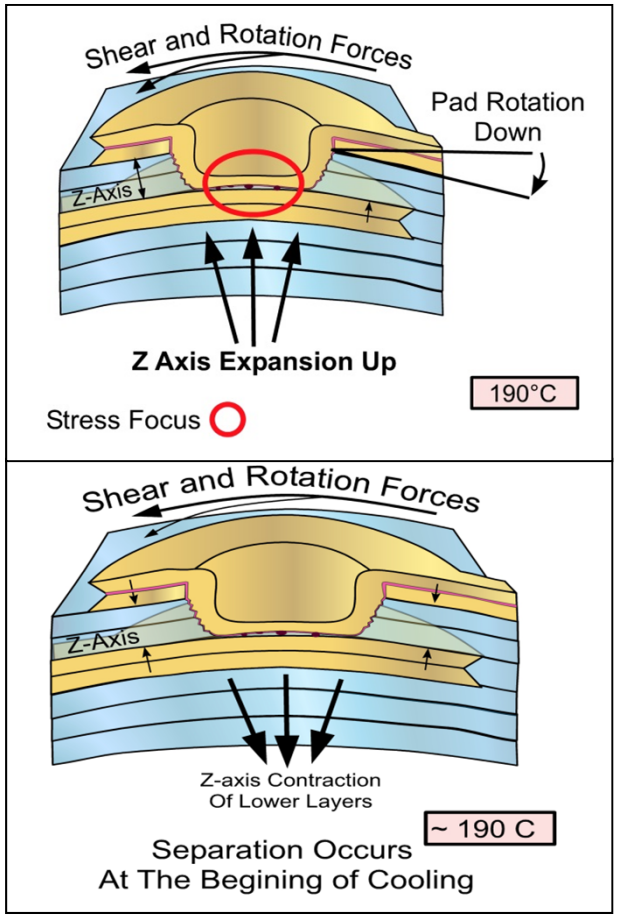




PWB interconnect solutions inc.
IST testing systems and services

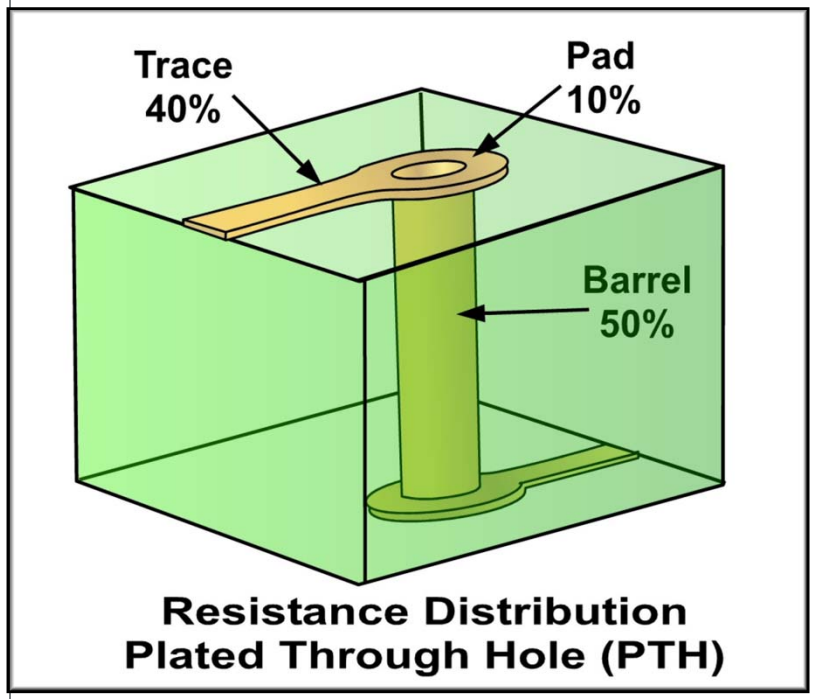
Physics of PTH and HDI Structure Failures

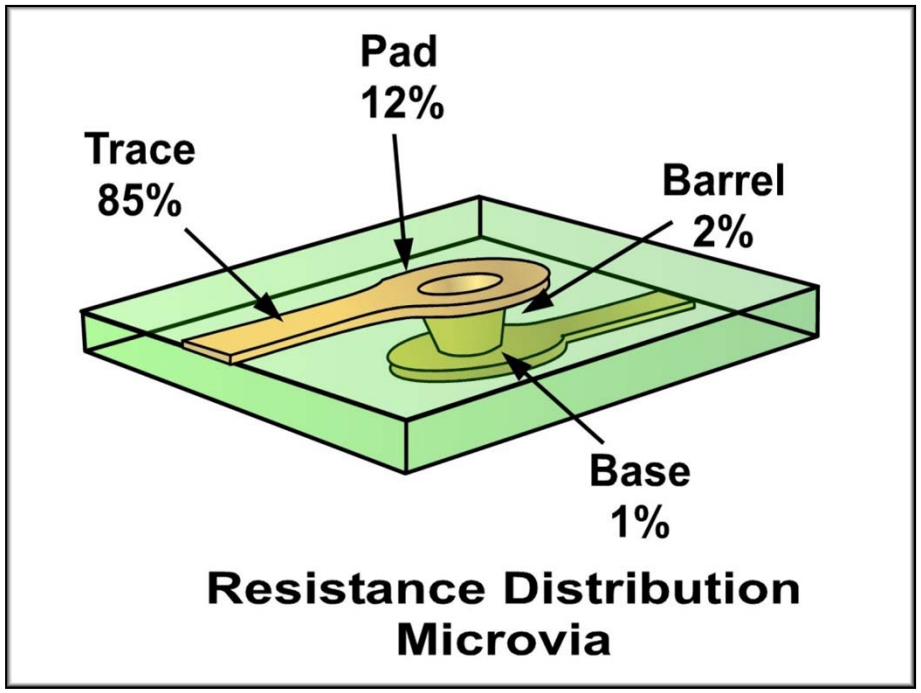




PWB interconnect solutions inc.
IST testing systems and services

Resistance Distribution of PTH Vs HDI Structures





When a PTH test circuit fails at 10%, the required increase in the PTH barrels bulk resistance must exceed 20%

When a microvia to target pad test circuit fails at 10%, the required increase in the microvias bulk resistance must exceed 1000% (virtual open)

PWB interconnect solutions inc.
IST testing systems and services

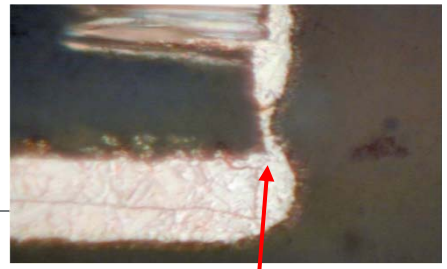
Test Circuit Resistance Distribution and Effective Increase Required to Measure the Industry Standard 10% Rejection Criteria

0.15mm Microvia Structures	Via to Trace/Pad Ratio	Trace to Via/Pad Ratio	Pad to Via/Trace Ratio	Effective Increase to measure 10%
Interface	1%	87%	12%	1000%
Single Via	2%	86%	12%	500%
2 Stack	5%	84%	11%	200%
3 Stack	7%	82%	11%	143%
4 Stack	9%	80%	11%	111%
4 + 4 Stack	36%	51%	13%	28%
PTH	50%	40%	10%	20%

Note 1: 4+4 assumes a buried via is connected between the stacked microvias

Note 2: A 1000% resistance change is effectively an open circuit

PWB interconnect solutions inc.
IST testing systems and services



Case Study Data For Kapton (Flex) Based HDI Substrates

IST Cycles to 10% failure, ambient = 210°C

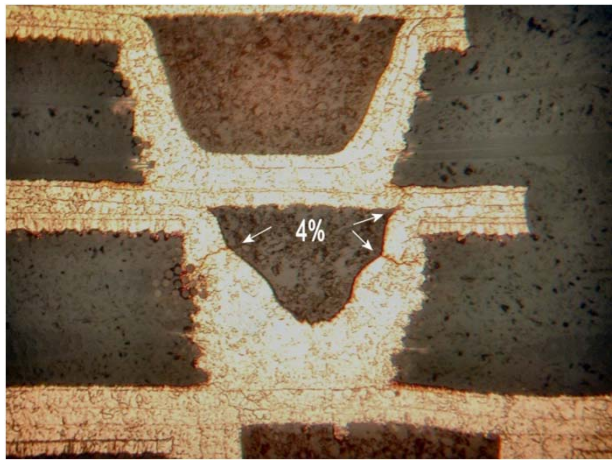
Coupon	Cycles	P%	S1 %	S2 %	S3 %	Result
1	250	3.0	1.3			Accept
2	250		0	0.3	0.1	Accept
3	250	3.8		0.8	0.8	Accept
4	250		0.1	0.1	0.1	Accept
5	250	8.7	3.1			Accept?
6	250	0.7		0.1	0.2	Accept
7	250	6.0	2.3			Accept?
8	250	5.9		0.2	0.1	Accept?
9	250	3.7	1.4			Accept
10	250		0.2	0.2	0.1	Accept

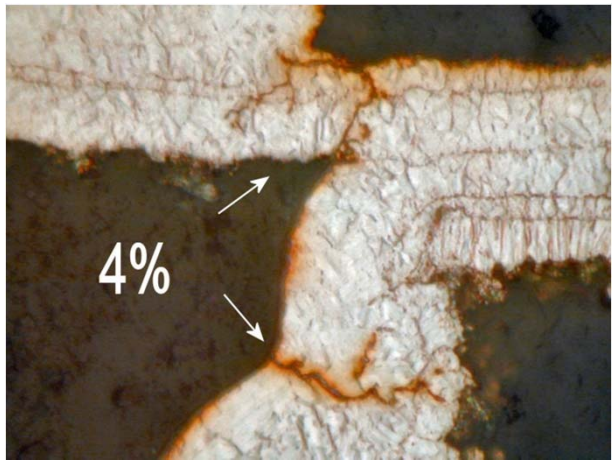
Notes:

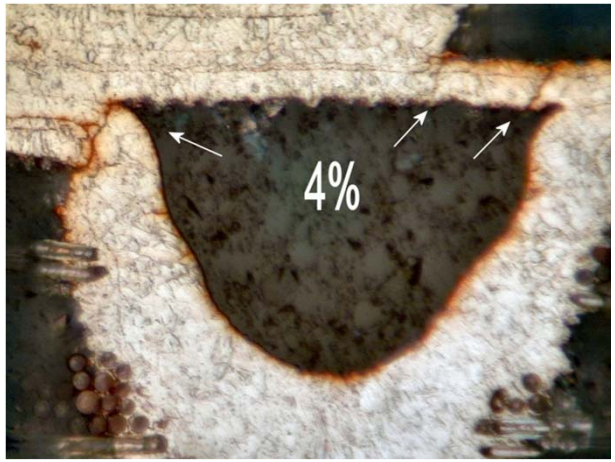
- Nonconforming samples passed the 10% resistance criterion after 250 cycles
- Detecting a 4% criterion is possible with the correct test design and methodology
- A 4% criterion would have captured these nonconforming samples

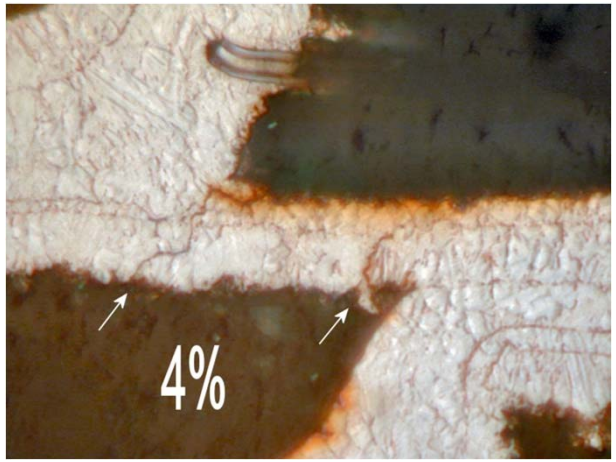
PWB interconnect solutions inc.
IST testing systems and services

Multi-level HDI Failure Modes









PWB interconnect solutions inc.
IST testing systems and services

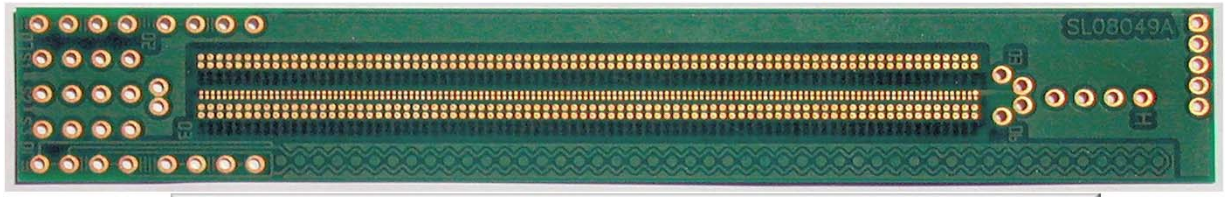
Prerequisites for Effective HDI Reliability Testing

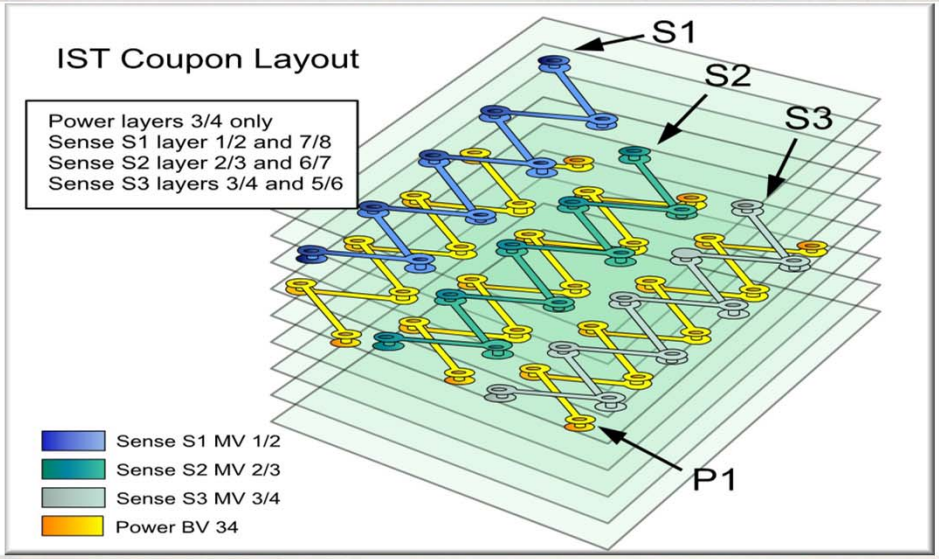
- **Test Vehicle Configured to Achieve Maximum Electrical Sensitivity and Understanding toward the Hierarchy of Failure**
- **Electrical Monitoring of Multiple Simulated Assembly/Rework Temperature Profiles, Completed Before Thermal Cycle Testing Begins**
- **Higher Temperature Testing – At, or Just Above Material Tg**
- **High Speed, High Resolution Multiplexing Measurement System**
- **Fully Automated Continuous Resistance Monitoring**
- **Variable Rejection Criteria**
- **Thermal Cycling That Stops at Failure, Avoiding Confounding Damage**
- **Non-contact Failure Site Detection**
- **Specialized Metrology/Micro-sectioning Capabilities**
- **Understanding of PWB Manufacturing Process and Material Properties to Complete Effective Failure Analysis.**

PWB interconnect solutions inc.
IST testing systems and services

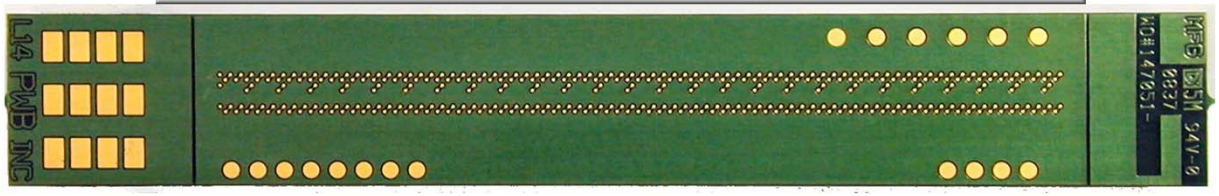
Intelligent Test Vehicle Design (Duplicates Product)

PTH Used





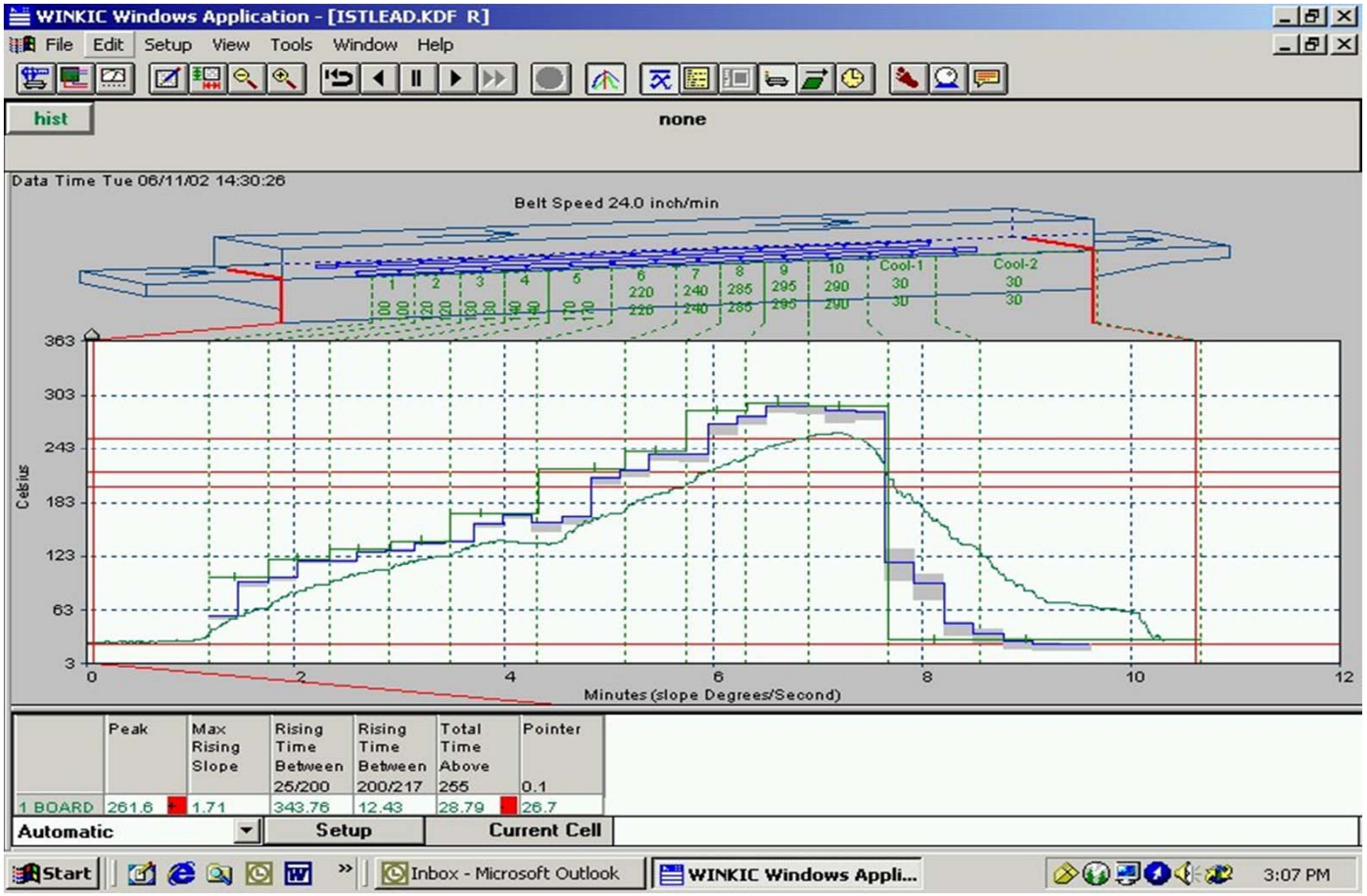
SMT Only



PWB interconnect solutions inc.
IST testing systems and services

Lead Free Assembly Environment

Must be Part of HDI Structure Reliability Assessment



PWB interconnect solutions inc.
IST testing systems and services

Test Methodologies

- Compliance to IPC-TM-650, 2.6.26, DC Current Induced Thermal Cycling
- Assembly simulated on tester
- IST has eight test ports, each capable of measuring three test circuits per coupon
- Resistance is monitored continuously
- 300 cycles takes about 24 hours
- Testing may be stopped on individual coupons at a set resistance increase

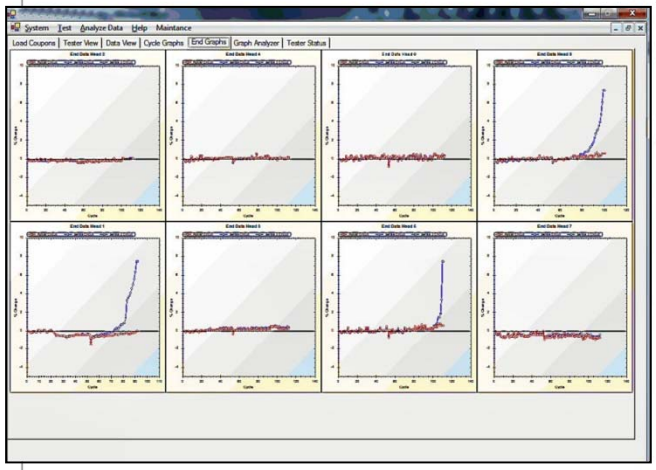
- Ovens can test 100+ ports, in batch type process, measurement time is based on number of samples involved
- Resistance is monitored continuously on external equipment (event detector)
- 24 or 48 cycles takes about 24 hours
- Testing can not be stopped on individual coupons at a set resistance increase

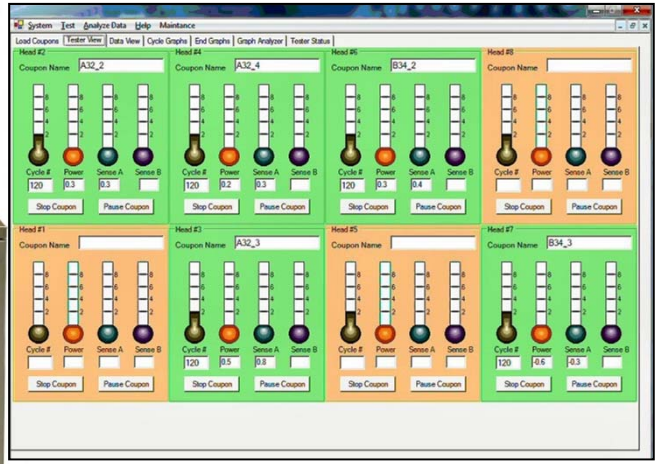
Interconnect Stress Test System

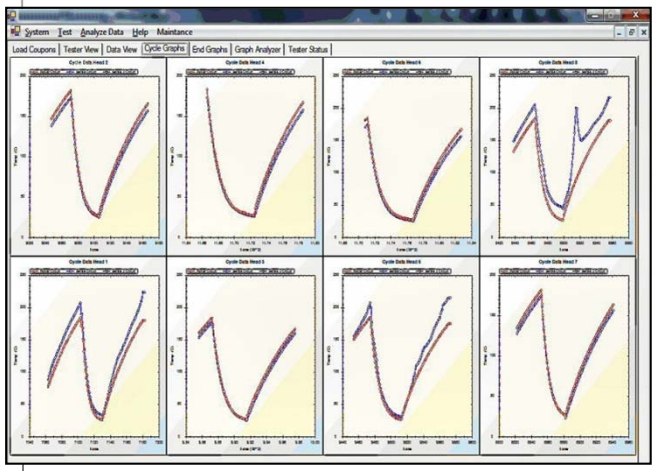
Accelerated Thermal Cycling Chamber

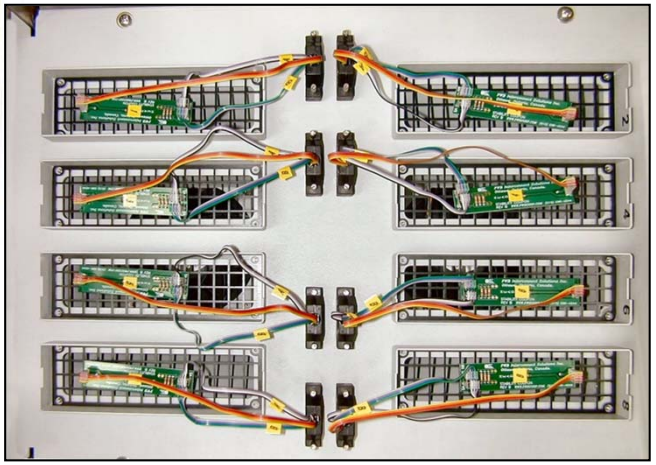
PWB interconnect solutions inc.
IST testing systems and services

I.S.T Accelerated Reliability Test Equipment



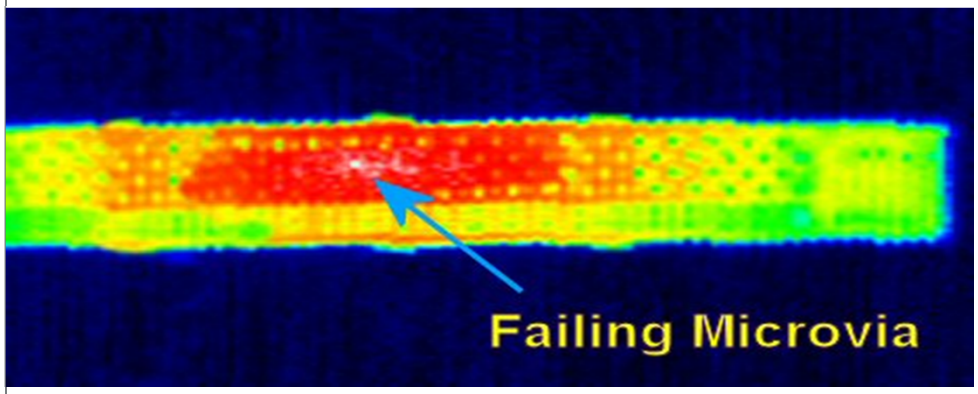


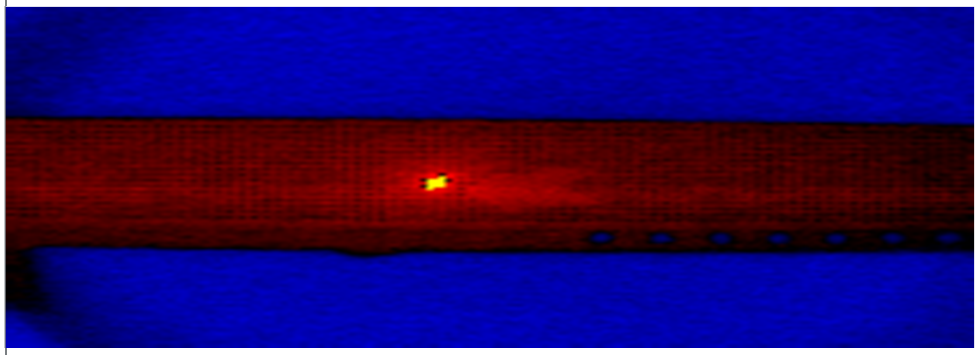


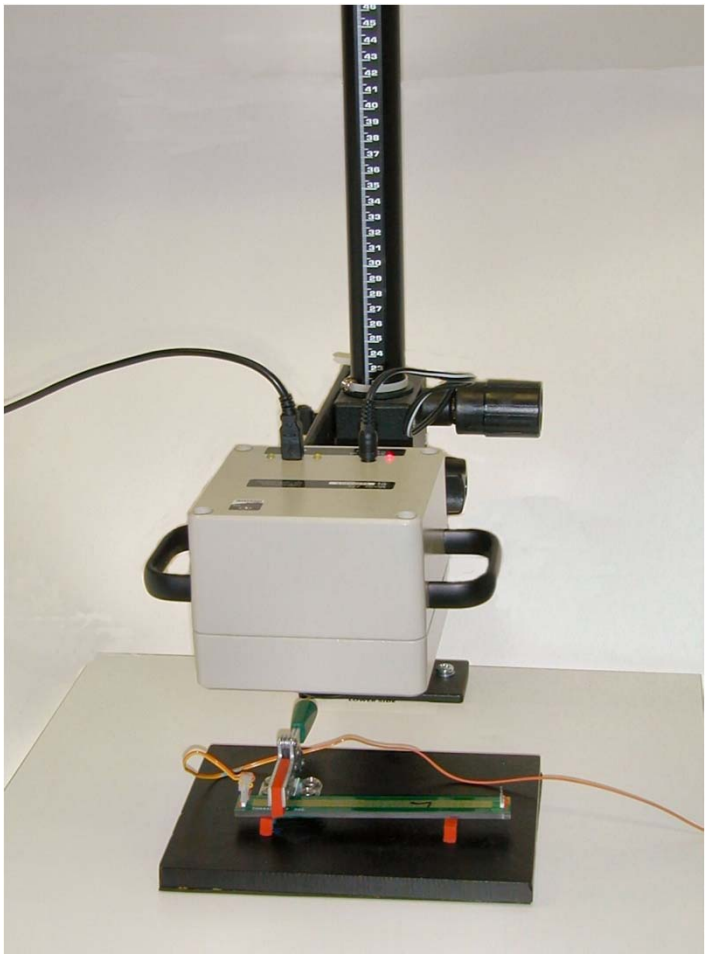


PWB interconnect solutions inc.
IST testing systems and services

Finding Microvia Failures Requires Specialized Tools







PWB interconnect solutions inc.
IST testing systems and services

HDI Reliability Considerations

Single and 2 stack microvias are generally the most robust types of copper interconnections used in HDI applications, increasing the technology to 3 stack and 4 stack requires concerted effort to assure product reliability.

Ranking the inherent reliability of 3 stack and 4 stack structures to other interconnects like plated through holes, blind, or buried vias, will need to be considered in future reliability test programs.

Changes in failure mode should be expected between single, two, three and four stack microvia structures relative to their relationship to and attachment to internal structures (buried vias) toward the center of the PWB construction.

The failure modes associated with multi-level stacked microvia structures include microvia base to target pad separation, microvia barrel cracks, corner cracks, target pad and “cap pull-out”.

PWB interconnect solutions inc.
IST testing systems and services

HDI Reliability Considerations (Cont'd)

- Reliability testing of multi-level microvia structures can be achieved effectively with engineered coupons based on actual product construction design rules.
- Accelerated life testing requires test temperatures just above the material Tg to effectively discern HDI structure reliability.
- Thermal cycle testing of microvias is effective at 190°C for FR4 based dielectrics material, these increased temperatures effectively demonstrate that 1 and 2 stack microvia are robust structures that can survive beyond 3000 IST thermal cycles.
- Lead/free assembly/rework temperatures has increased the stresses experienced by the PWB substrate. These higher thermal excursions degrade the reliability of all interconnections and materials.
- Interconnect technology is changing so rapidly that no industry database is available for designers to understand the reliability trade-offs.
- Implementing reliability testing into actual product is easily achieved.

PWB interconnect solutions inc.
IST testing systems and services

Conclusions

- Specifications calling out a rejection criterion of 10% resistance increase have been in place since the early 1960s
- The criterion does not specify via type, number of vias nor does it consider if resistance change is localized, or global
- PTH failure modes that defined the requirement are not applicable for HDI microvia structures in use today
- HDI microvia structures are a small percentage of the total test net resistance
- Evaluating high-reliability products using HDI technology is improved with an appropriately designed test circuit
- Measurement systems with better accuracy and data transfer speed permit lower level resistance measurement
- The reliability of microvia structures used for meet the challenges of HDI applications must be assessed with exposure to the lead/free assembly environment.

PWB interconnect solutions inc.
IST testing systems and services

Conclusions (cont'd)

- Microvia reliability testing shows that a 4% resistance increase is enough to cross a point of irreversible change
- Root cause analysis can be performed before additional damage is incurred
- Failure analyses found quality non-conformance of HDI coupons on samples passing 10% resistance increase
- **Key takeaway: The rejection criterion for test resistance increase should be tightened from 10% to 4% to ensure maximum efficacy of screen for the reliability of HDI structures**

PWB interconnect solutions inc.
IST testing systems and services

Thank you for your attention!

Contact info:
bill.birch@pwbcorp.com
Canada Prefix: 613-596-4244
http://pwbcorp.com