Stacking of known good rebuilt wafers for high speed memory and Systems in package

Jérome NOIRAY
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Buc, France

Outline

- Introduction
- Wire free Die on Die technology
- High performance memory stacking
- Embedded programmable Module
- Conclusions and outlook

- **Introduction**
- Wire free Die on Die technology
- High performance memory stacking
- Embedded programmable Module
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- French Company founded in 1995
- Privately owned (HEICO, HEI on NYSE)
- Locations: Buc, France
  McKinney, TX, USA
  Fremont, CA, USA

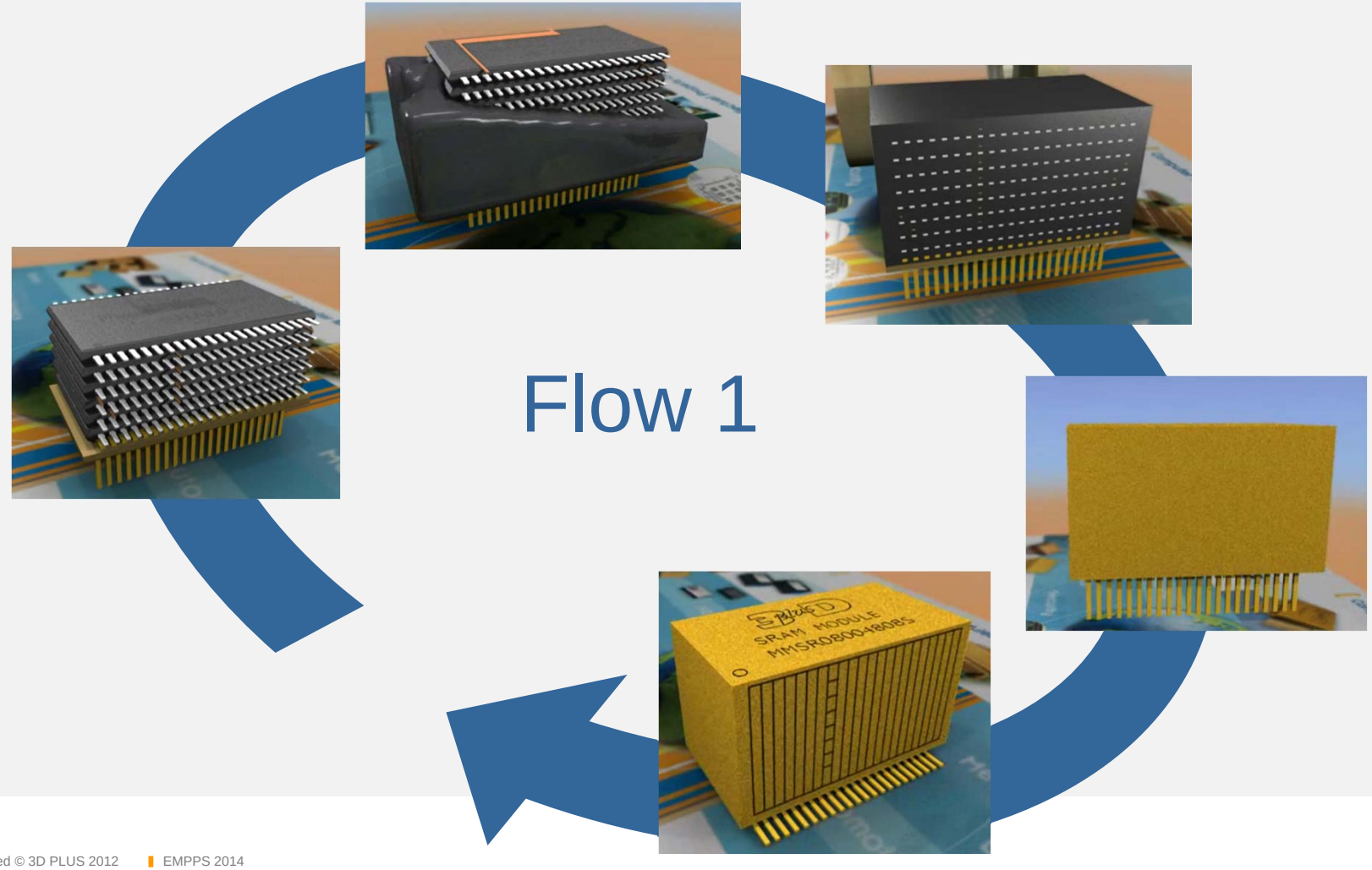
Headquarters
BUC, France

Marketing & Sales USA
MC Kinney, TX, USA

Tech. Center USA
Fremont, CA, USA

- People: 128 employees (+14 % in 12 months)
- Developer of advanced high density 3D package and die stacking technology
- Designer of Space Radiation Hardened electronics
- Manufacturer of 3D standard products and System in Package for high reliability and high performance product applications
- ISO-9001:2008 certified
- NASA, JPL, ESA, CNES qualified manufacturing line for Space Applications
- Largest Space Qualified MCM Manufacturer located in Europe (ITAR FREE)
- Flight proven with more than 70.000 modules in space beginning of 2013
- Supplier of Major Aerospace Prime Contractors worldwide

- 3D-Plus is leader in space/defense 3D stacking



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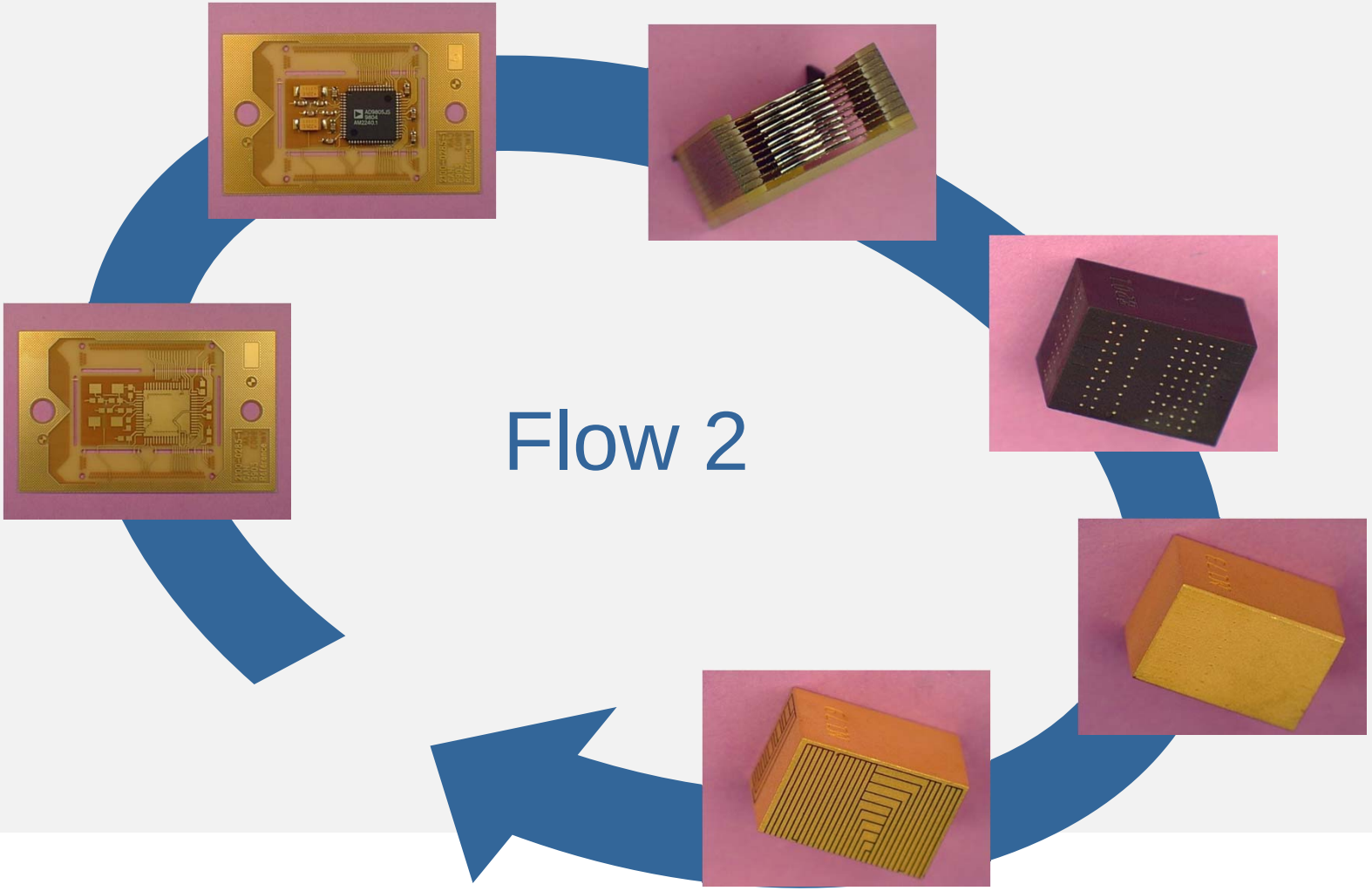

- Flow 1 and flow 2 are fully qualified for space applications
- A disruptive technology is a must for long term challenges
- First introduction in markets such as
  - Medical applications
  - Industrial applications
- Availability in the near future for space applications

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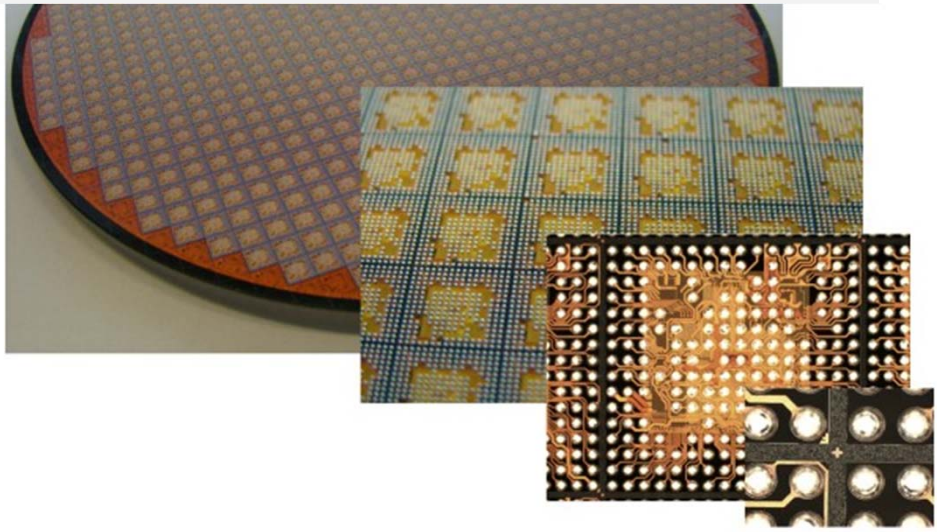
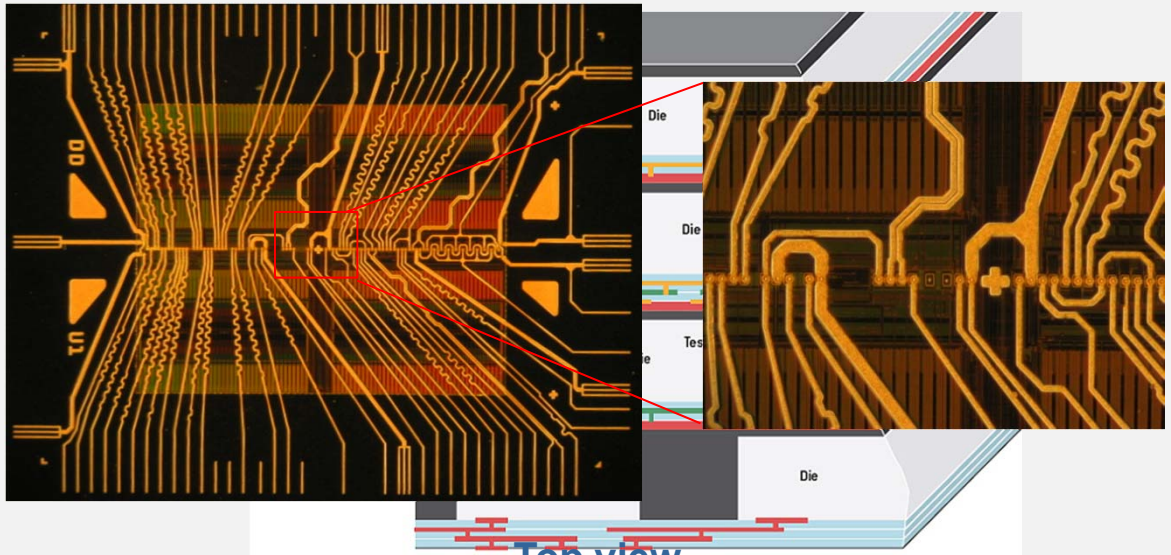
WDoD technology: Flow 3



- 3D stacking patented by 3D PLUS
- e-WLB/RCP based 2D technology
- Polymer Stacking
- Layer thicknesses down to 200 µm thick
- Multi chips per level
- Mixed with PCBA when components not available at die level
- Materials can be selected according to product specifications (low alpha emissions and RoHS materials)

Wire free Die on Die technology



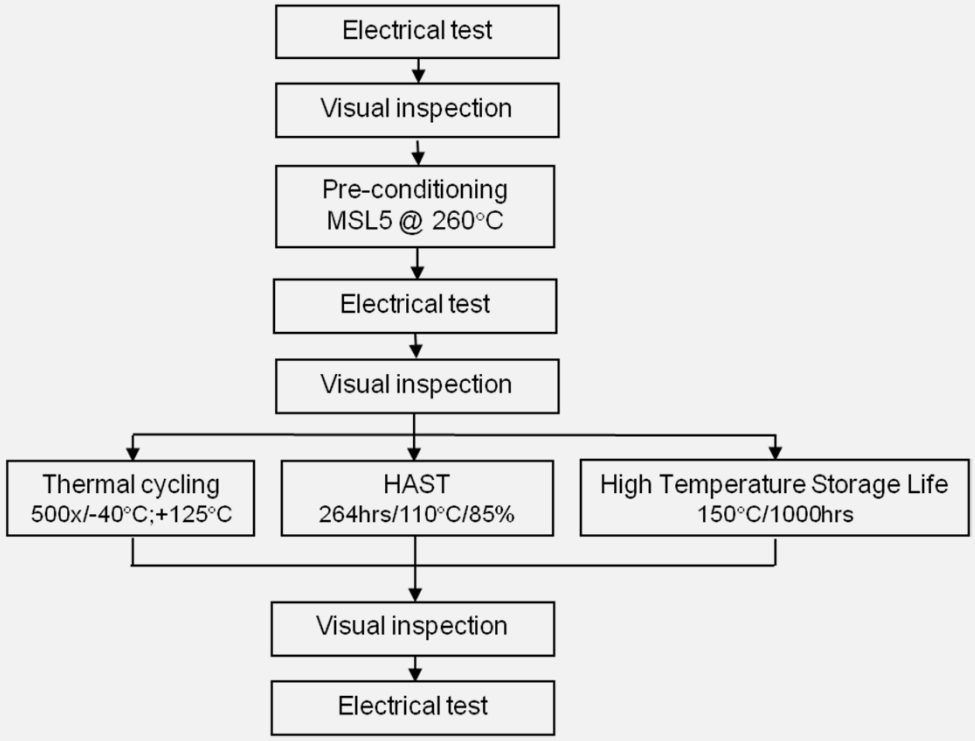
Top view

RDL

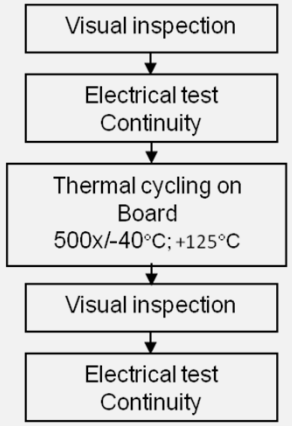
Cross section

Huge shrinkage allowing small form factor components

Evaluation flow



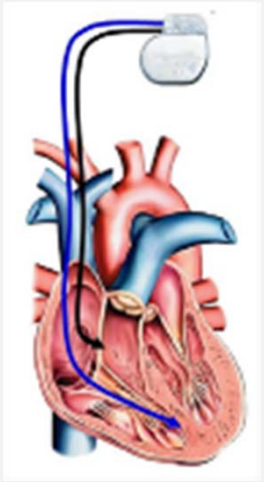
Package Level



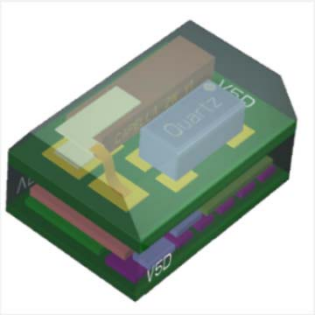
Module Level

Medical application (SORIN GROUP)

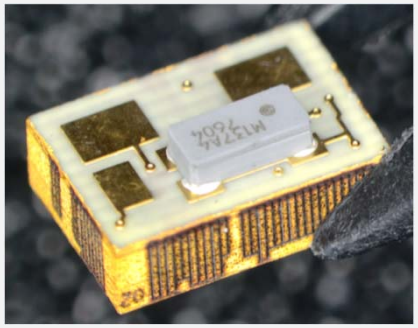
Implanted leadless pacemaker



16x shrinkage



a)



b)

- 2.3 x 5.2 x 7.3 mm^3
- Volume is less than 1 cm^3

- Bus metal laser pitch is 250 µm
- ASICs and silicon based capacitors
- SMD components

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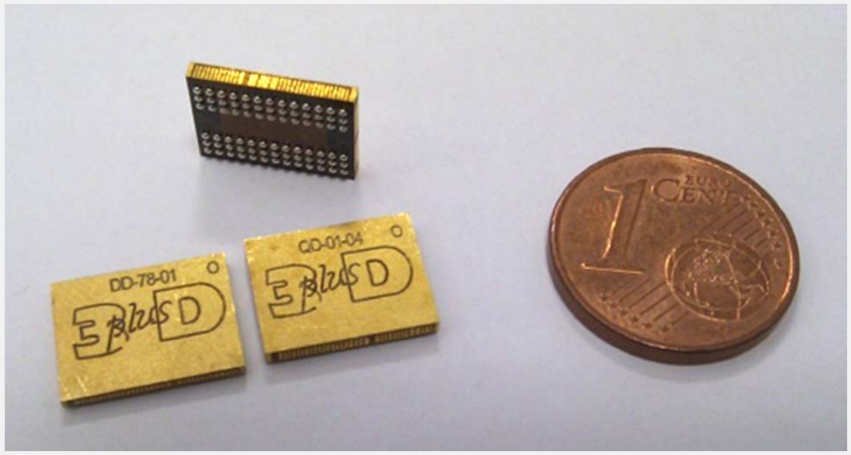
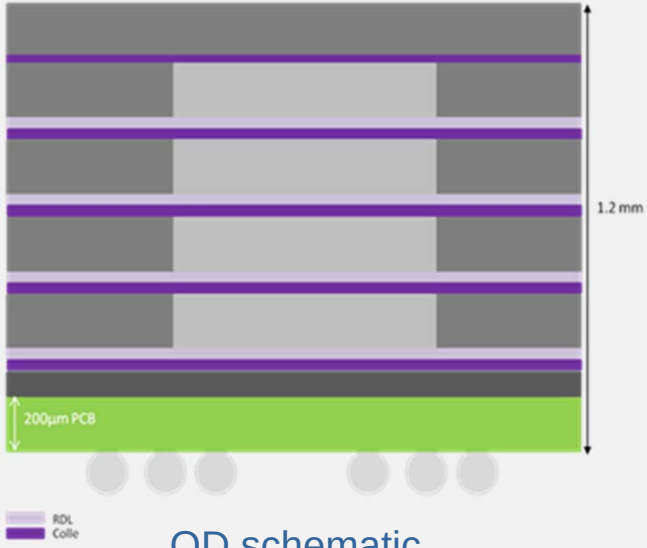
High performance memory

- Memory units:
  - Dual Die DDR3 (2Gb 8x)
  - Quad Die DDR3 (4Gb 8x)

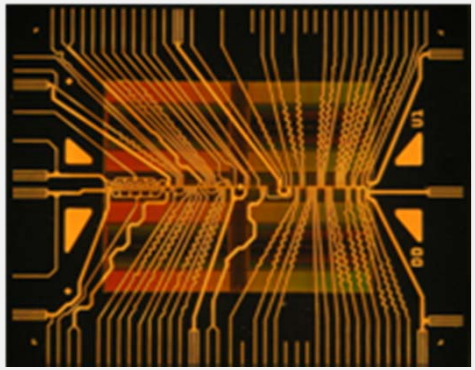


- Specifications
  - Balling JEDEC compatible
  - Working frequencies: 533 and 667 MHz
  - Dual Die: 8.5x11x1.2 mm
  - Quad Die: 8.5x11x1.6 mm
  - Each level: 200 µm thick
  - Average pitch at the edge: 250 µm
  - Lead free

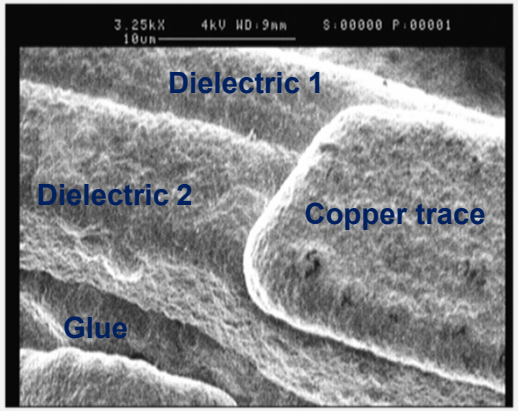
High performance memory stacking



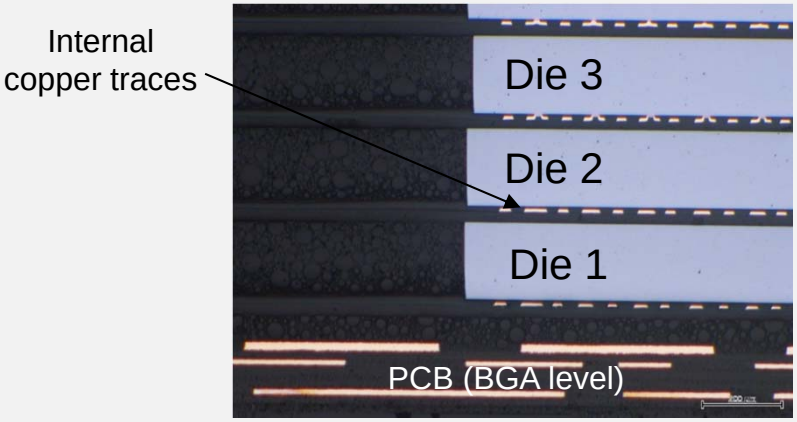
QD schematic



Internal RDL based level



Side view of the bus metal



QD cross section

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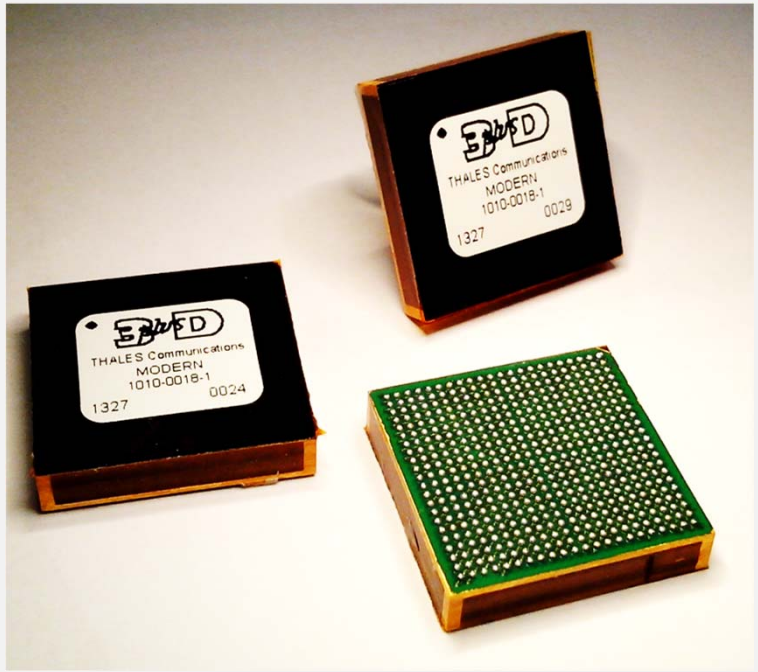
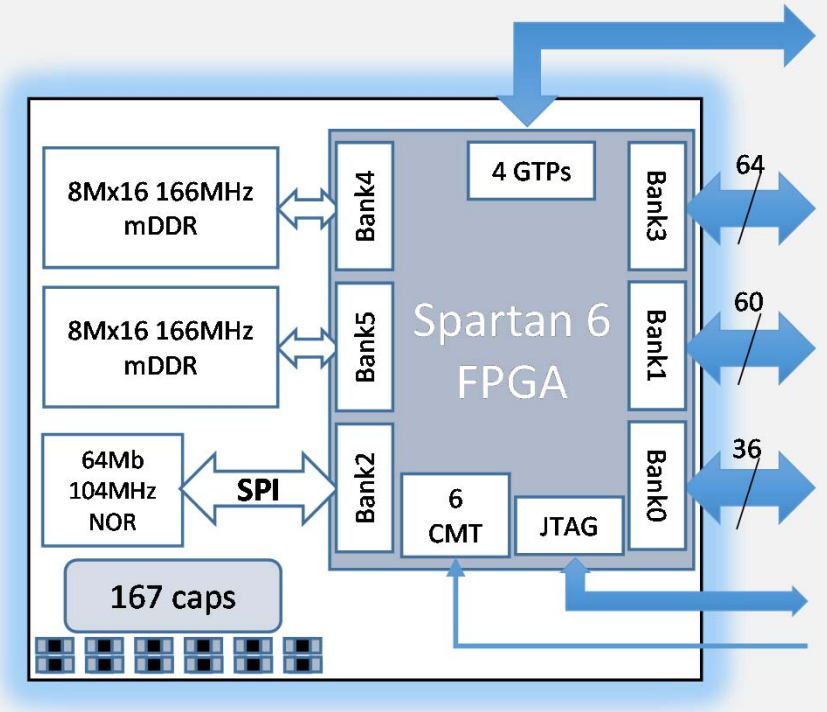


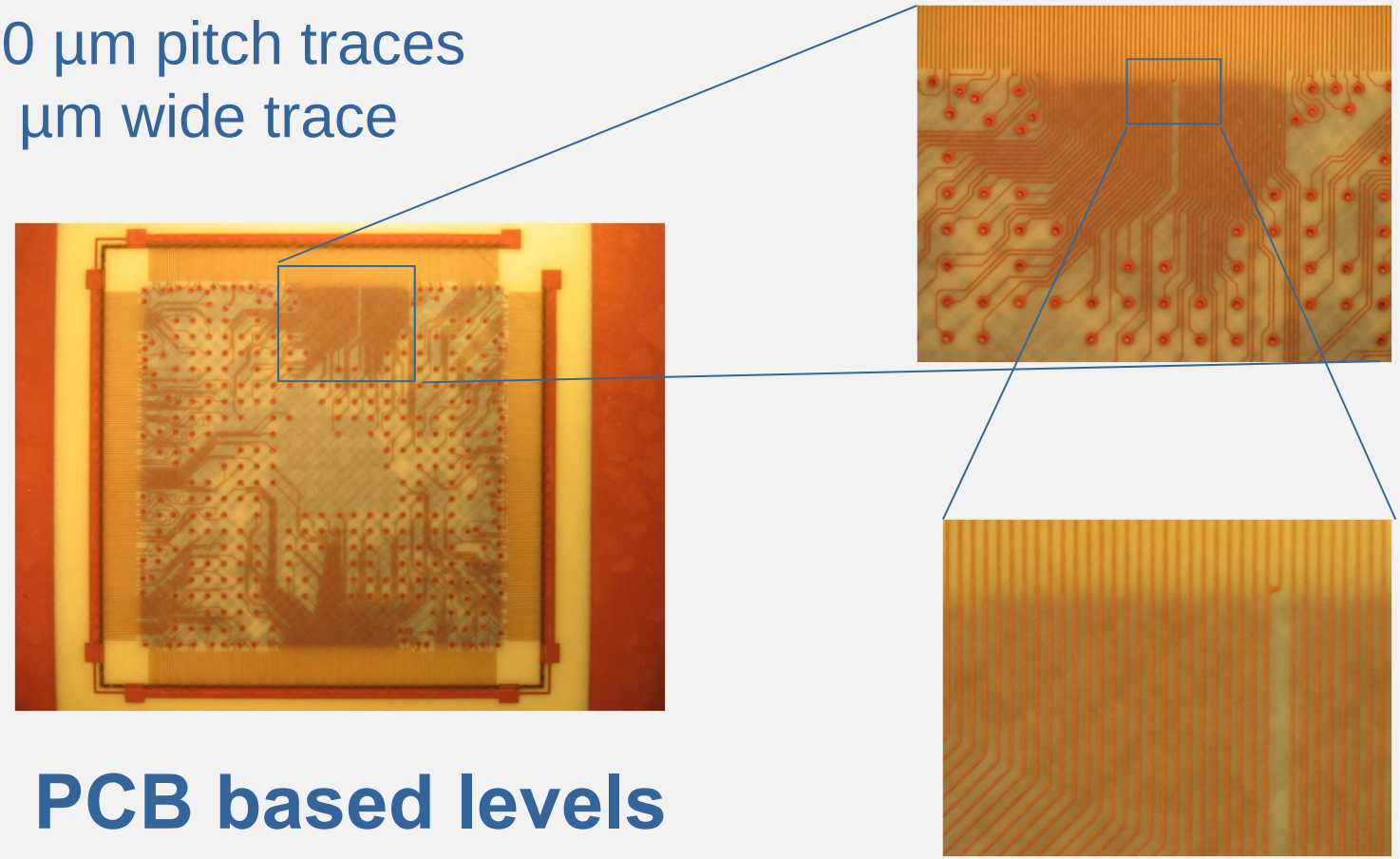
FUSIO-II module

Same footprint as a single SPARTAN 6 CSG484

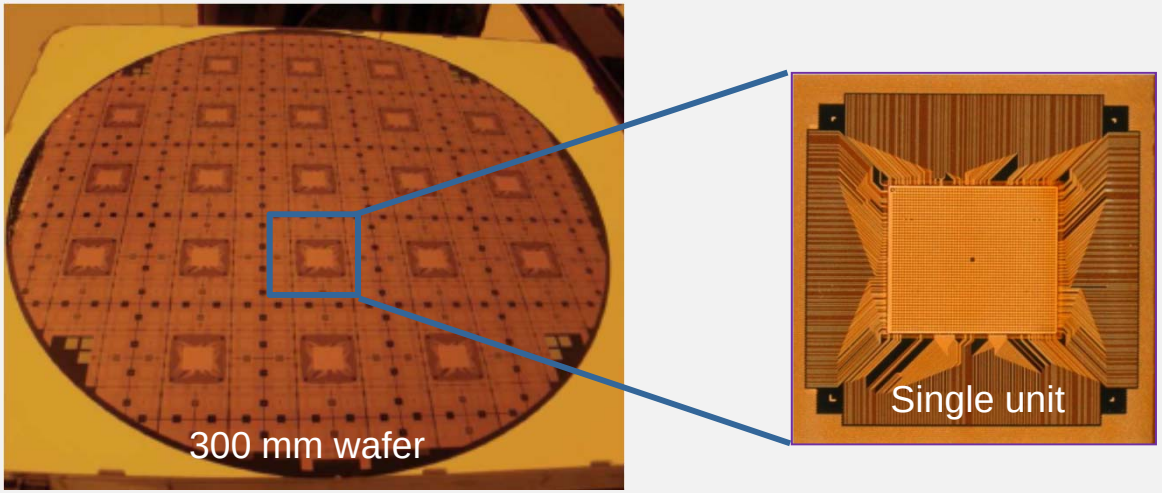


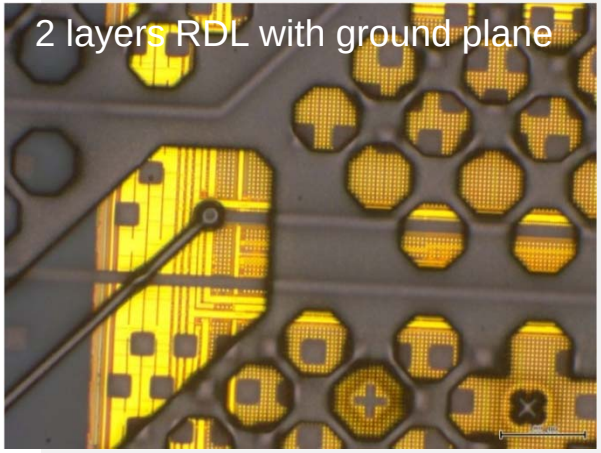
System block diagram

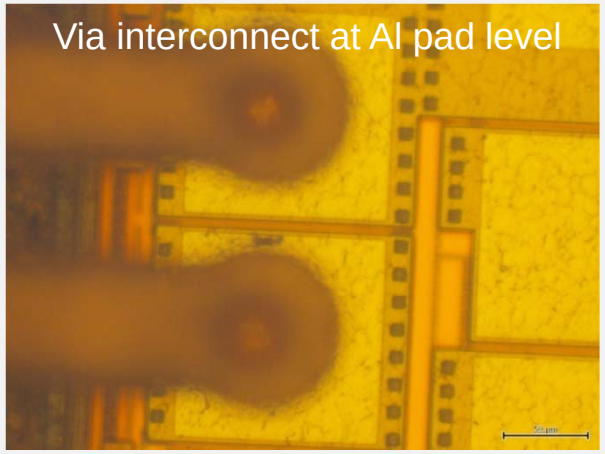
- 8 layers PCB
- µ vias
- 100 µm pitch traces
- 30 µm wide trace

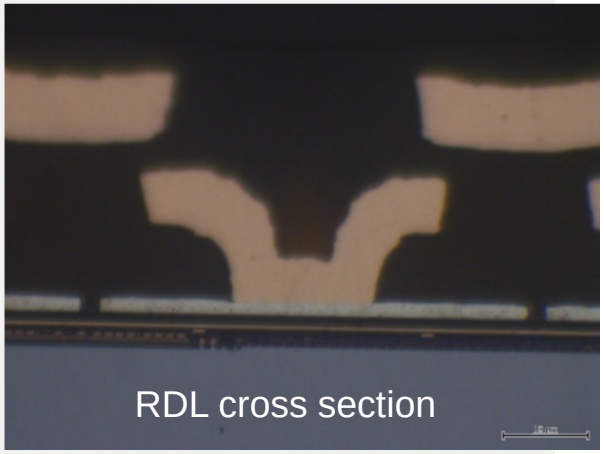


PCB based levels

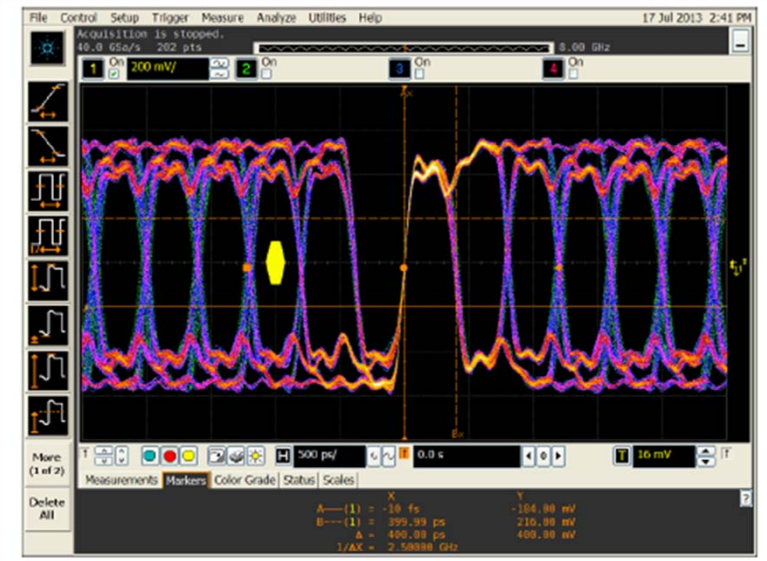






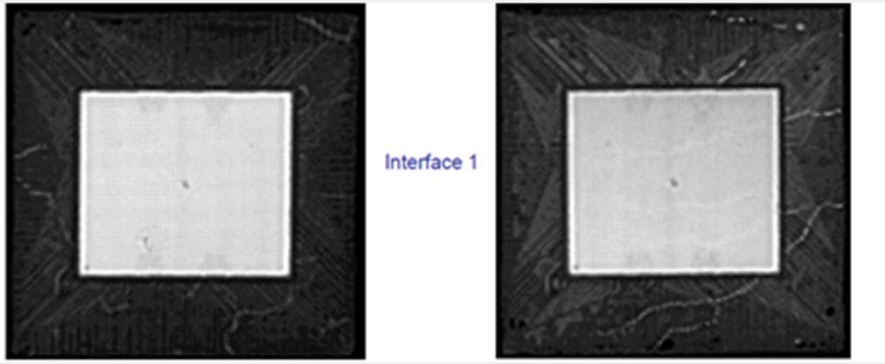


RDL based levels



Eye diagram

Very good electrical performance



CSAM analysis

No issue after first reliability screening

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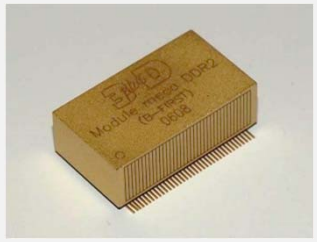
- 3D-PLUS is offering a new 3D integration technology for commercial and industrial applications with:
  - High miniaturization
  - High electrical performance (short interconnect – low parasitic elements – embedded decoupling capacitors)

- In the near future, space application requiring high numbers of I/Os in a small form factor product could be fulfilled with this new technology

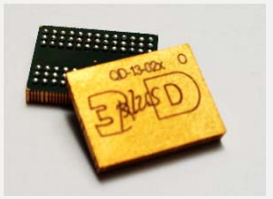
Space QD DDR



TRL 9

Weight saving
25x

WDoD based QD DDR



TRL 4 → 5

Acknowledgements

- ESIP (ENIAC European project)
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Thanks for your attention

www.3d-plus.com

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