4th QCA Presentation Day
SRAM construction analysis
Wo05 Co15

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DTE Group specialisation….

■ **Intellectual Property investigation**:
Patent infringement analysis, patent portfolio management, market analysis & prior art investigation.

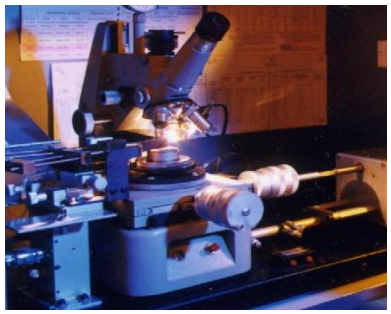
■ **Design & technology assessment.** *Design & process extraction for performance simulation, quality checks & competitive analysis.*

■ **Electrical design evaluation & diagnostic measurements.**

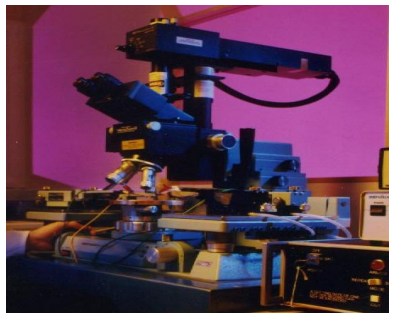
■ **IC & 'smart card' security assessment.**

■ **Process measurements & failure analysis.**

■ **Consultancy & training in measurement & analysis.**



Doping profiling



Precision Micro-probing

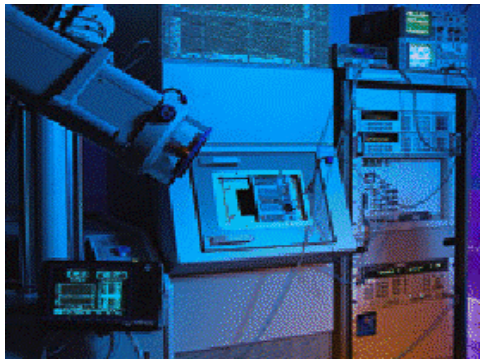
Mixed Signal IC Characterisation

Design & Technology Assessment

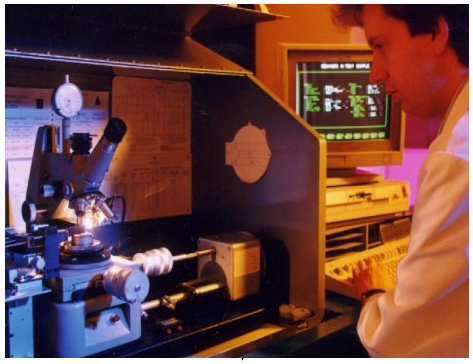
Circuit

Process

Electrical



- Extract circuit design
- Geometries (Horizontal)
- Layout issues
- Simulation (verify ccty).



- Process description
- Geometries (Vertical)
- Materials used
- Doping profiles

- Specification checks
- Non specified data
- Application specific

Main techniques used:

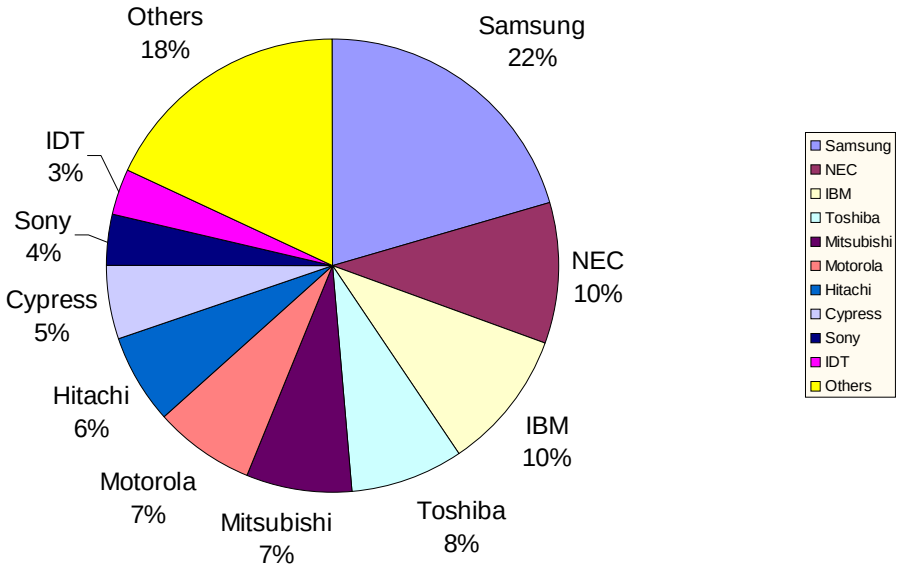
Microprobing, delayering, imaging, cross-sectioning, SEM, TEM, EDX, SRP, EM, SIMS, Electrical Characterisation, . . .

Scope of work

- Extraction of SRAM memory cell process technology and sizes for radiation study

- Nine 1Mbit SRAMs from 3 manufacturers
- Mitsubishi (x3)
- Cypress (x2)
- Samsung (x4)

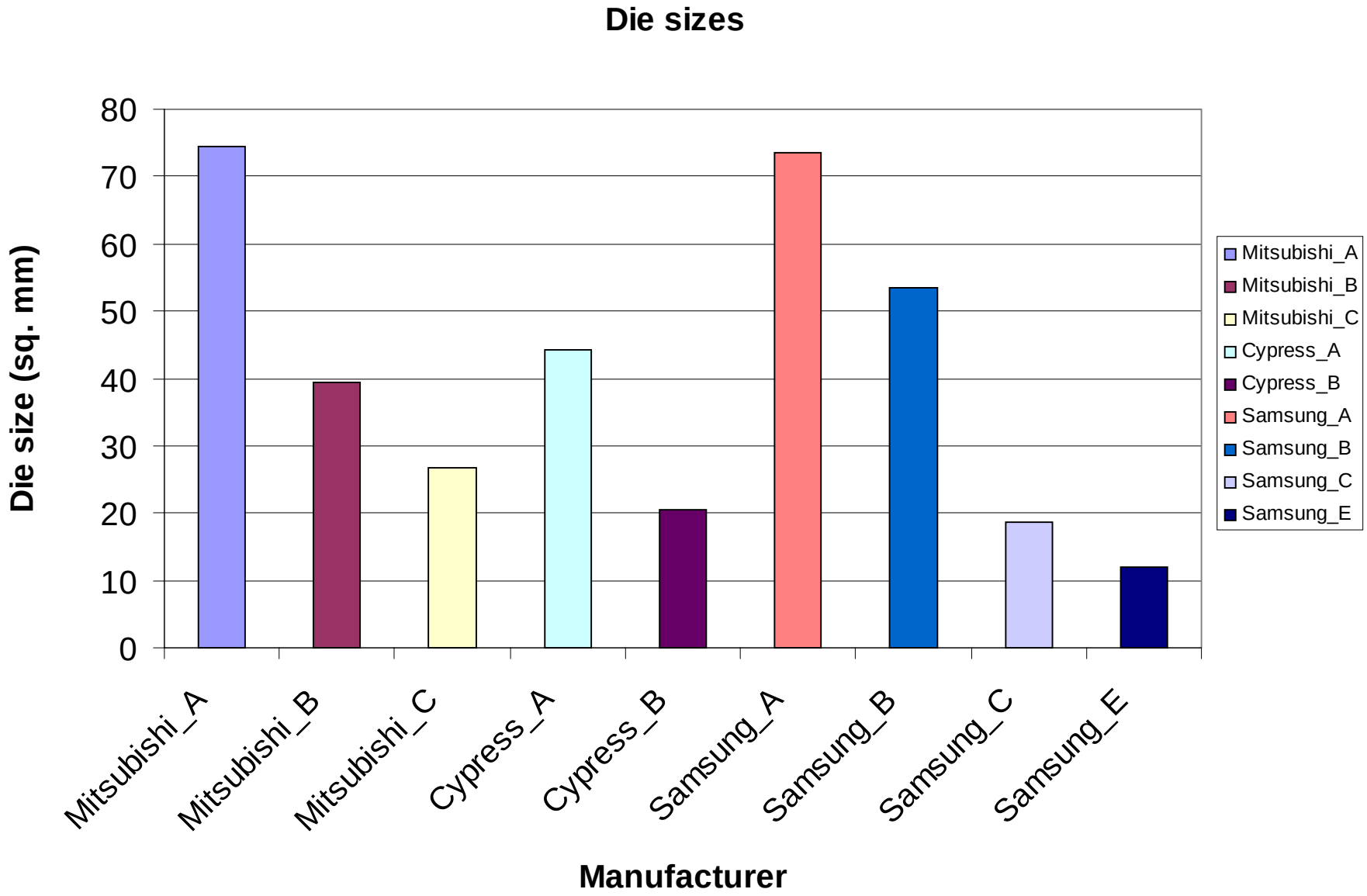
SRAM market share 1998: total US$3.648billion

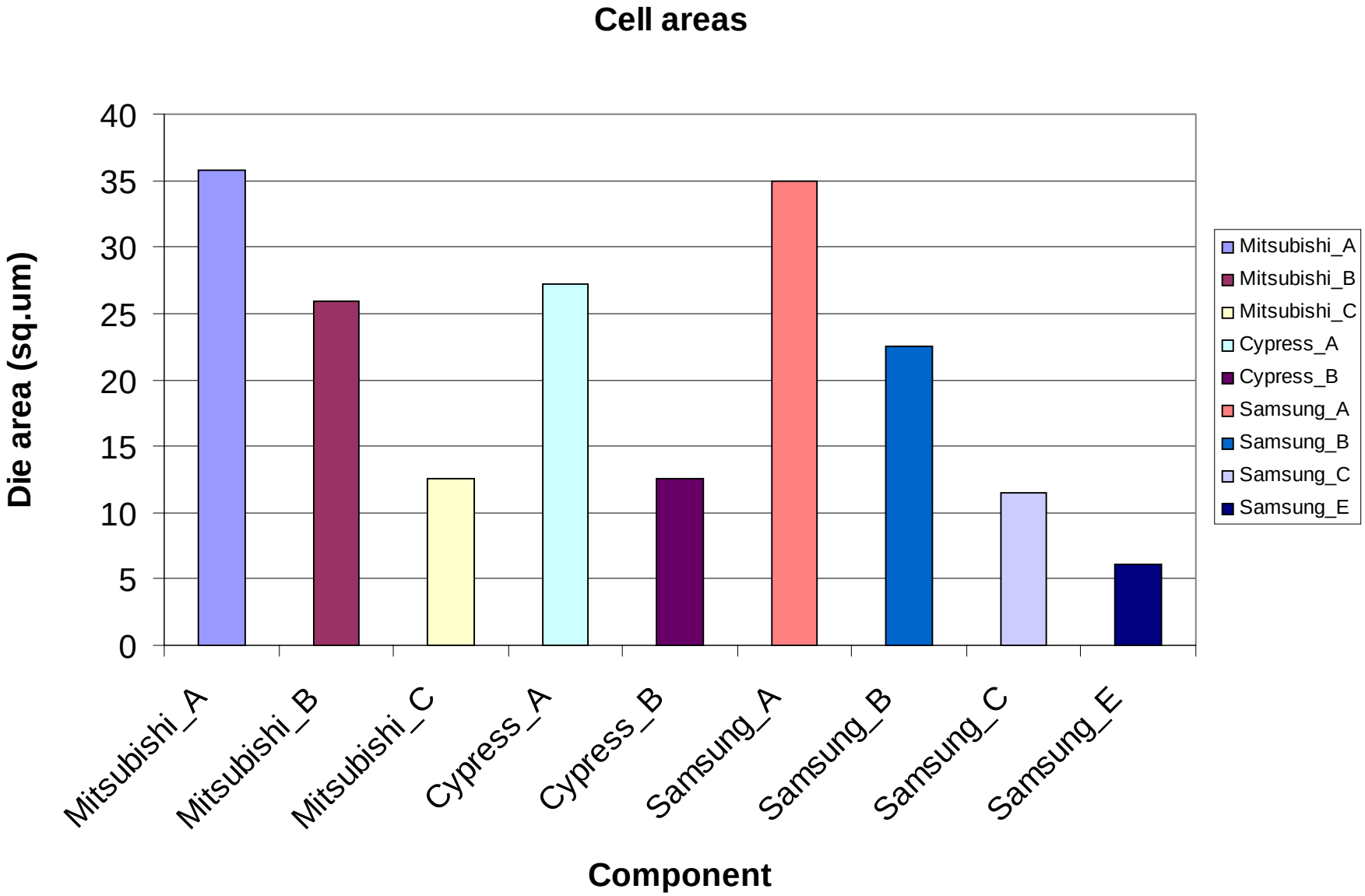


Manufacturer	Part	Feature size	Metal	Poly	Cell	Die area	Cell area
Mitsubishi	M5M5100AVP	0.6μm	1	3	High R	74.5mm^2	35.8μm^2
	M5M5100BFP	0.6μm	1	3	High R	39.4mm^2	25.9μm^2
	M5M5100CFP	0.35μm	2	4	TFT	26.8mm^2	12.6μm^2
Cypress	CYC10920VC	0.8μm	2	2	High R	44.3mm^2	27.2μm^2
	CYC10925VC	0.35μm	3	1	6T	20.6mm^2	12.5μm^2
Samsung	KM6810000ALG	0.8μm	1	3	High R	73.6mm^2	34.9μm^2
	KM6810000BLG	0.5μm	1	3	High R	53.5mm^2	22.5μm^2
	KM6810000CLP	0.45μm	1	4	TFT	18.6mm^2	11.5μm^2
	KM6810000ELT	0.3μm	2	3	TFT	12.0mm^2	6.14μm^2

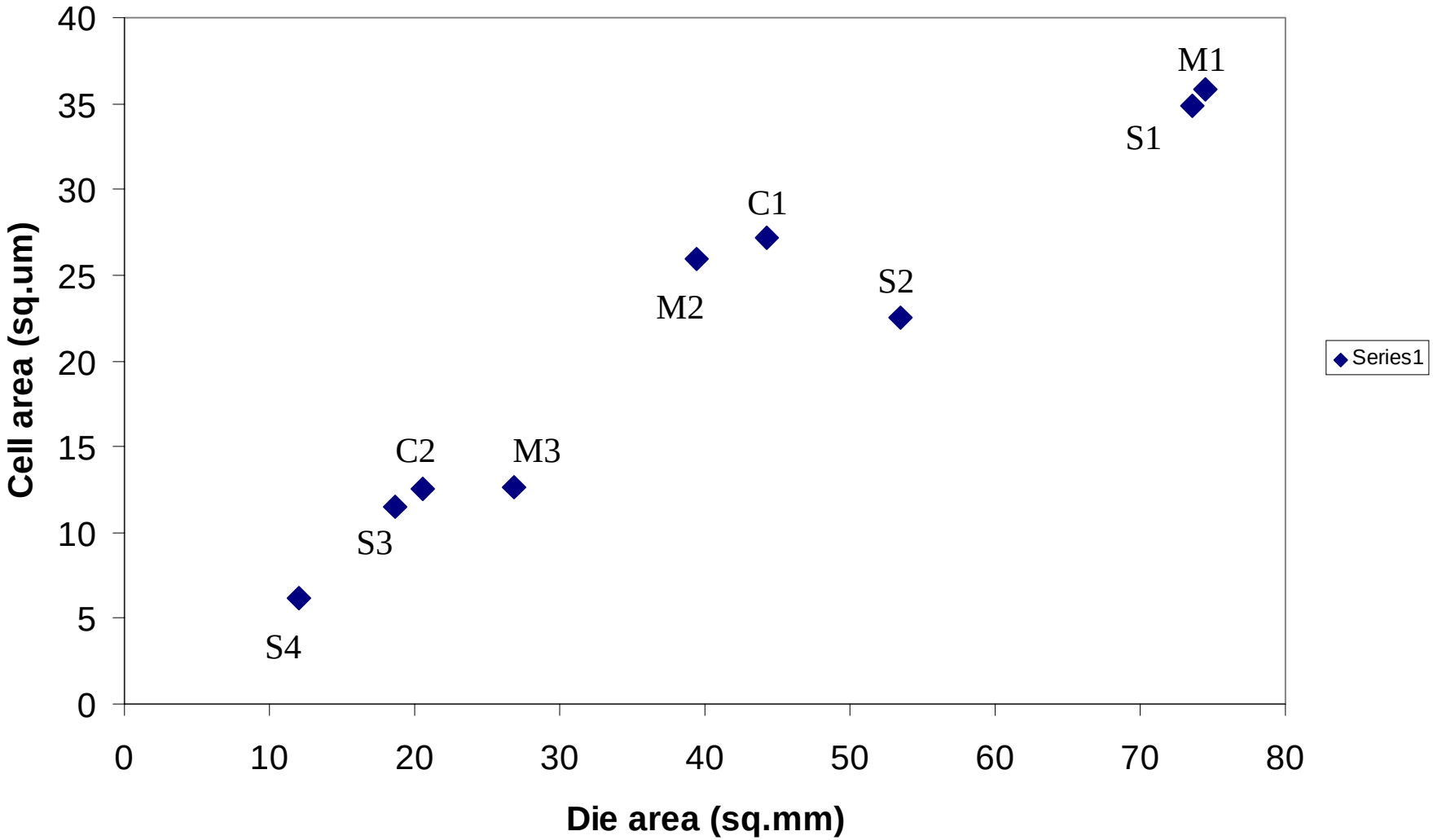
Note: feature size based on minimum polysilicon linewidth

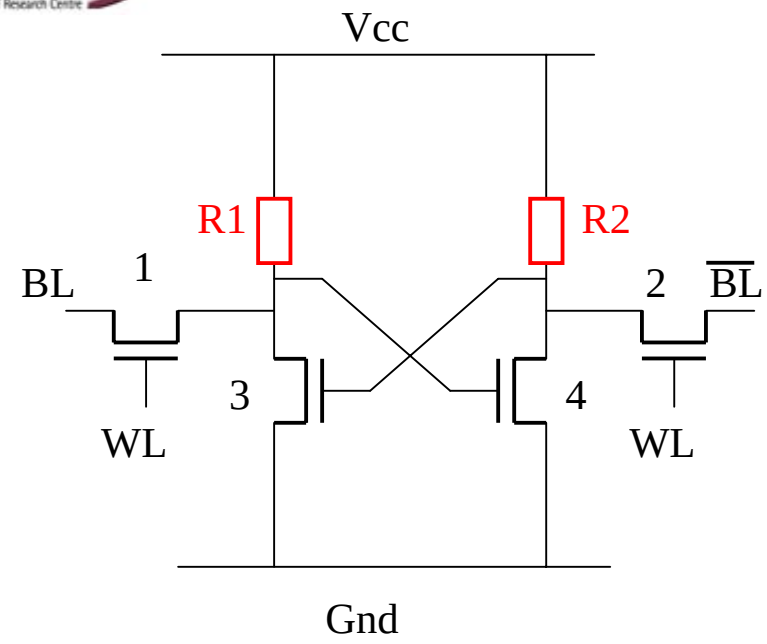
SRAM technology and size summary


Die sizes
Die size (sq. mm)
80
70
60
50
40
30
20
10
0
Mitsubishi_A
Mitsubishi_B
Mitsubishi_C
Cypress_A
Cypress_B
Samsung_A
Samsung_B
Samsung_C
Samsung_E
Manufacturer

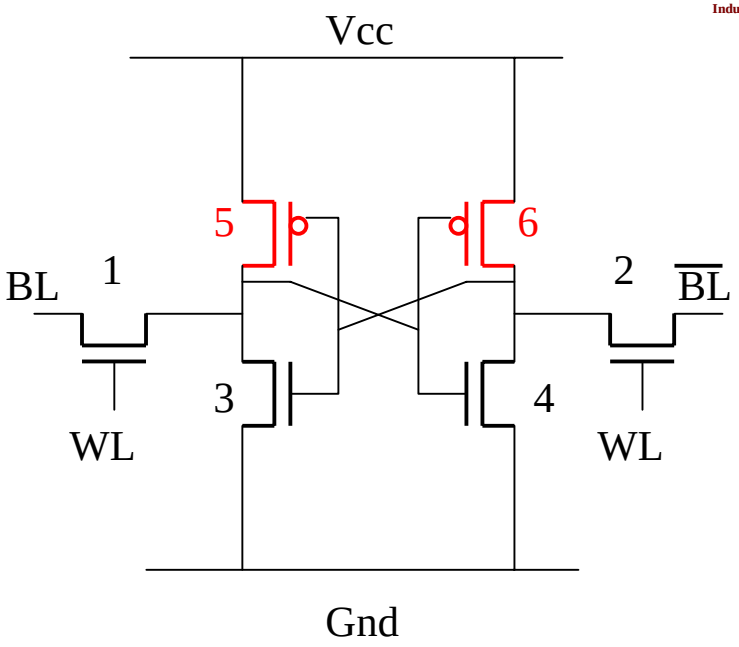

Cell areas
Die area (sq.um)
40
35
30
25
20
15
10
5
0
Mitsubishi_A
Mitsubishi_B
Mitsubishi_C
Cypress_A
Cypress_B
Samsung_A
Samsung_B
Samsung_C
Samsung_E
Component

Cell area vs. die size





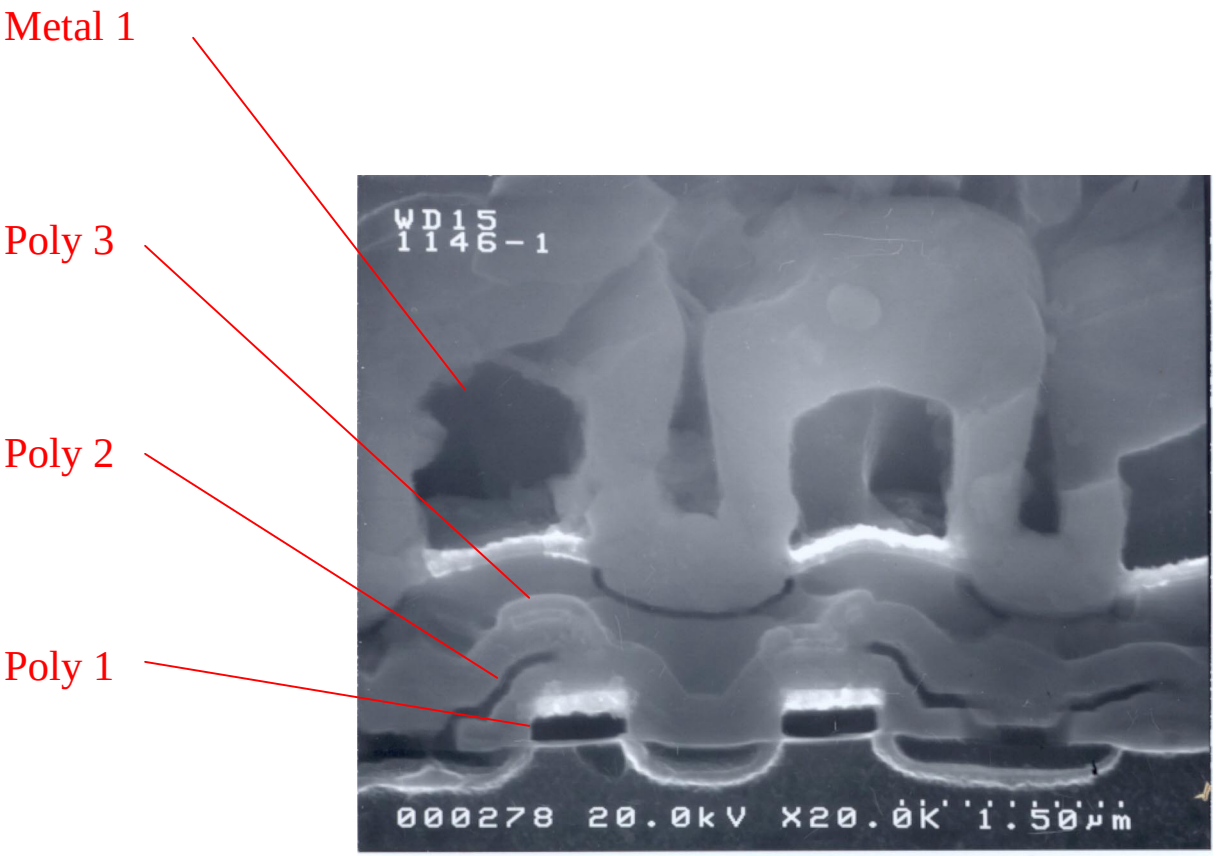
High resistance cell



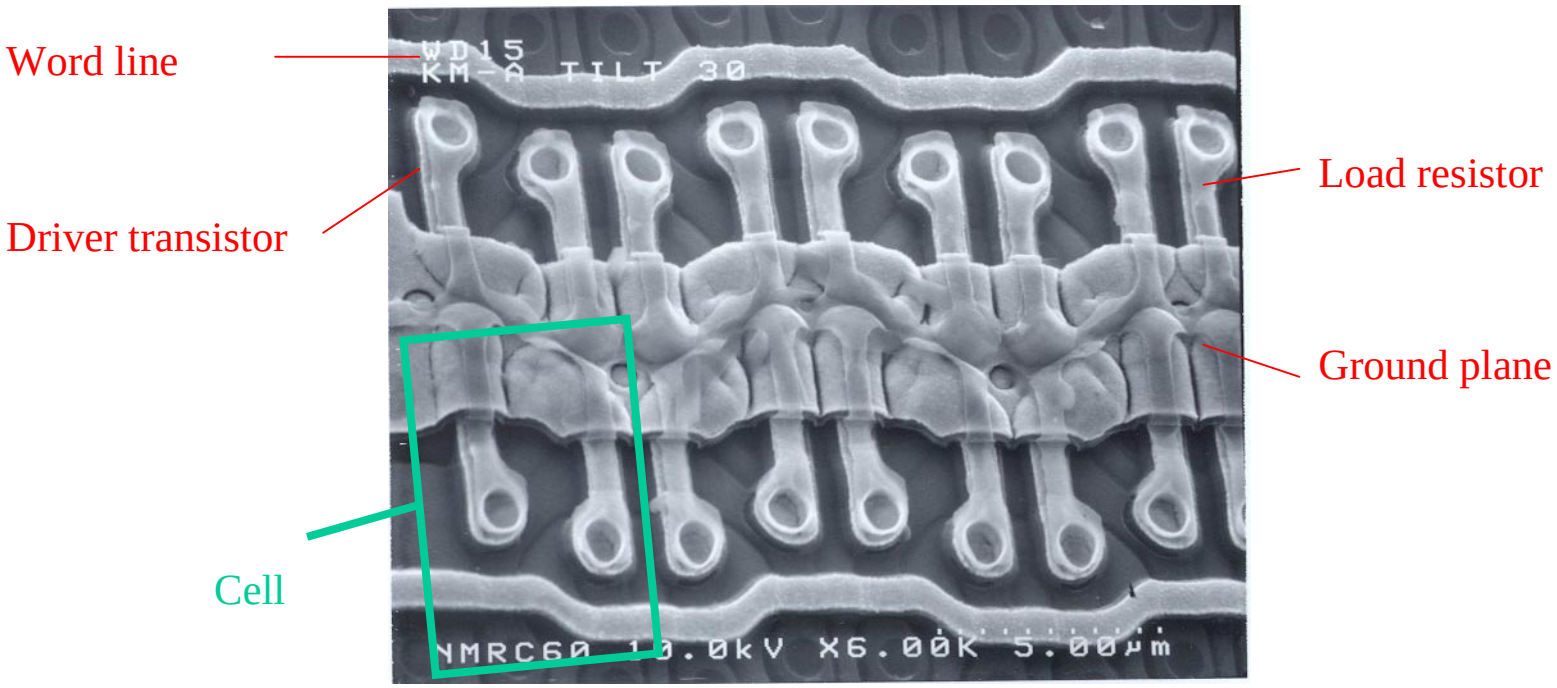
CMOS 6T cell

TFT cell

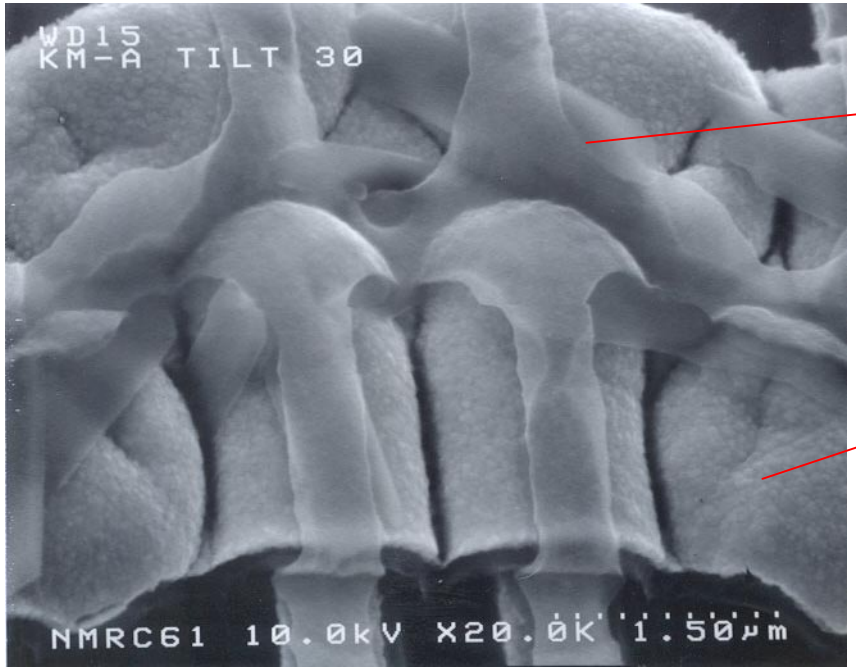
SRAM cell electrical schematic diagrams



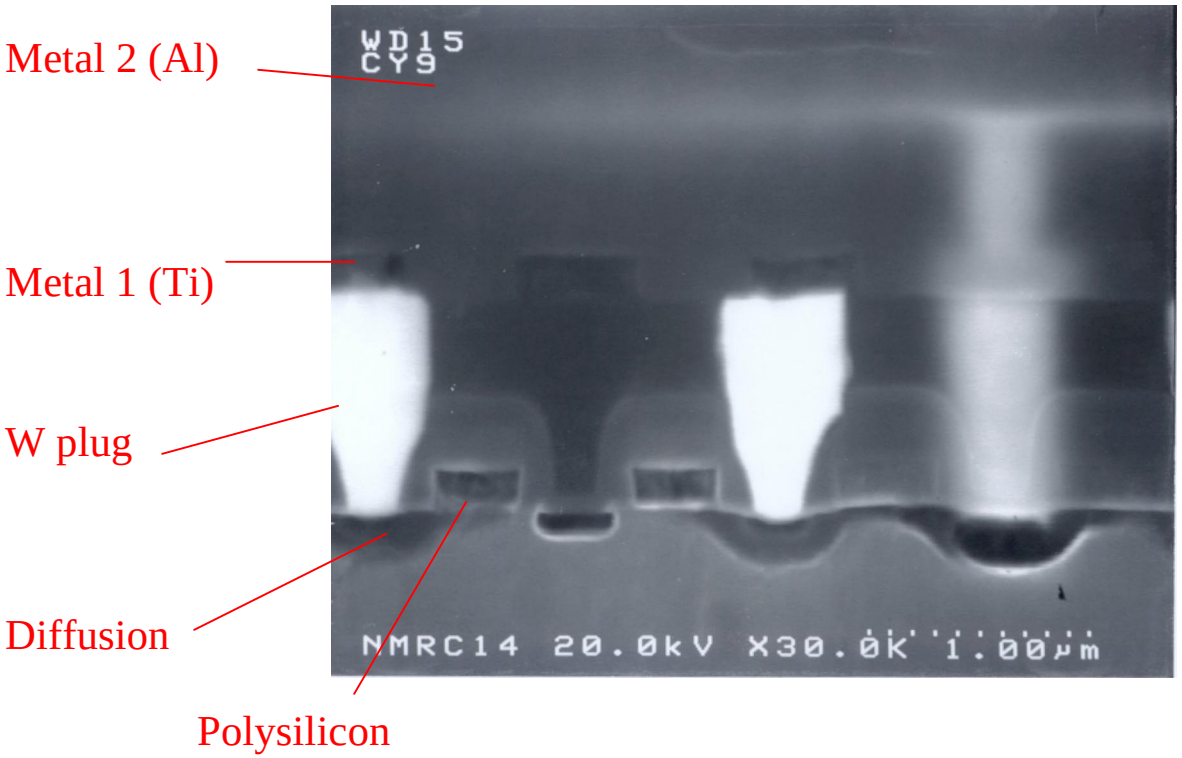
SEM cross-section:High R: Mitsubishi M5M51008AVP



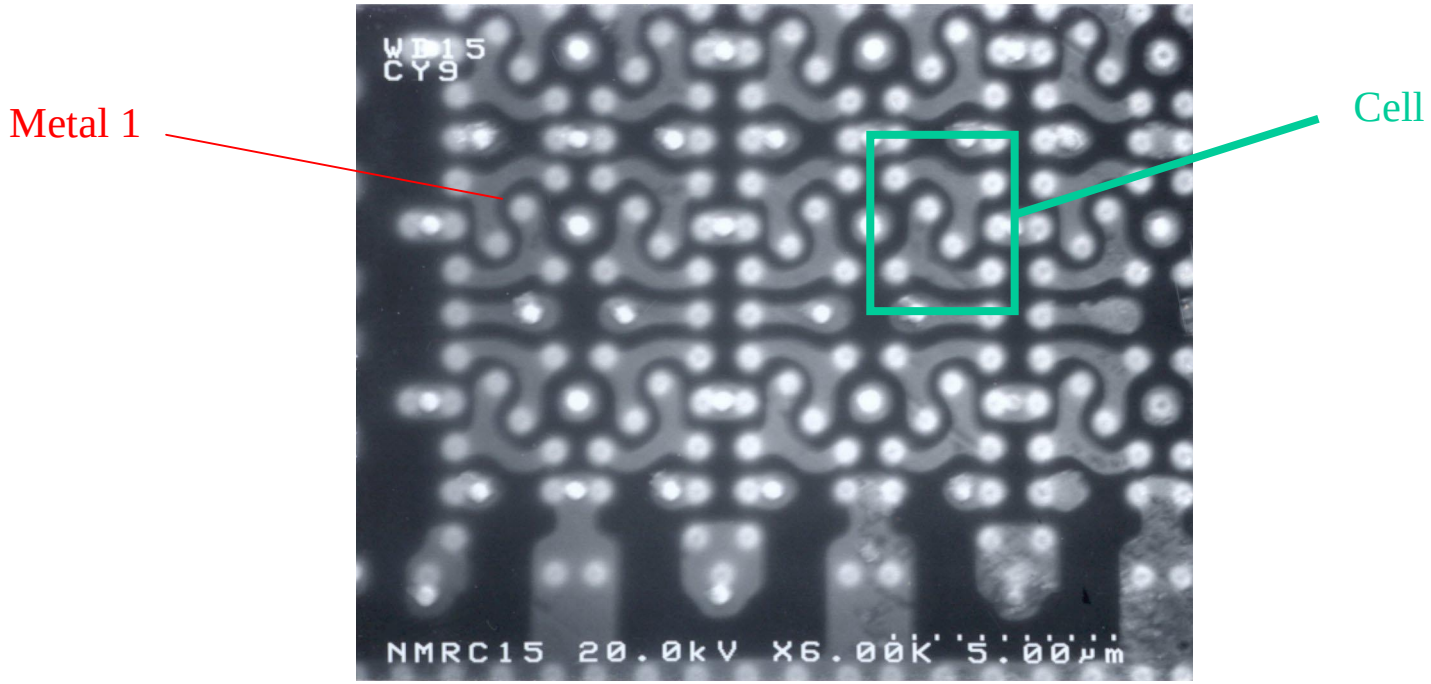
SEM delayered cell: High R: Samsung KM68100ALG



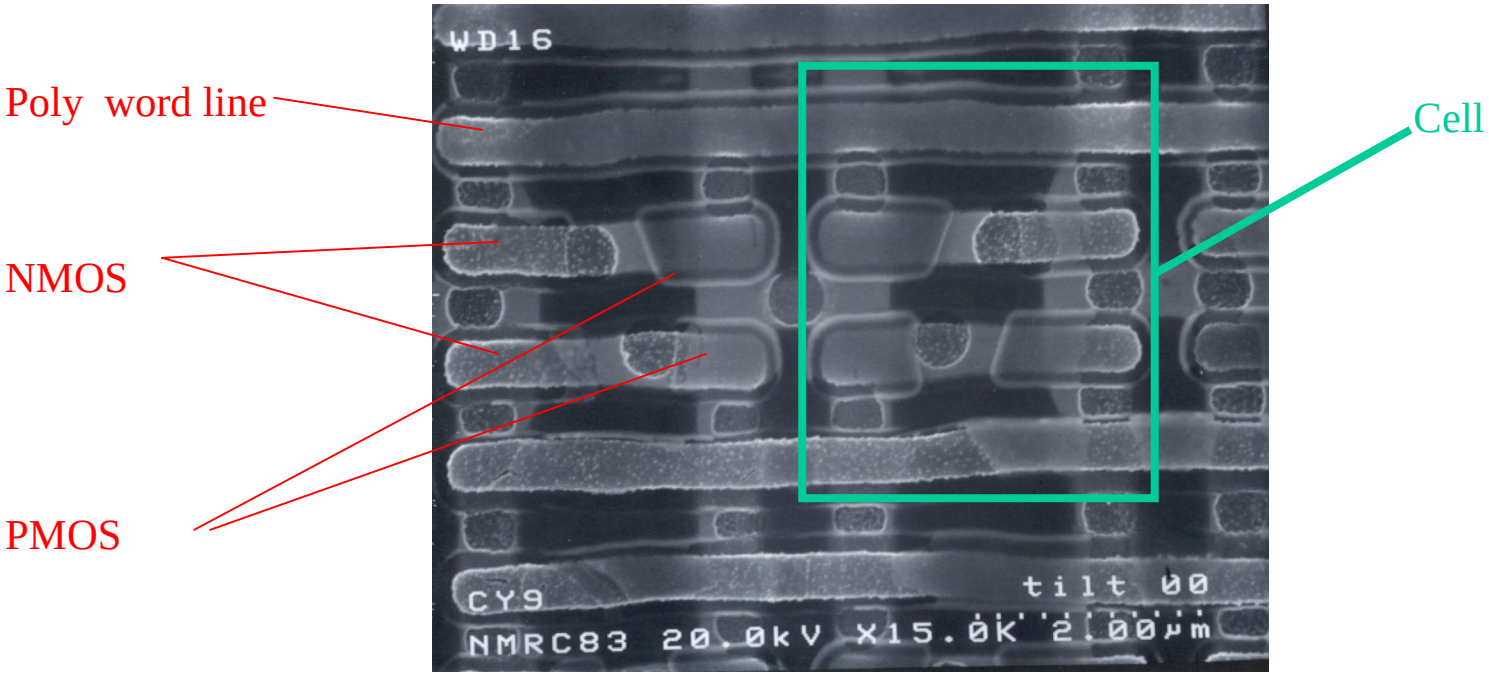
SEM delayered cell: High R: Samsung KM68100ALG



SEM cross-section:6T cell: Cypress CYC109-25VC



SEM delayered cell: 6T : Cypress CYC109-25VC



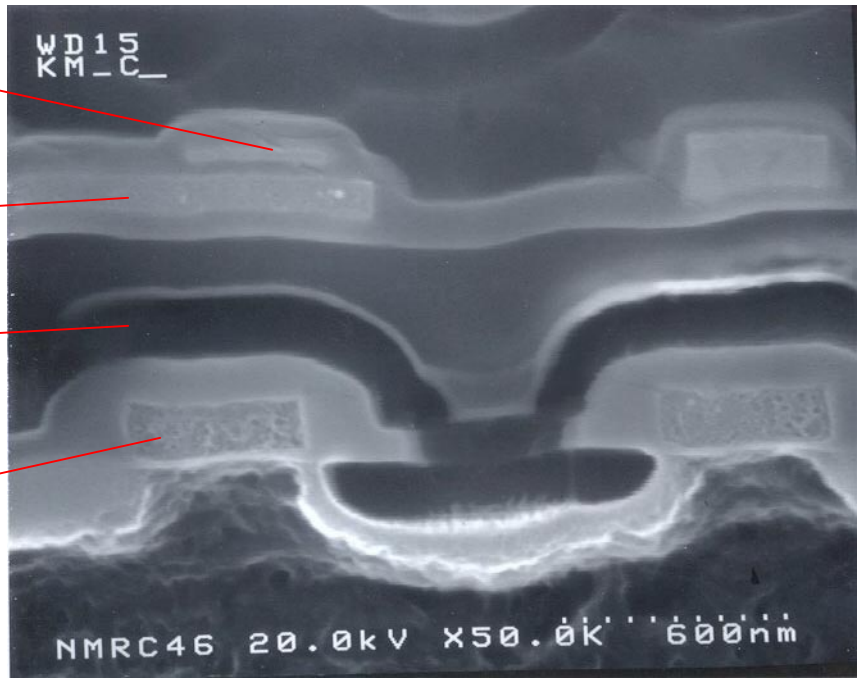
SEM delayered cell: 6T : Cypress CYC109-25VC

Poly 4: TFT active

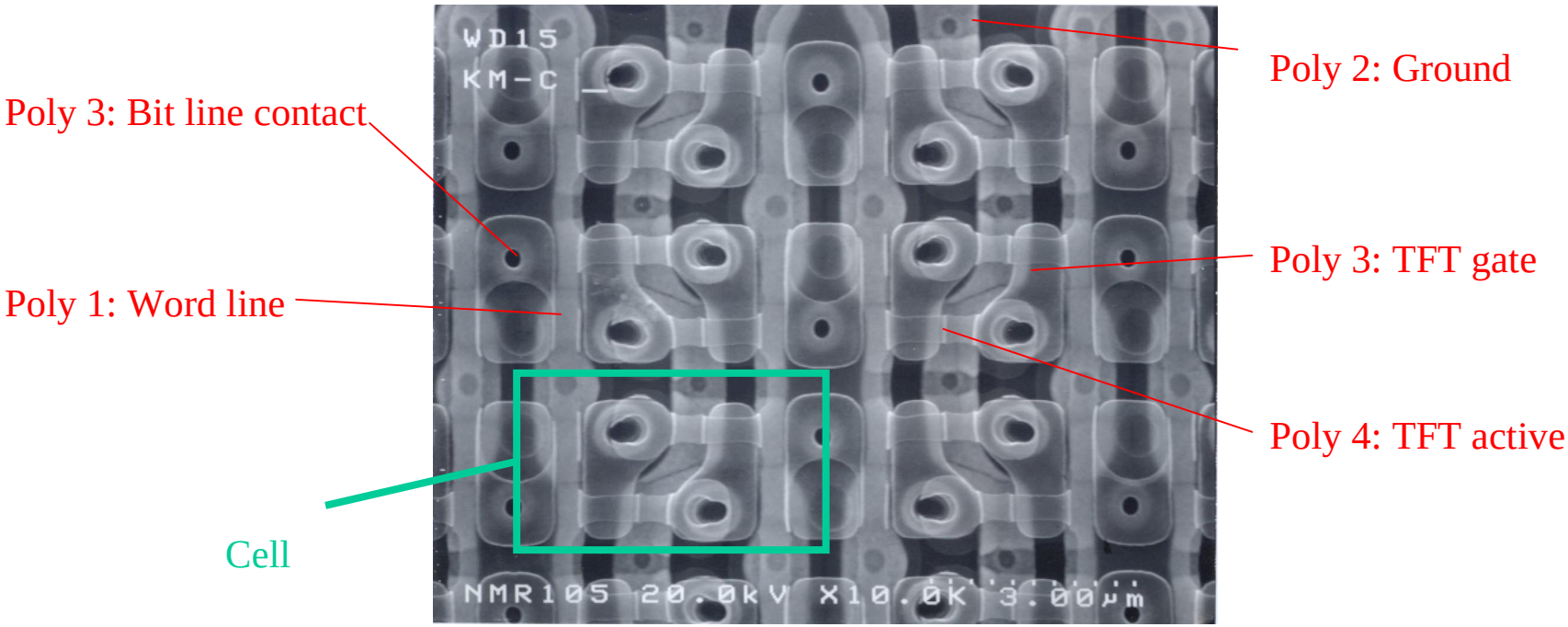
Poly 3: TFT gate

Poly 2: Ground

Poly 1: Word line



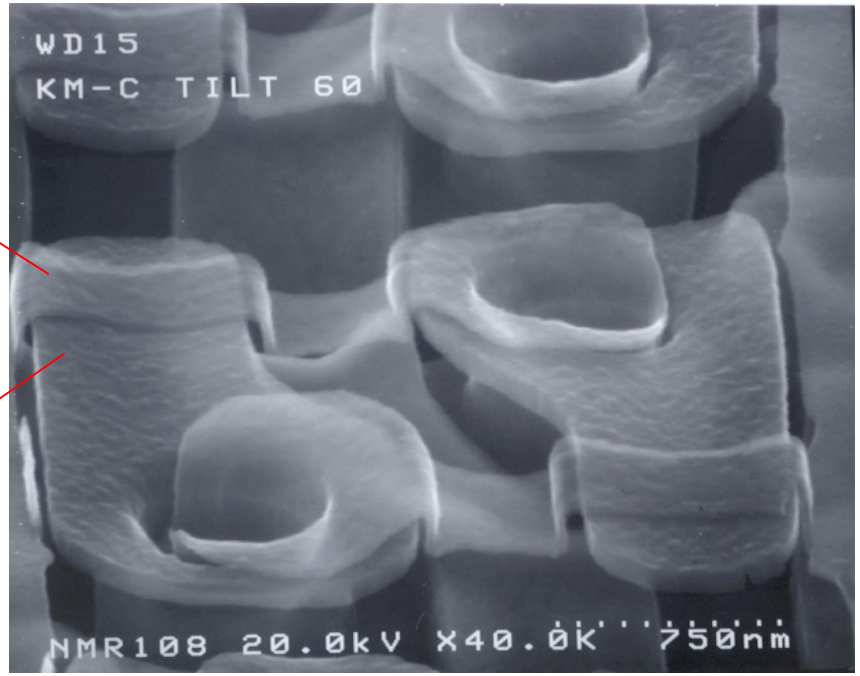
SEM cross-section: TFT cell: Samsung KM681000CLP-7L



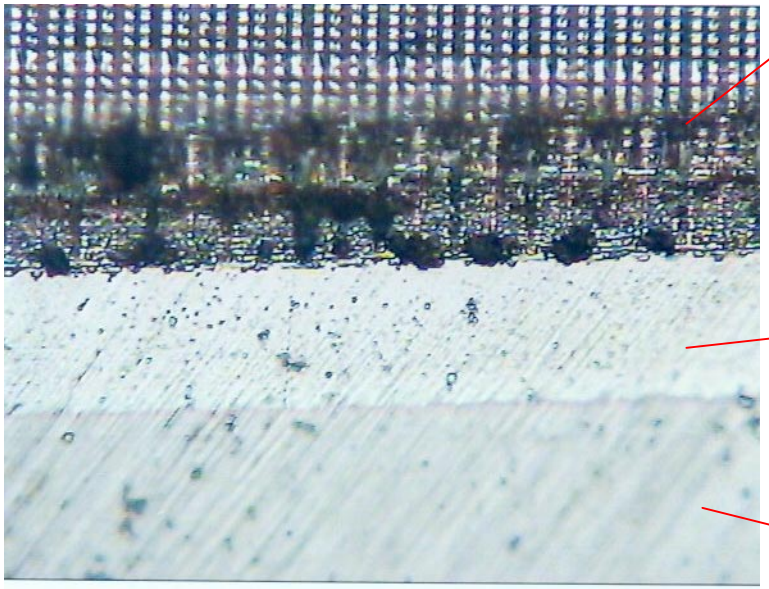
SEM delayered cell: TFT: Samsung KM68100CLP

Poly 4: TFT active

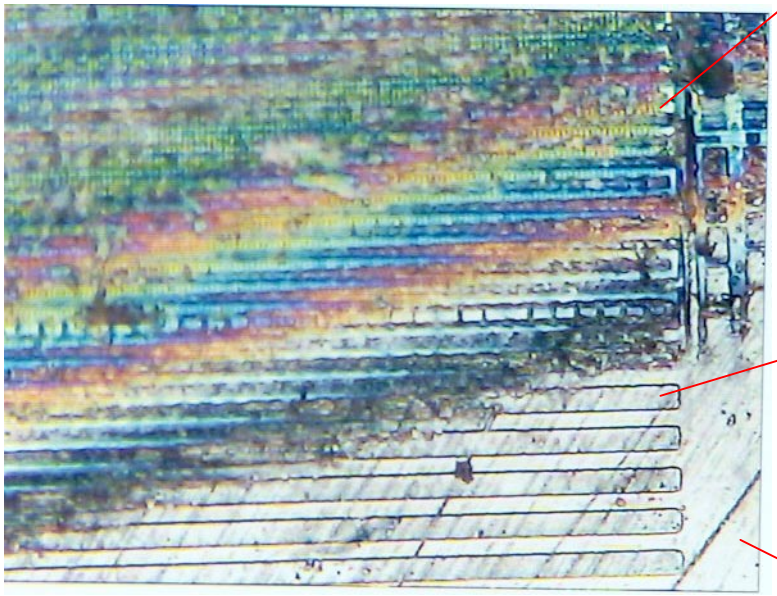
Poly 3: TFT gate



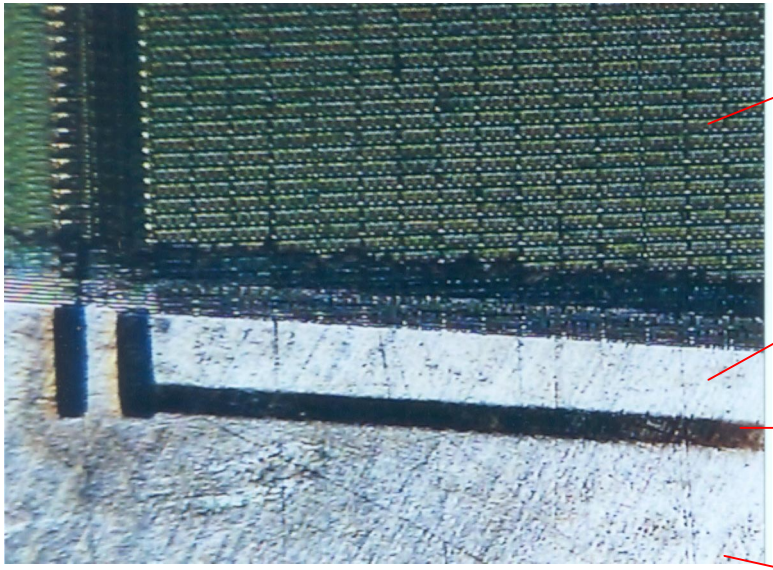
SEM delayered cell: TFT: Samsung KM68100CLP



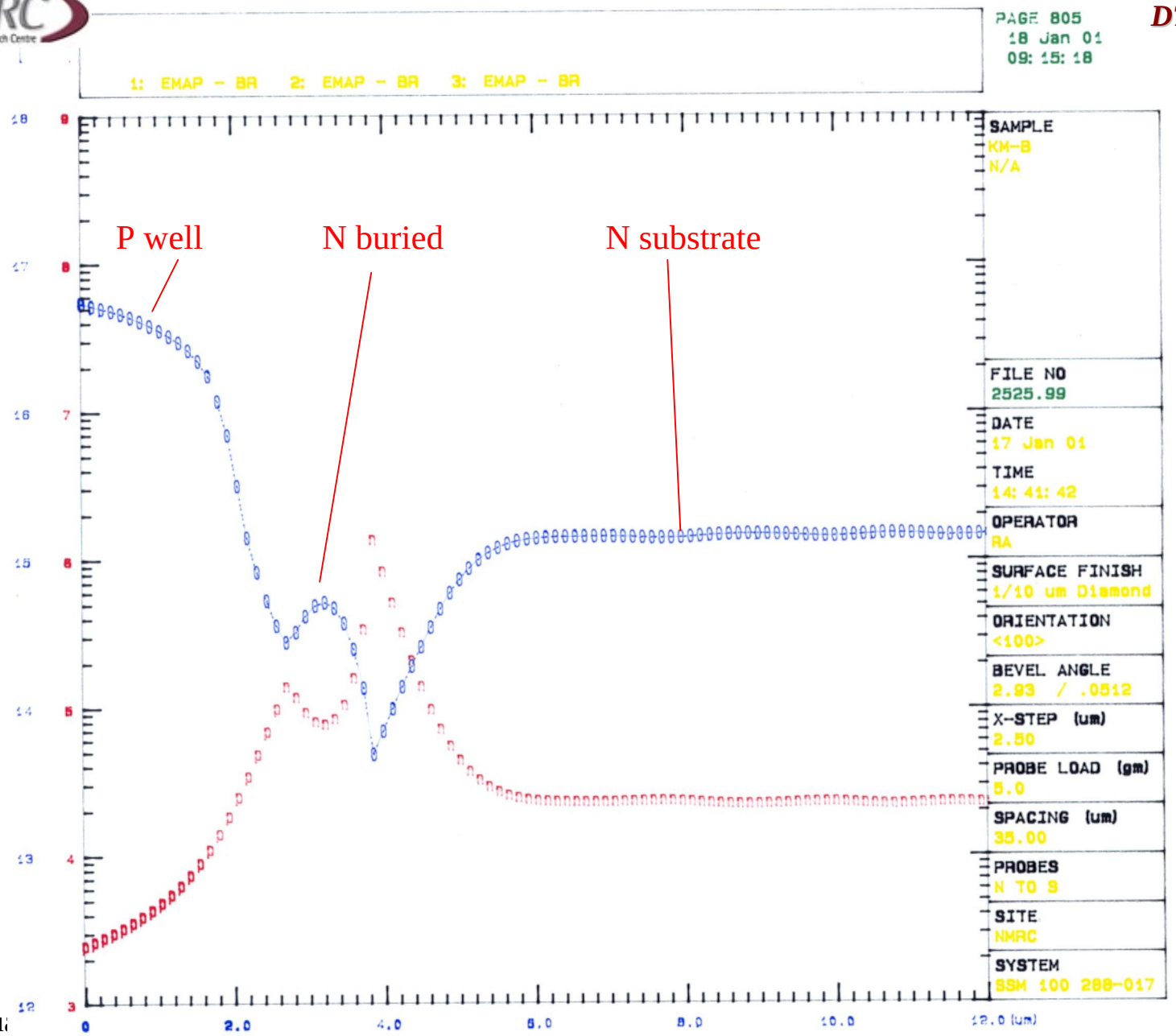
Stained bevel: High R : Cypress CYC109-20VC



Stained bevel: 6T : Cypress CYC109-25VC



Stained bevel: High R : Samsung KM681000BLGI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