Current state and future trends of PCBs in AVIO

May 20, 2014

Nippon Avionics Co., Ltd.

Contents

What's AVIO?

- Nippon Avionics Co.,Ltd. (AVIO) was established in 1960 between NEC and Hughes aircraft company.
- PCB division was licensed in multilayer board technology by Hughes.
- AVIO's PCBs were certified by JAXA in 1972, and we have been supplying PCBs for Japanese space programs more than 40 years.

JAXA : Japan Aerospace Exploration Agency

AVIOs PCB products

Space system,

Government system

High Reliability

Communication Network

Network system for Mobile phone,

Broadcast system

Semiconductor Testing

Information Processing

Super computer

High end server

IC tester

Probe Card

Load Board

Socket board

Burn in Board

1. Printed Circuit Boards qualified by JAXA

1. Printed Circuit Boards qualified by JAXA

AVIO have JAXA-qualified PCBs according to JAXA-QTS-2140 (generic specification)

JAXA-QTS-2140	Printed Wiring Boards, General Specification For

Appendix A	**PRINTED WIRING BOARDS**, GLASS BASE WOVEN POLYIMIDE RESIN OR GLASS BASE WOVEN EPOXY RESIN BASE MATERIAL
Appendix B	**FINE PITCH** PRINTED WIRING BOARDS, GLASS BASE WOVEN POLYIMIDE RESIN OR GLASS BASE WOVEN EPOXY RESIN BASE MATERIAL
Appendix D	PRINTED WIRING BOARDS, **FLEXIBLE**, POLYIMIDE FILM BASE MATERIAL
Appendix E	**RIGID-FLEX** PRINTED WIRING BOARDS
Appendix F	PRINTED WIRING BOARDS, **CIC*1 CONTROLLED THERMAL EXPANSION**, GLASS BASE WOVEN POLYIMIDE RESIN BASE MATERIAL
Appendix G	PRINTED WIRING BOARDS, **AREA ARRAY PACKAGING CAPABLE** (Qualified January 2014)
(Appendix H)	PRINTED WIRING BOARDS,**HIGH SPEED DIGITAL SIGNAL** (Under Qualification Test)

*1 CIC : Copper-Inver-Copper

JAXA-QTS-2140 can be soon available from :
https://eeepitnl.tksc.jaxa.jp/en/qts_list

2. PCBs Road Map

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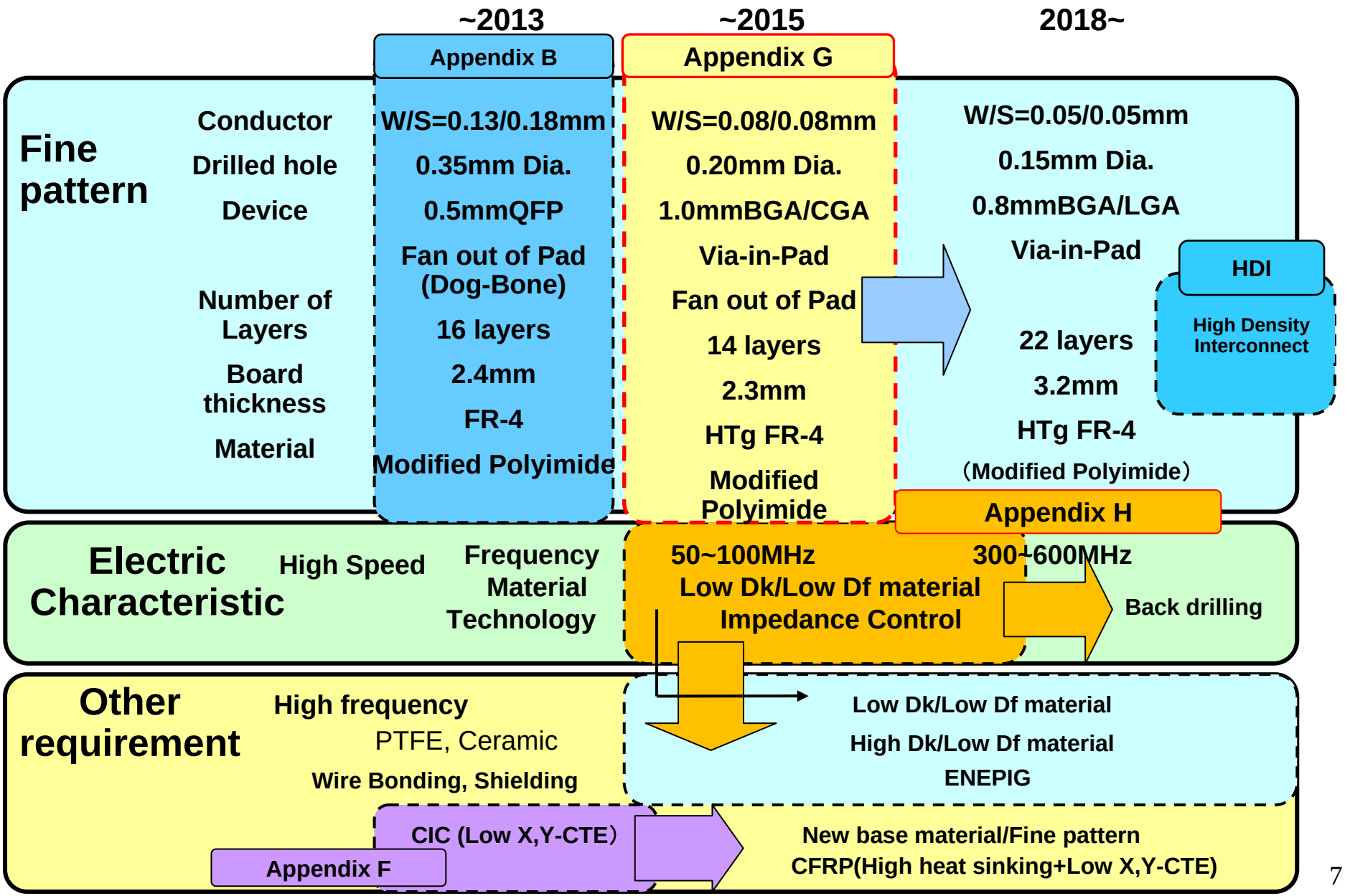


3.PCBs for AREA ARRAY PACKAGING

3. PCBs for area array package

Avio

Target of Area Array Package to be mounted on PCB

- Ceramic BGA/CGA for space use
- 1.0mm pitch
- Approximately 2000 pins

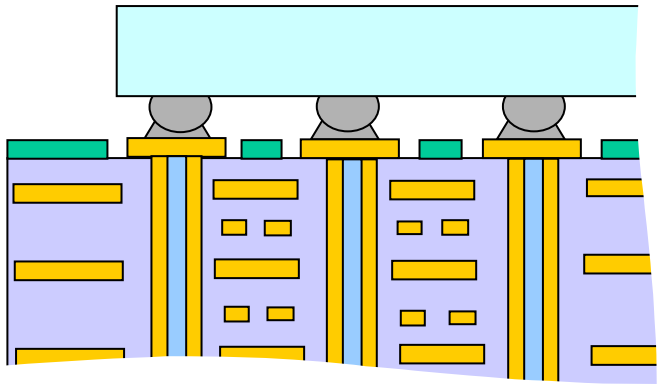
Key Technologies of PCBs

✓High density via pitch

Via-in-Pad (VIP) structure and Via fill

✓Fine pattern

Conductor Width and Spacing
0.08mm/0.08mm

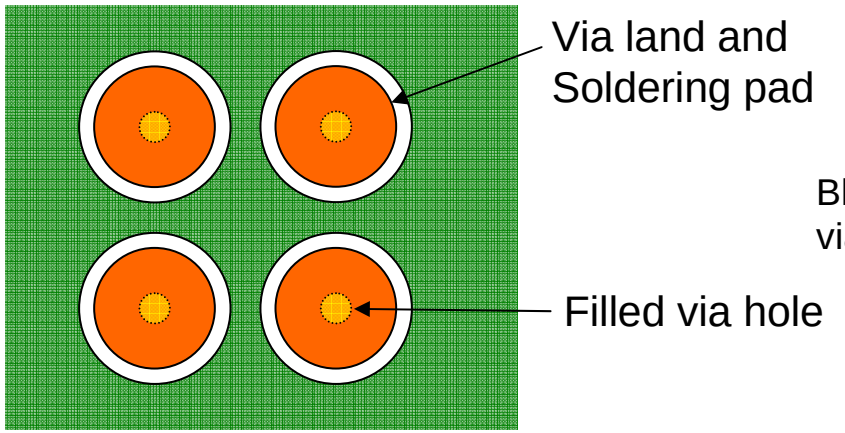


Cross section image of Area Array Package and Printed Wiring Board

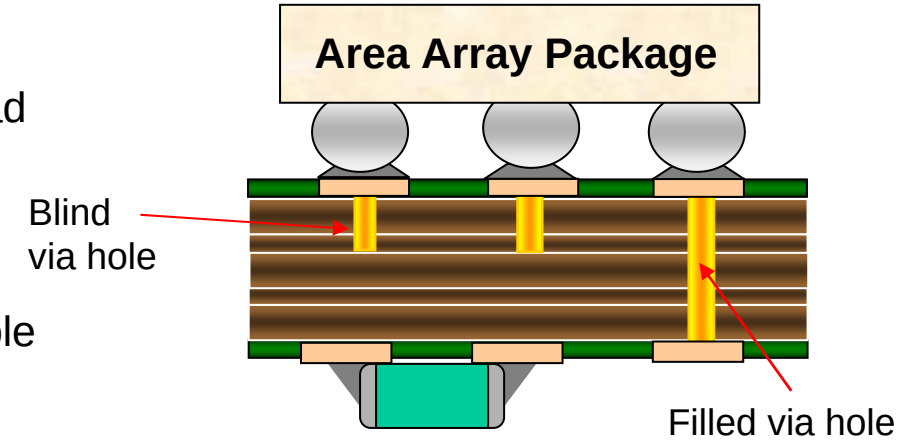
3.1 High density via pitch-1

Via-in-Pad structure and Via fill

- Via-in-Pad structure gives more flexibility to soldering pads design than Fan out pads structure.
- Via-in-Pad structure perform fine pitch area array pads with conventional high reliable PTH.



Top view of Via-in-Pad structure



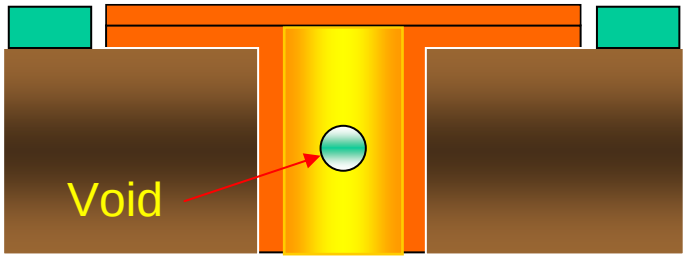
Cross section of Via-in-Pad structure

3.1 High density via pitch-2

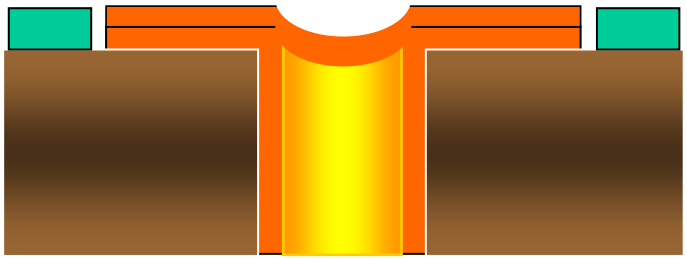
Issues of VIP

In general, Via in Pad structure has three issues as follows.
We consider that blister of cap plating is the rested issue of all.
Therefore we evaluated the blister.

1.Void in resin fill

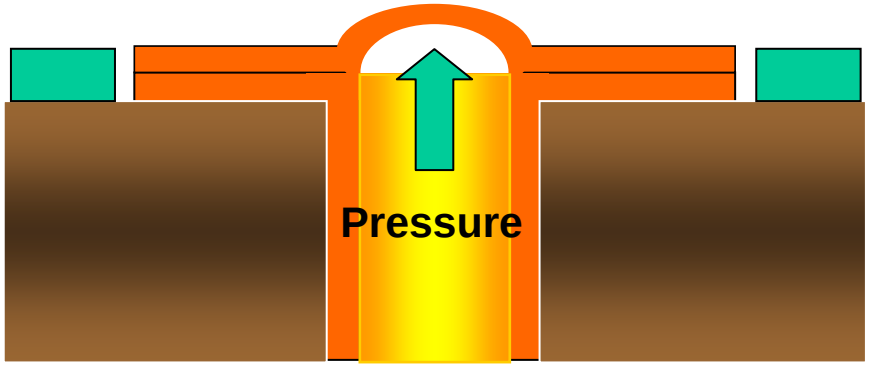


2.Dimple of cap plating



These risks can be controlled by resin fill method and process control.
Therefore we consider these as low-risk.

3.Blister of cap plating



Blister could affect long term reliability of solder joint.

Mechanism of blister occurrence

1.In soldering, cap plating receives the pressure from filled resin expanded in plated through hole.

2.Cap plating deforms beyond plastic deformation limit.

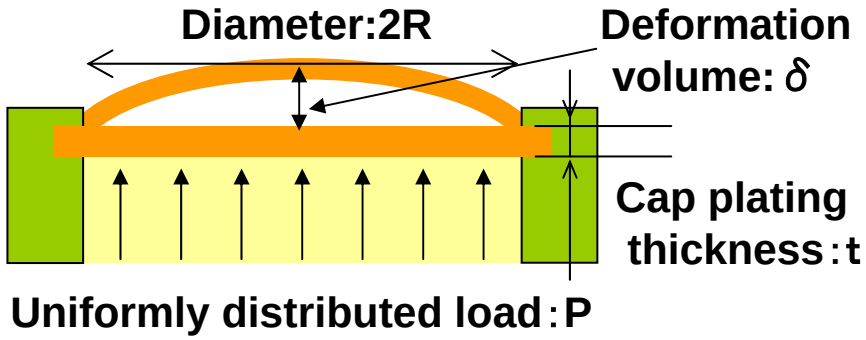
3.Then by cooling, filled resin returns to the original form, but cap plating can not return.

Blister rely on cap plating thickness and via hole (drill) diameter. We should be consideration for the optimum conditions for space use.

3.1 High density via pitch-3

Evaluation

We considered the cap plating section as picture below. Then we calculated the risk of blister occurrence as deflection volume for drill diameter and cap plating thickness shown in the table. Next we made sample board and evaluated the actual blister of cap plating by thermal stress test. We compared calculation and evaluation.



Max. deformation volume ：δ max.

$$\delta \max. = \frac{3(m^2-1)PR^4}{16Em^2t^3}$$

Young's modulus :E Poisson's ratio ：1/m

Condition of blister evaluation

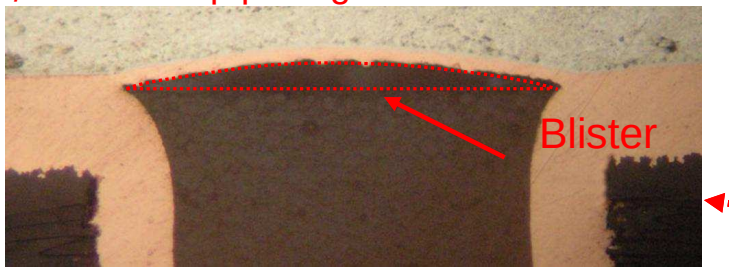
Drill diameter	φ0.20, 0.25, 0.30, 0.35mm
Cap plating thickness	0.005, 0.010, 0.015, 0.020, 0.040, 0.045, 0.050, 0.055mm
Board thickness	2.4mm
Test condition	Thermal stress test (Solder float) Temperature=288℃, Time=10seconds, Operation=3times
Evaluation method	Observation of cross section by microscope
Requirement	No blister

3.1 High density via pitch-4

Result of Evaluation

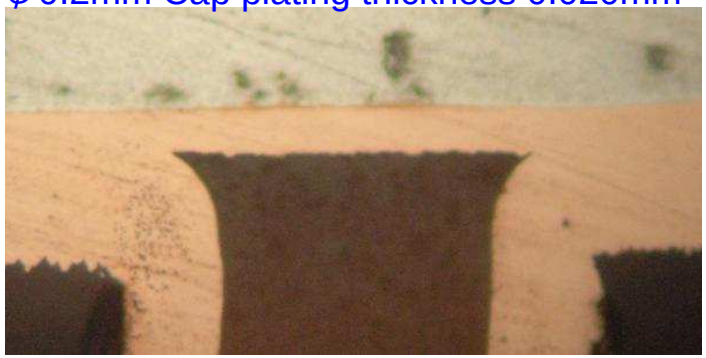
We obtained risk curve and blister occurrence for each drill diameter and cap plating thickness.

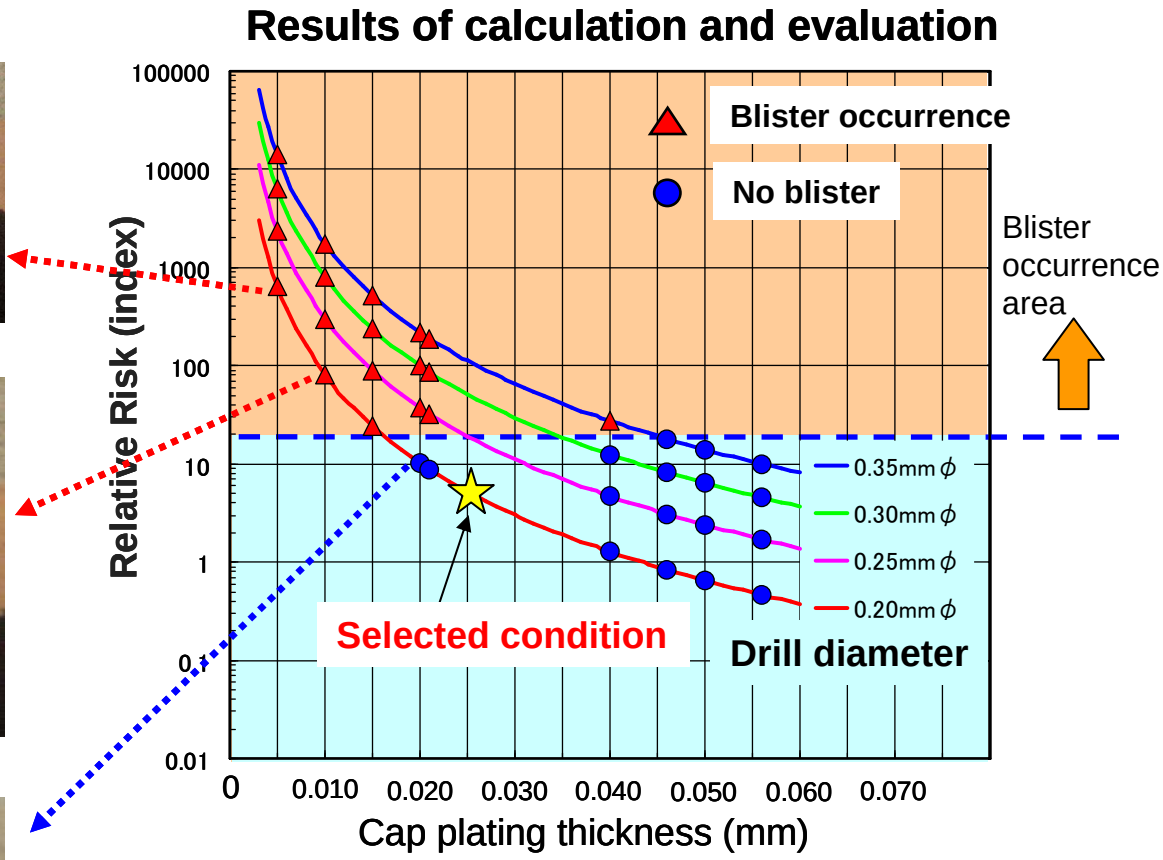
ϕ0.2mm Cap plating thickness 0.005mm



ϕ0.2mm Cap plating thickness 0.010mm

ϕ0.2mm Cap plating thickness 0.020mm



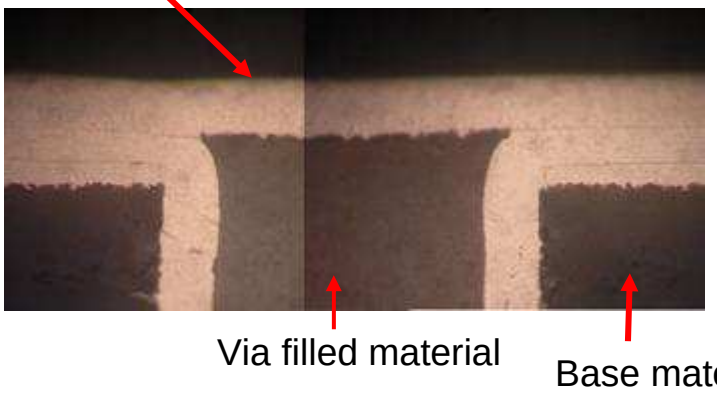


We find that blister occurrence risk decreases by using small drill diameter and thick cap plating from above chart.
We selected condition of Via in pad structure with margin.
Dill diameter= ϕ0.20mm,
Cap plating thickness=0.025mm(nominal)

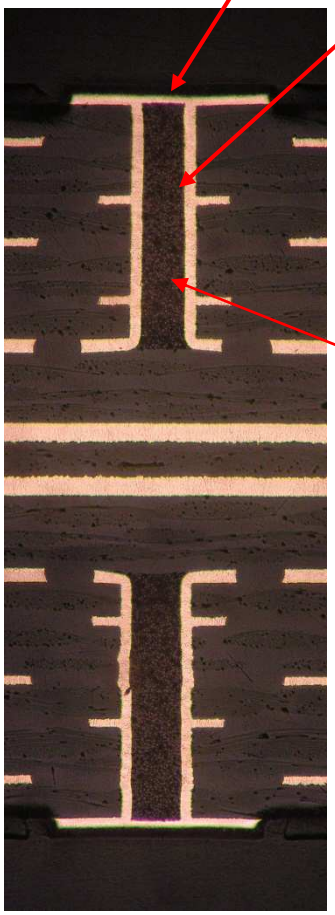
3.1 High density via pitch-5

Via-in-Pad structure and Via fill

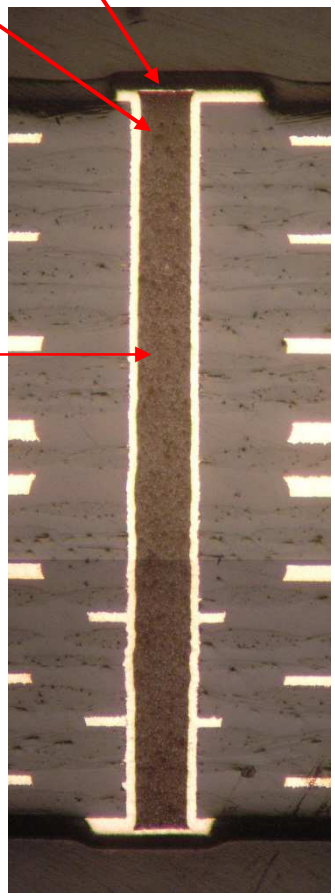
Soldering Pads need flatness of surface without void in solder or other soldering problem. We solved this issue by vacuum via filled technology.



Magnifying of Via-in-Pad



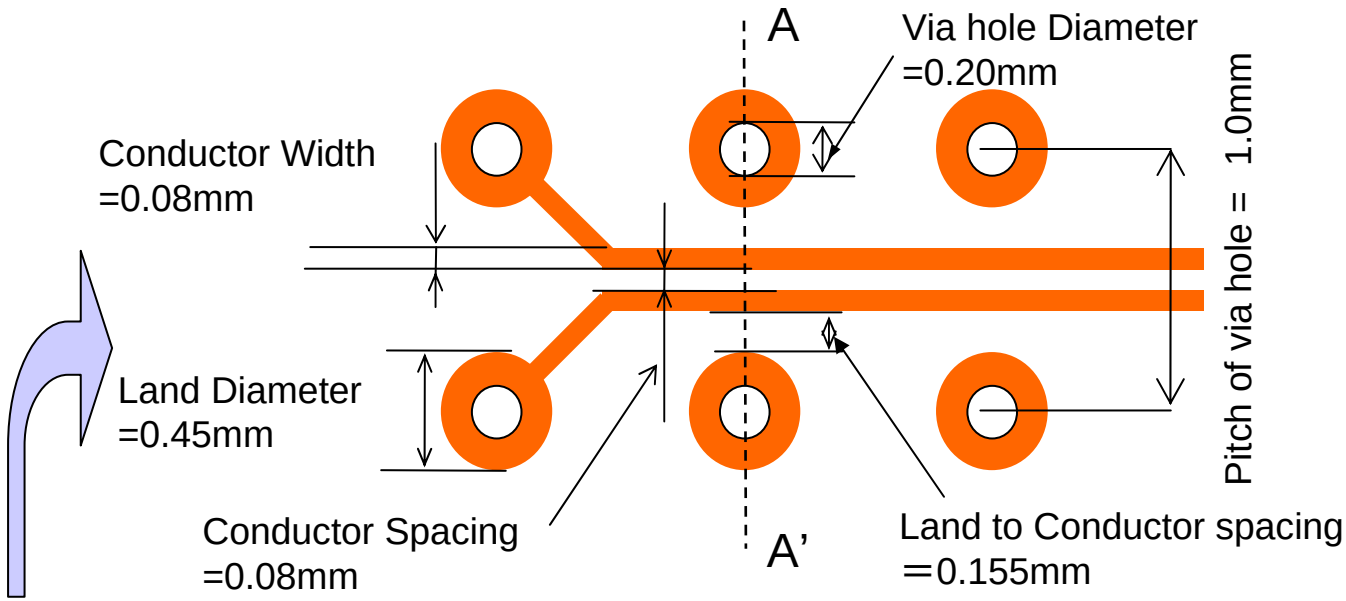
Cross section of Blind Via Holes



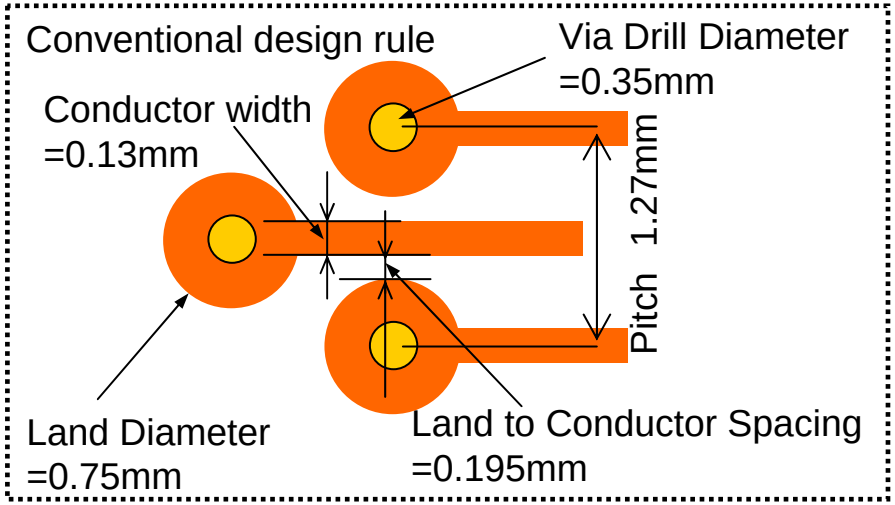
Cross section of Via Hole

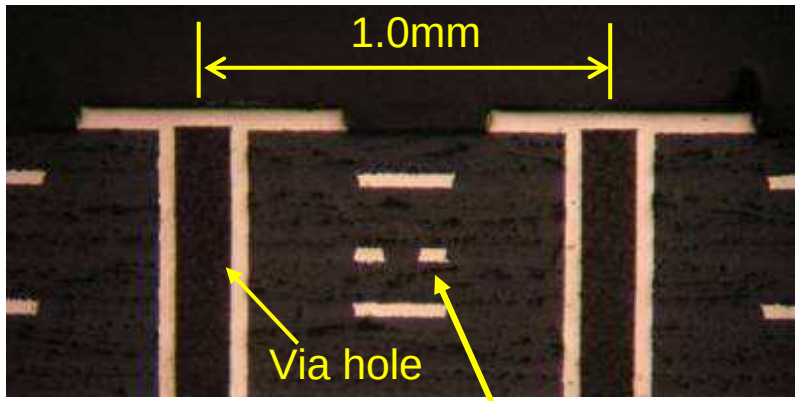
3.2 Fine pattern layout

Design for 1.0mm pitch via hole and two signal lines.



Laser direct imaging





Conductor Width and Spacing=0.08mm/0.08mm

Cross section of A-A'

3.3 Qualification Test

We passed the Qualification Test under JAXA-QTS-2140 Appendix G.

The main items of QT are as follows;

Item	Requirements	Result
Thermal cycling	-30 to +125 deg.C, 1,000 cycles (Preconditioning : 240 deg.C, max. reflow 3 times)	pass
Solder bath float	288 deg.C , 10 seconds	pass
Hot oil dip Resistance	260deg.C, 10seconds, 10 cycles	pass
Humidity and Insulation Resistance	25 to 65deg.C, 90~98%RH, less than 500M ohm	pass
Dielectric Withstanding Voltage	500Vdc, 30 seconds	pass
Radiation Hardness	$1X10^4$Gy, less than 500M ohm	pass

3.4 Specification

Table: Specification JAXA-QTS-2140 Appendix G.

Item		**Specification**	
Pad	Pitch	1.0mm	
	Structure	Fan out of Pad	Via-in-Pad
Drilled hole diameter		0.20mmDia.	
Conductor (External)	Width	0.10mm	
	Spacing	0.15mm	
Conductor (Internal)	Width	0.08mm	
	Spacing	0.08mm	
Number of Layers	Total	14	
	Blind via	6	
Board thickness	Modified Polyimide	2.1mm	
	HTgFR-4	2.3mm	
Surface finish		HASL*(SnPb solder)	

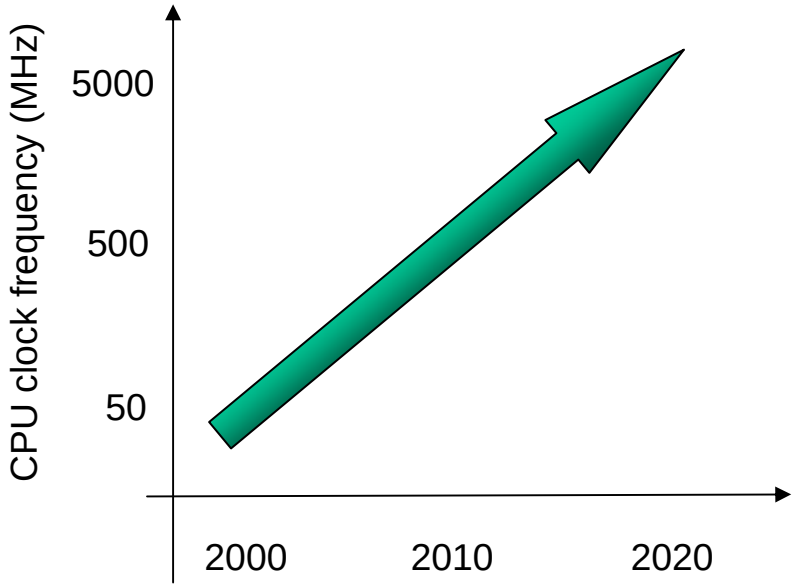
*Hot Air Solder Leveler

4.PCBs for High Speed digital signal

4. PCBs for high speed digital signal

Target of Development

- Frequency : Higher than 1GHz
- Impedance control : +/- 10 %
- Qualified : Oct. 2014



Transition of CPU clock per years

Elemental Technologies

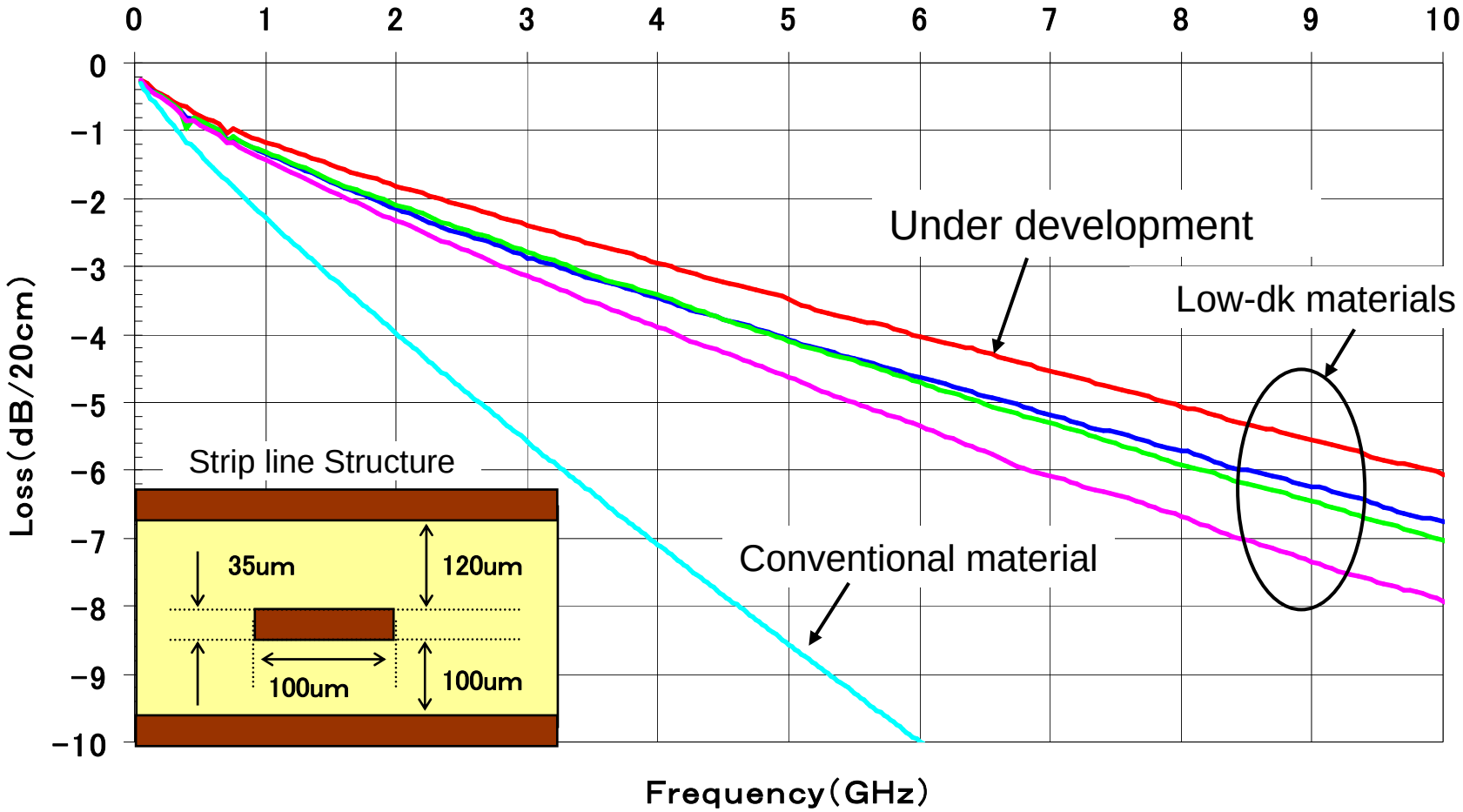
✓ Processing technology for low dielectric constant material

✓ High accuracy conductor width control

by thin conductor thickness and large number of layers

4. PCBs for high speed digital signal

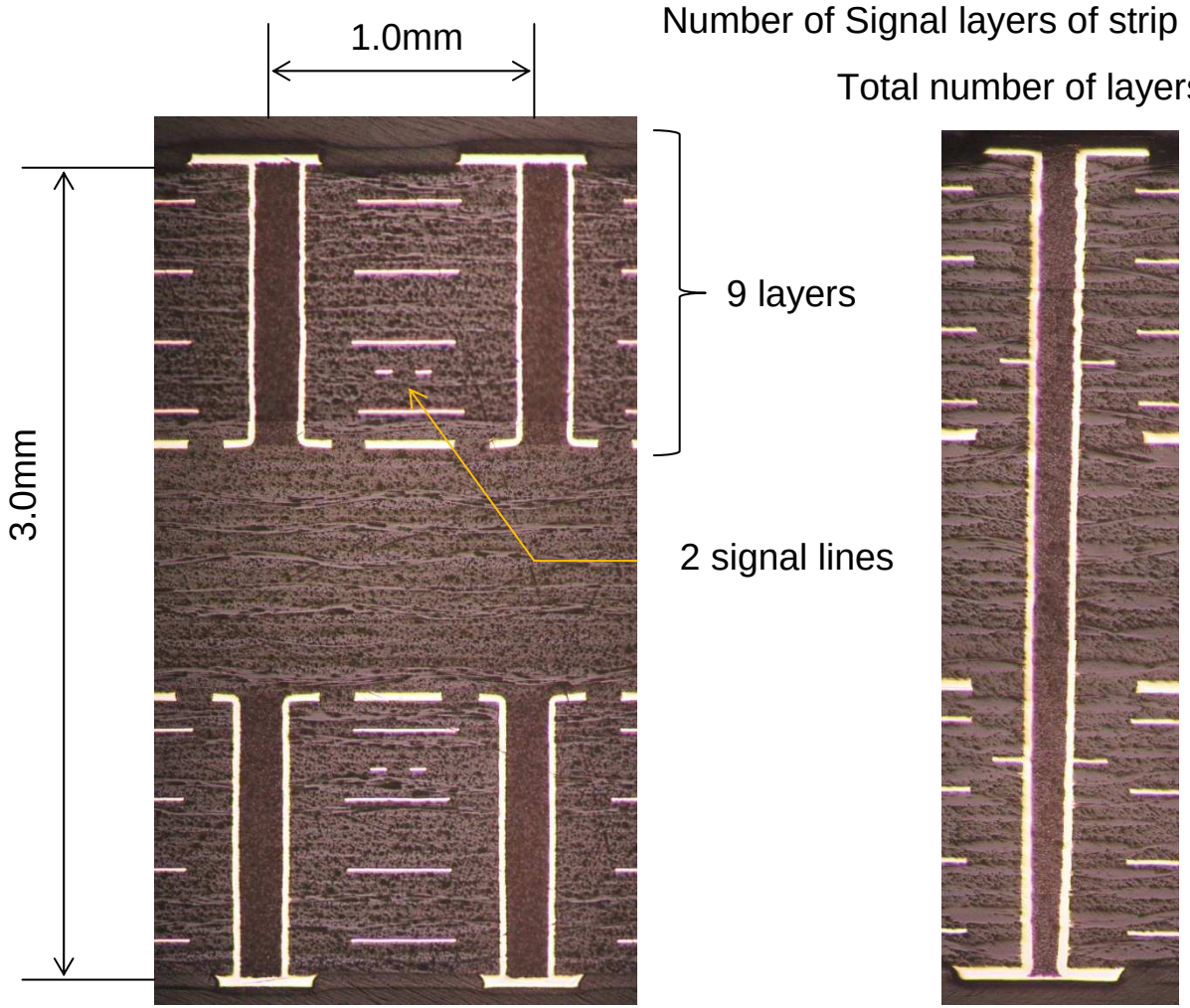
We evaluated signal loss of 4 types Low dielectric constant (Low-dk) materials and conventional material. We selected the material with best result.



Measuring instrument : Network analyzer E8363B Agilent technologies inc

4. PCBs for high speed digital signal

High accuracy conductor width control for characteristic impedance control by thin conductor thickness, low profile copper foil, and large number of layers.



Cross-section of Blind via hole

Number of Signal layers of strip line structure = 6

Total number of layers = 18

Cross section of PTH

4. PCBs for high speed digital signal

Avio

Specification

Item		**Specification**	
Base Material	Dk (ε r) (1GHz)	3.65	
	Df (tan δ) (1GHz)	0.002	
Pad	Pitch	1.0mm	
	Structure	Fan out of Pad	Via-in-Pad
Drilled hole diameter		0.20mmDia.	
Conductor (External)	Width	0.12mm	
	Spacing	0.14mm	
Conductor (Internal)	Width	0.07mm	
	Spacing	0.08mm	
	Thickness	0.018mm	
Number of Layers	Total	18	
	Blind via	9	
Board thickness		3.0mm	
Surface finish		HASL(SnPb solder)	

5. Summary

5. Summary

•Needs to Printed Circuit Boards for space use are to respond to the high performance and down sizing of electronic components.

-We were qualified capable PCBs that be 1.0mm pitch and 14 layers for high pin counts BGA/CGAs.

-We are developing PCBs for high speed digital signal with Low-Dk. (We will finish in September 2014)

Thank you for your attention.

Point of Contact

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Mt. Fuji was registered as a world cultural heritage in 2013.

http://www.avio.co.jp/products/mlb/index.htm