



# Capacitors Basics & Applications

**KEMET**  
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Applications - I  
Oct 2006

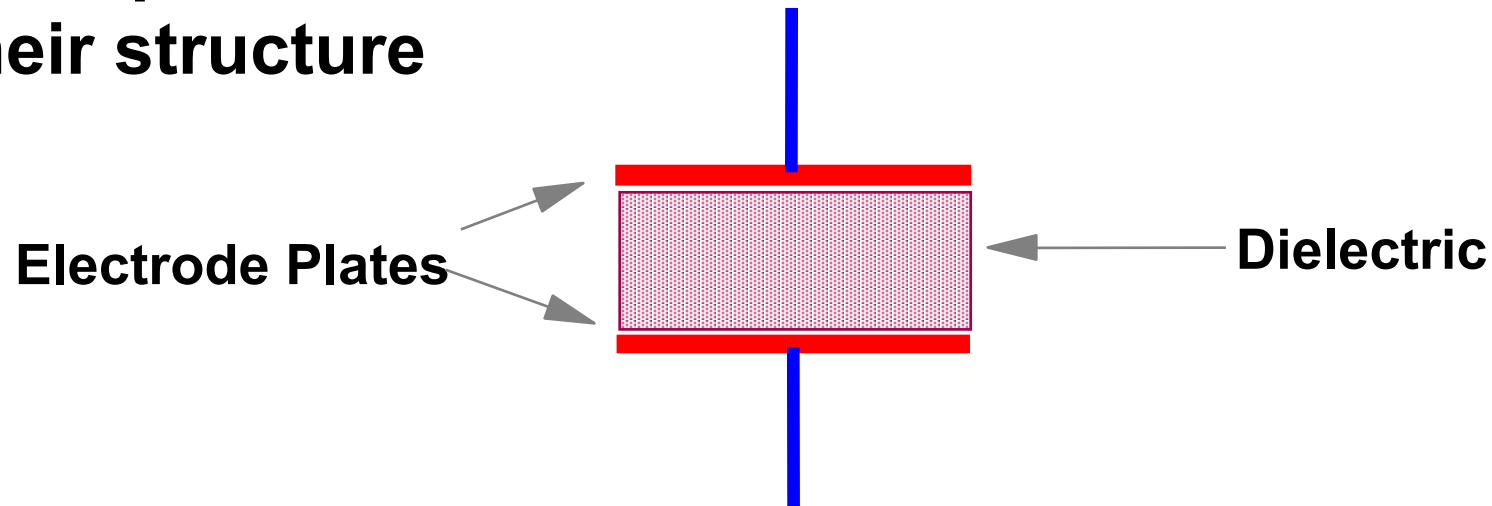
CARTS-Asia 2006

# Capacitors & Applications



**Ceramic**  
**Tantalum**  
**Alum. Elect.**  
**Film**

**All capacitors utilize the same basic mechanism in their structure**



**The value of a capacitor is measured in farads. For 1 farad of capacitance, 1 coulomb of charge is stored on the plates, when 1 volt of force is applied.**

$$1 \text{ farad} = 1 \text{ coulomb} / 1 \text{ volt}$$

**1 coulomb represents  $\sim 6 \times 10^{19}$  electrons**

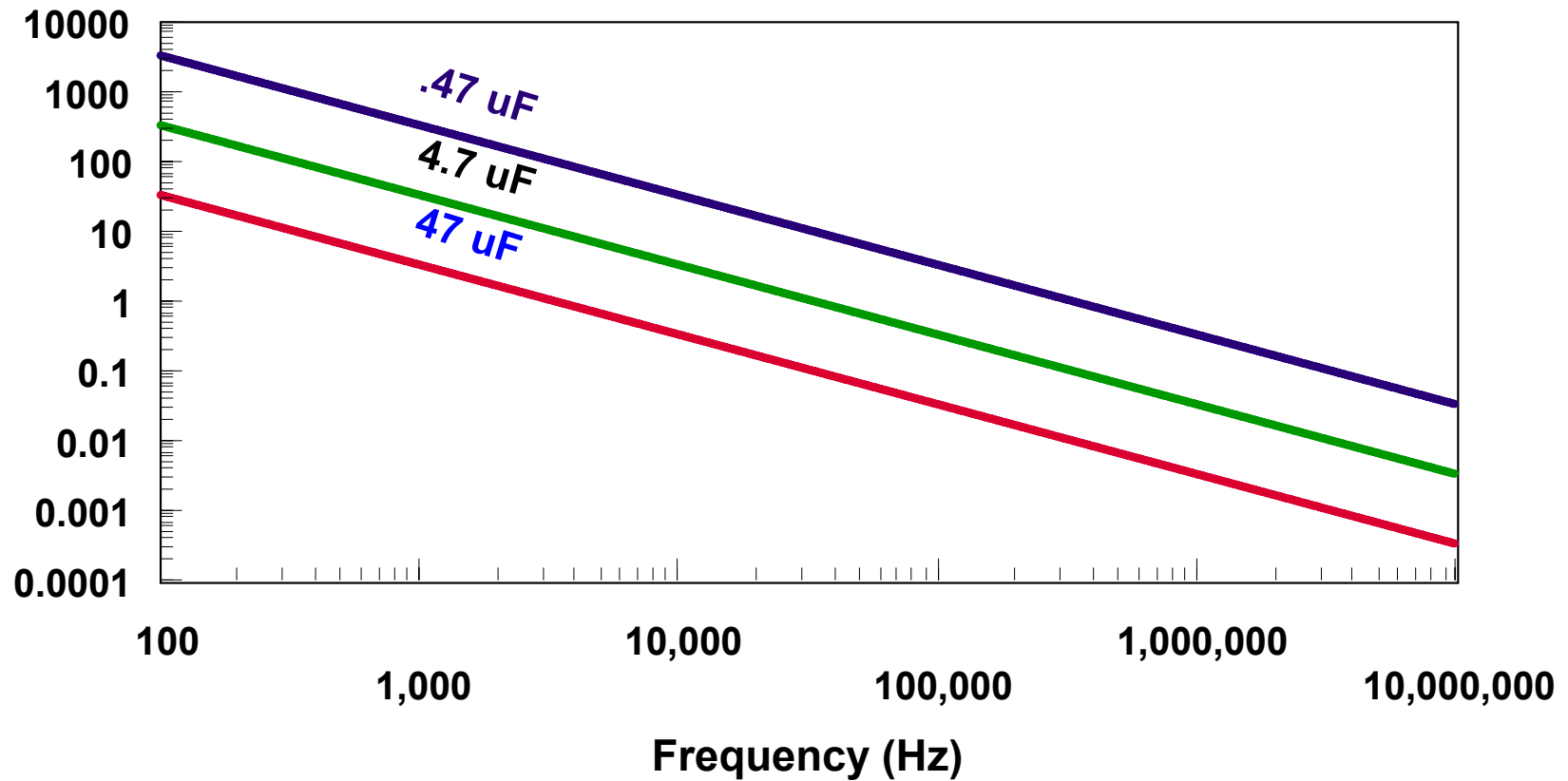
## “Pure” Capacitor

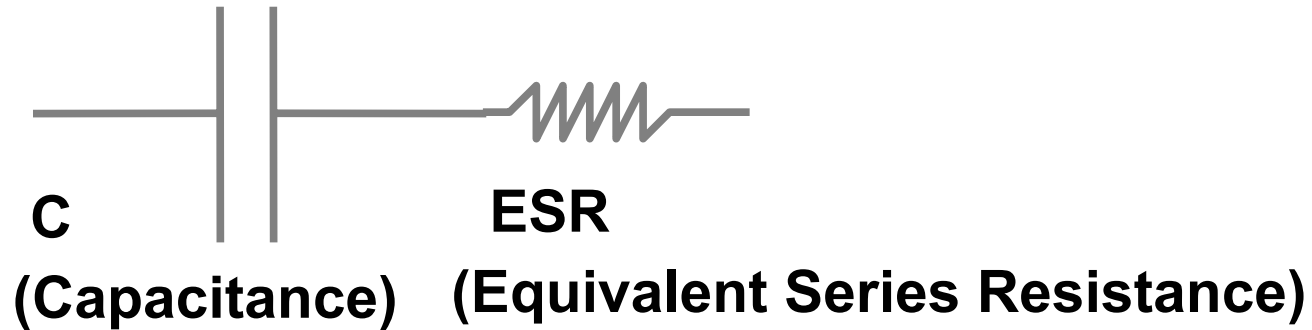


$$Z = X_C = \frac{1}{2\pi f ( \text{Hertz} ) C ( \text{Farads} )}$$

# “Pure” Capacitor’s Performance

Impedance (Ohms)





$$|Z| = \sqrt{X_C^2 + ESR^2}$$

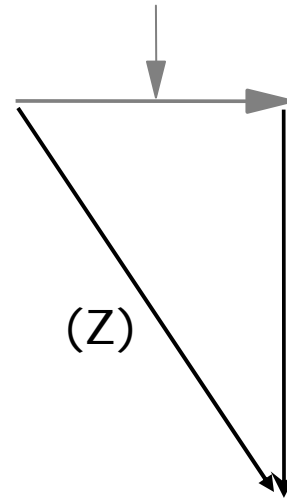
# Impedance, Reactance, and Resistance are **Vectors**

## Impedance

**Z** is complex, containing both real and imaginary coefficients, or magnitude and angle (direction).

Resistance

(ESR)  
is "Real Element"

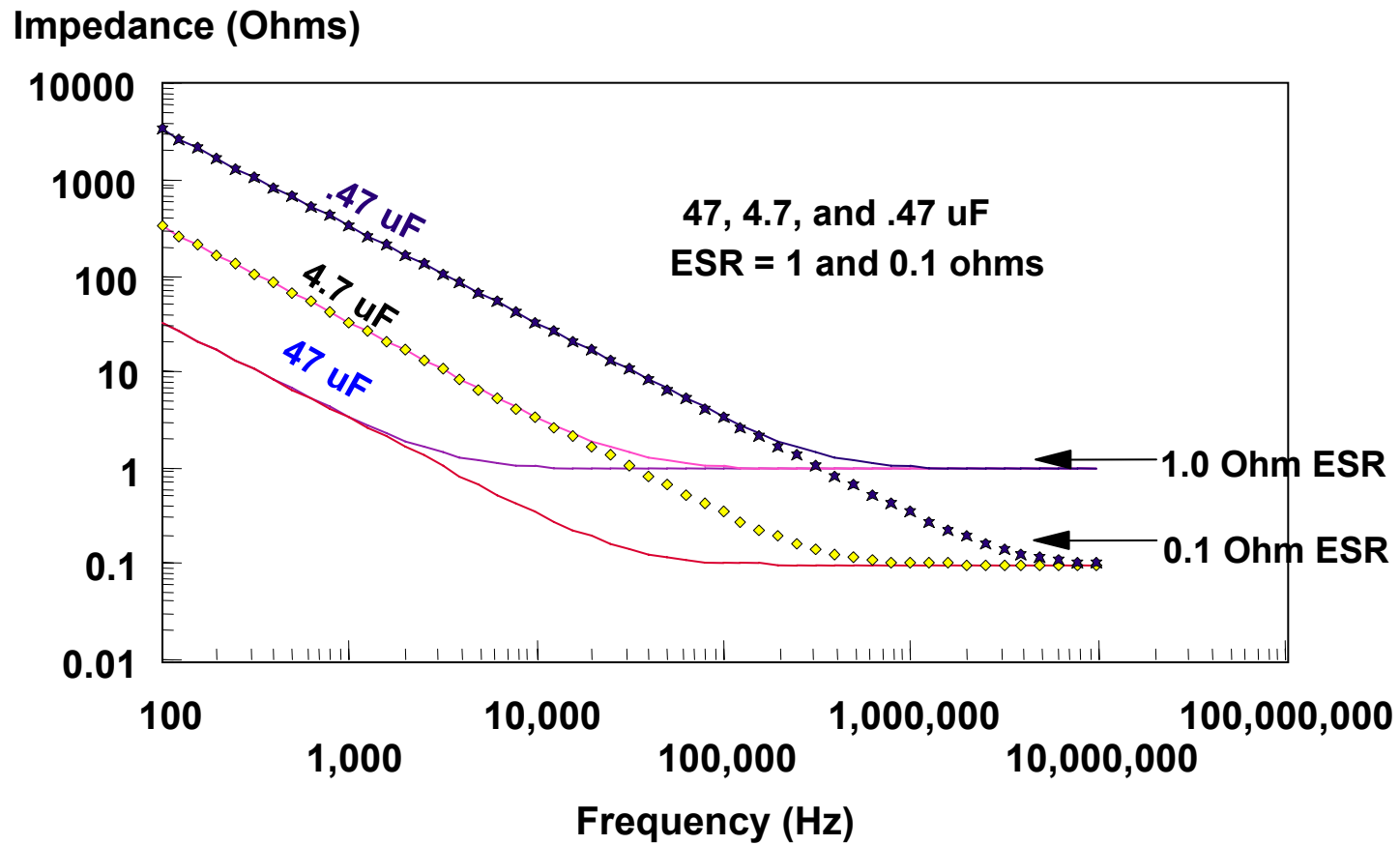


Reactance

$(\vec{X}_L + \vec{X}_C)$   
is imaginary

$$|Z| = \sqrt{X_C^2 + ESR^2}$$

## Capacitance with ESR vs. Frequency





**High Frequency or Tuned Circuit  
Applications**

**Q**

**Power Applications**

**ESR**

**General Applications**

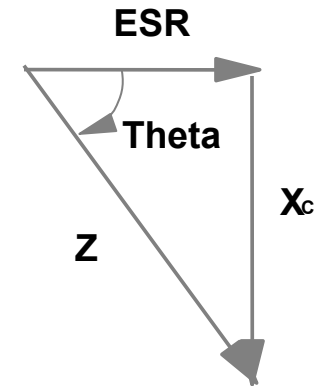
**DF**

Based on Vector relationship

$$DF = \cot(\text{Theta}) = ESR / X_c$$

$$PF = \cos(\text{Theta}) = ESR / Z$$

$$Q = \tan(\text{Theta}) = X_c / ESR = 1 / DF$$



*where*

**DF = Dissipation Factor**

**PF = Power Factor**

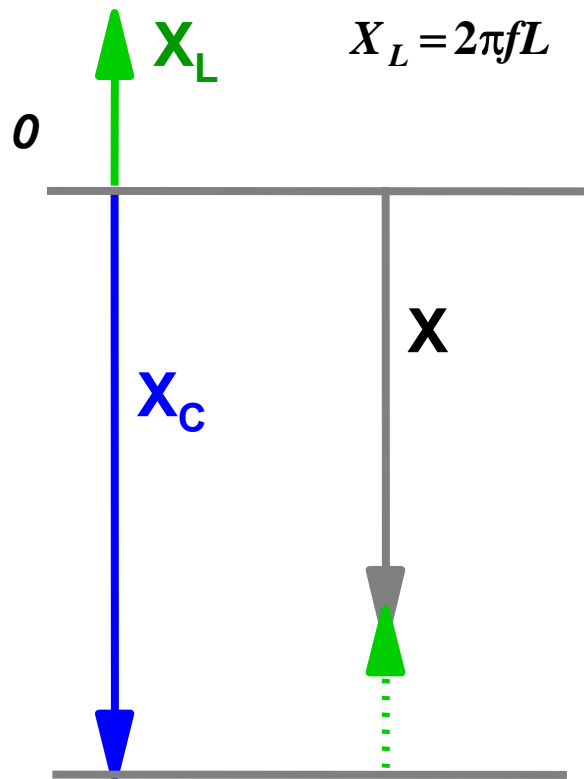
**Q = "Q" or figure of merit**

## The “RLC” Circuit

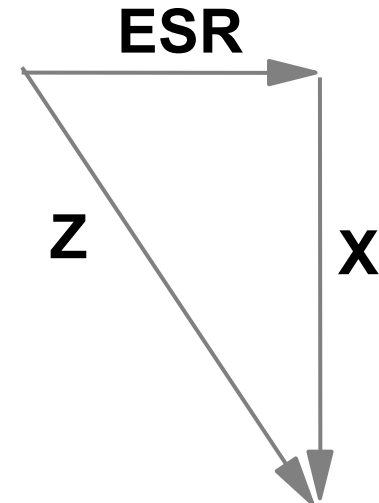


**ESL or Equivalent Series Inductance is created by restricting current to a defined, physical path**

**ESL - Inductive Reactance ( $X_L$ ) opposes Capacitive Reactance**



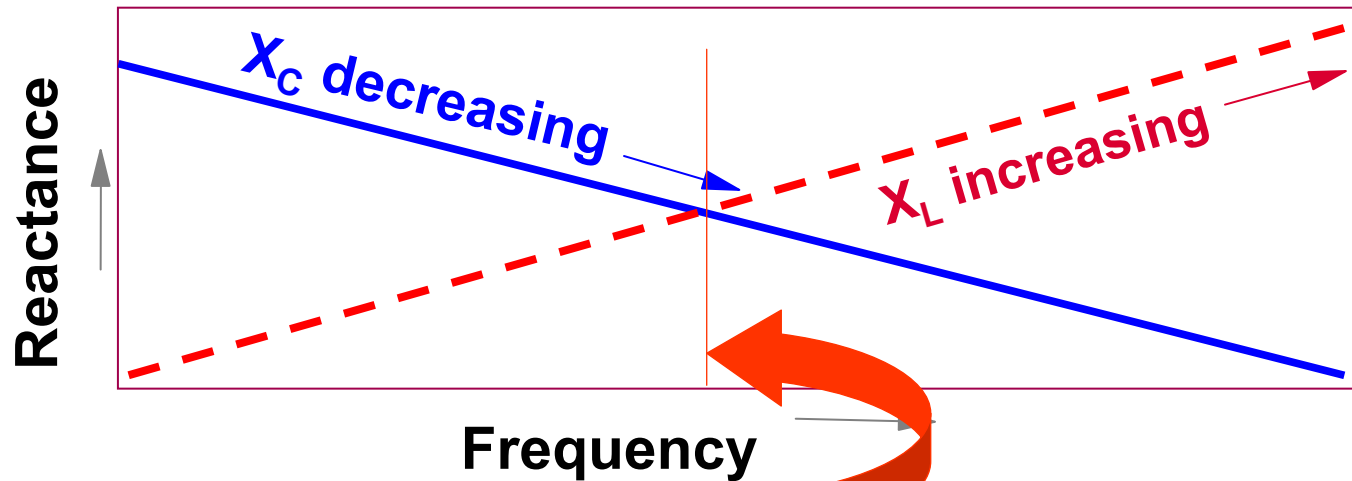
**Impedance is a factor of vector summation.**



$$\vec{Z} = \vec{X}_C + \vec{X}_L + \vec{R}$$

**or**

$$|Z| = \sqrt{(|X_C| - |X_L|)^2 + |R|^2}$$



The frequency at which  $X_C = X_L$  is the **self-resonant frequency.**

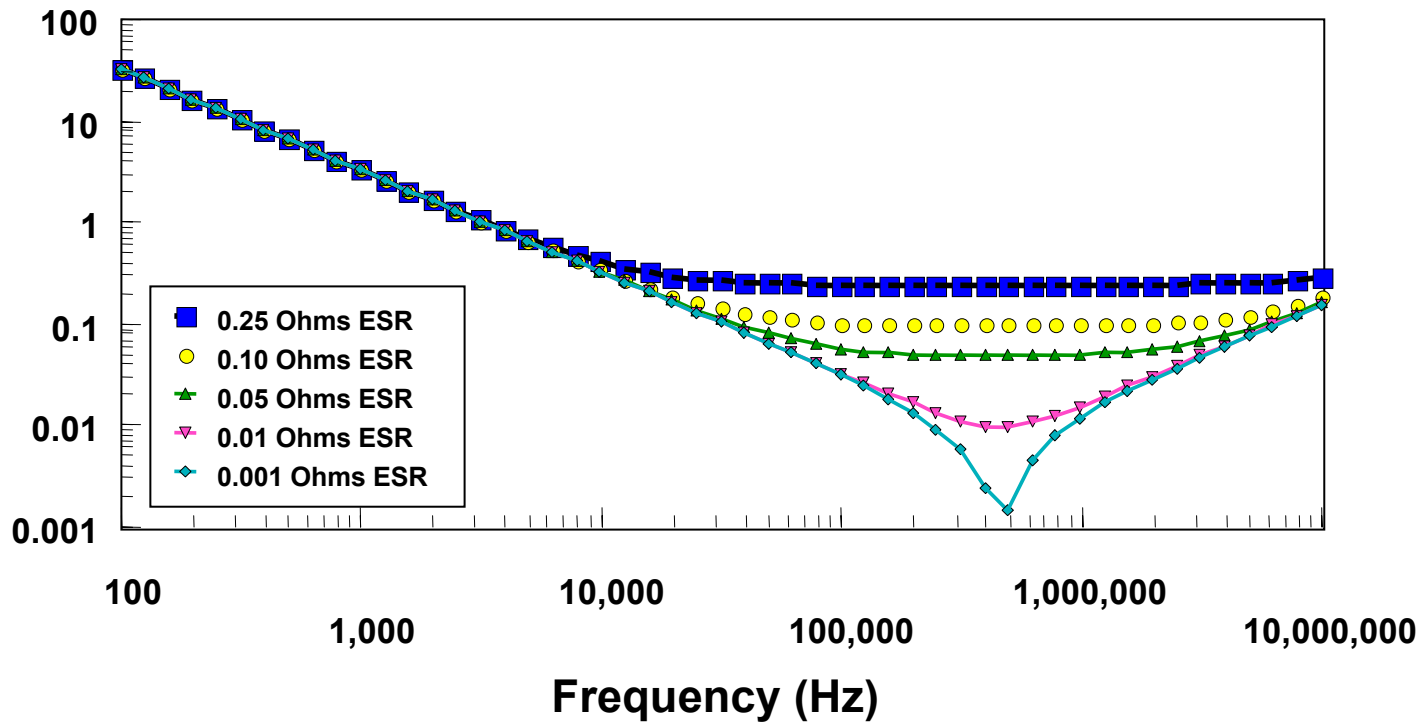
At this frequency,  $X_C = -X_L$ , or zero, and the impedance is equal to the ESR.

Prior to this frequency, component behaves as capacitor; after this frequency, component behaves as inductor.

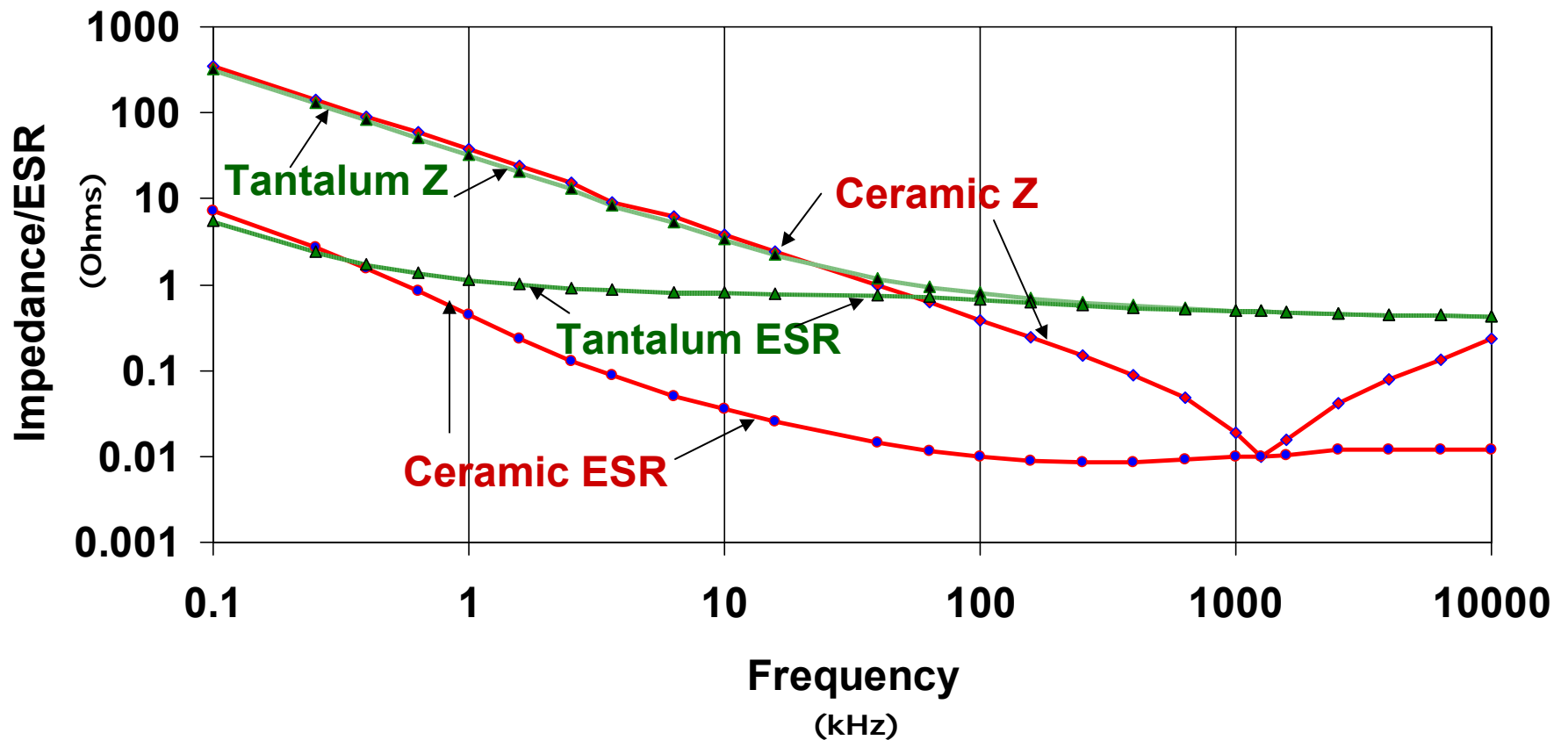
$$f = \frac{1}{2\pi\sqrt{LC}}$$

## 47 $\mu\text{F}$ Capacitance / 2.5 nH ESL Impedance versus Frequency versus ESR

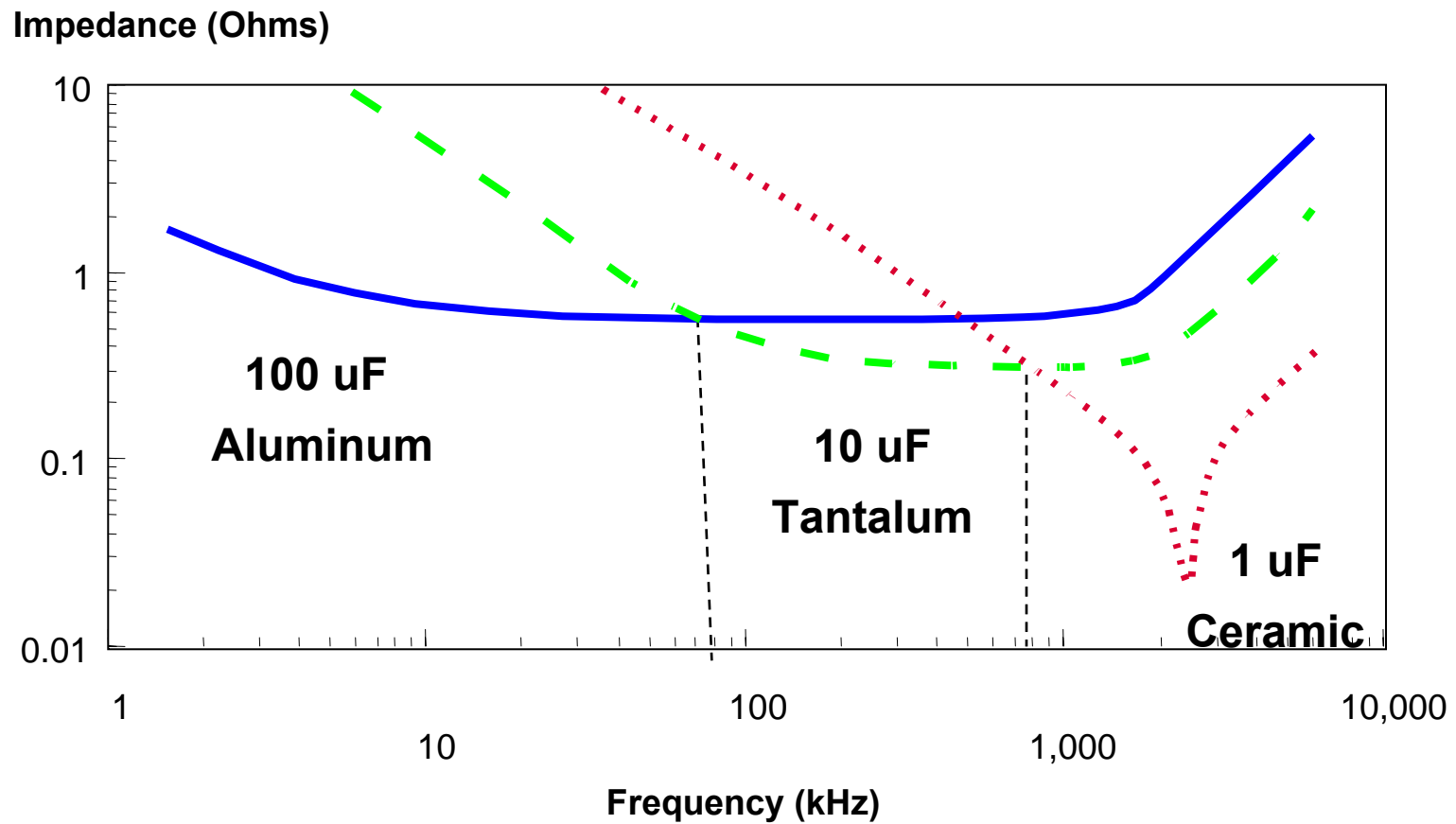
Impedance (Ohms)



Ceramic vs. Tantalum (4.7 uF)

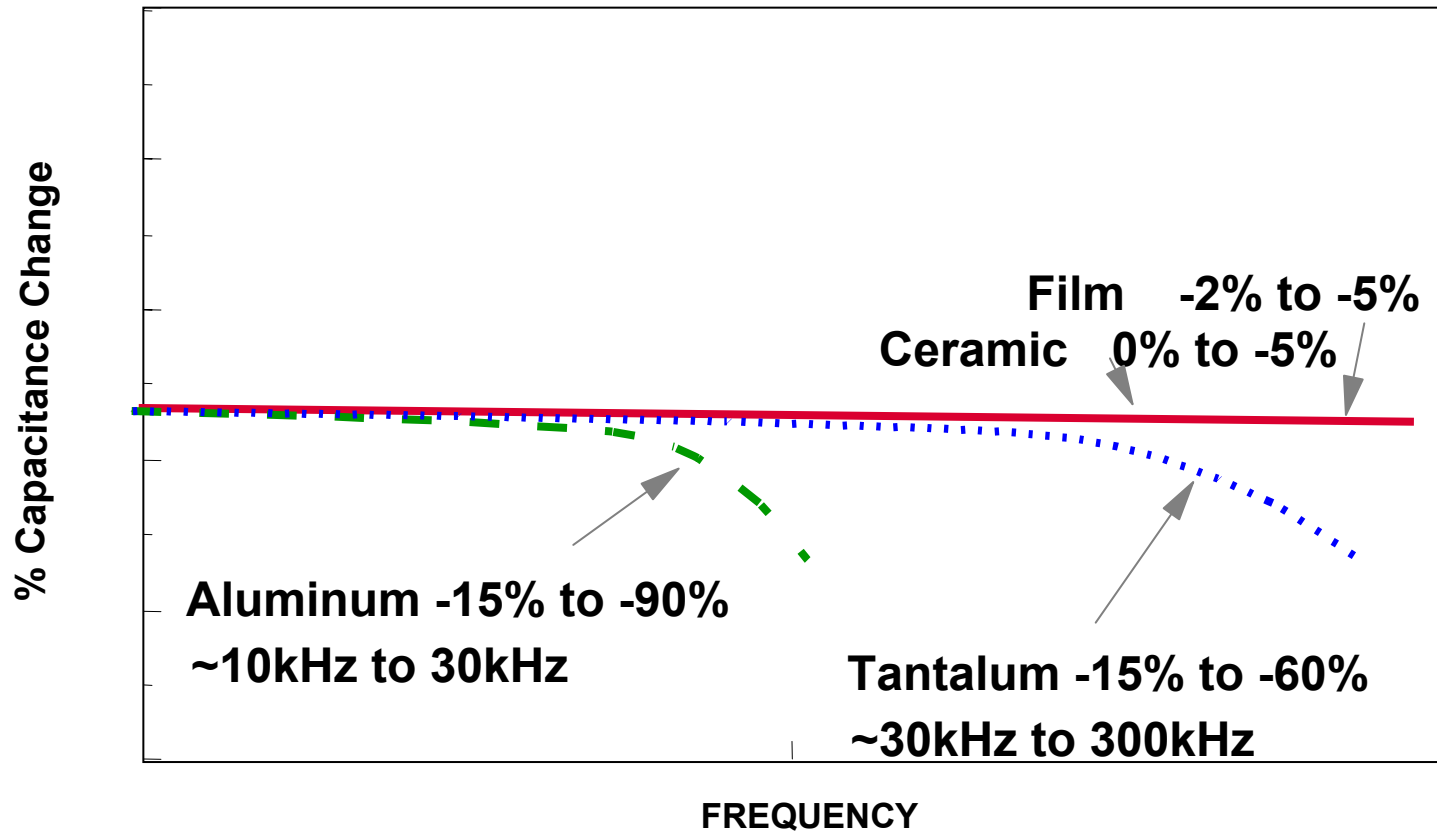


Lowest Impedance is not always highest Capacitance



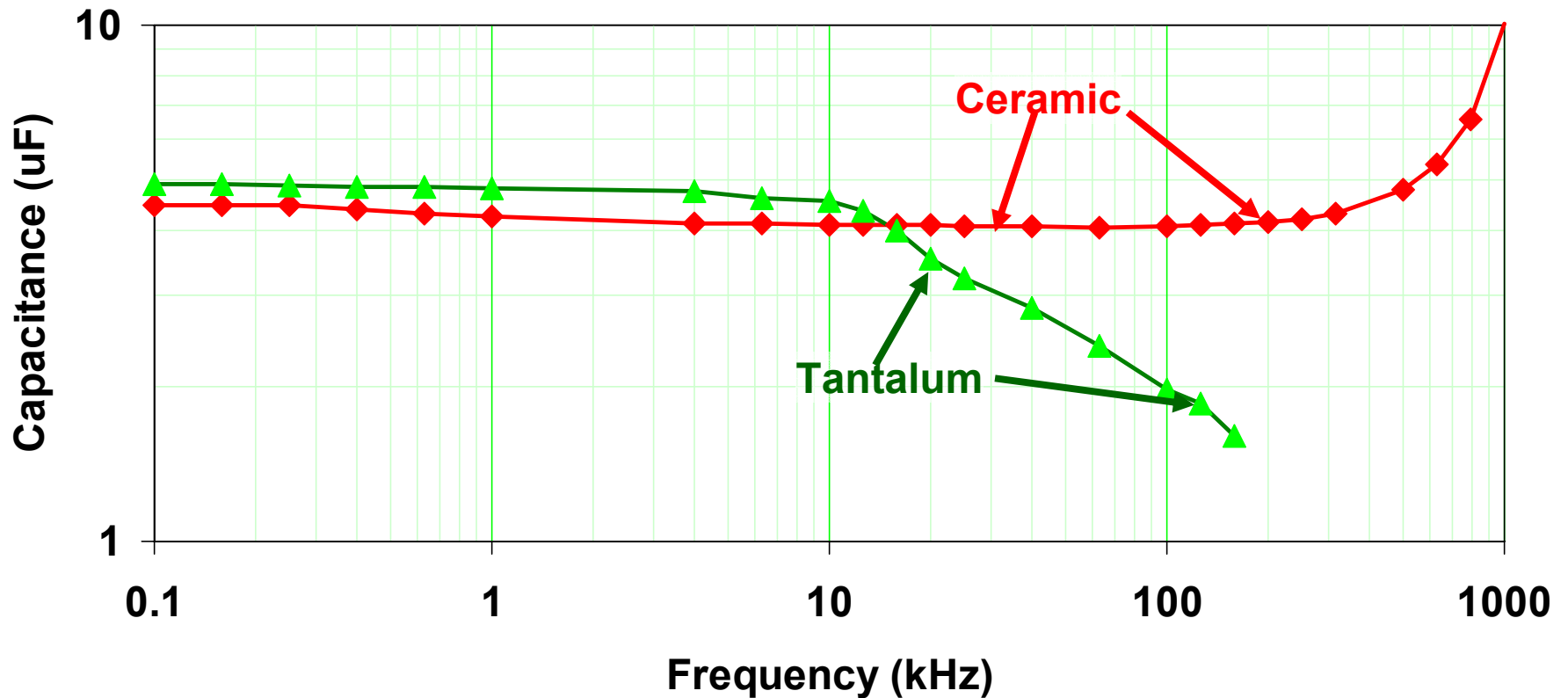


## Capacitance change with frequency



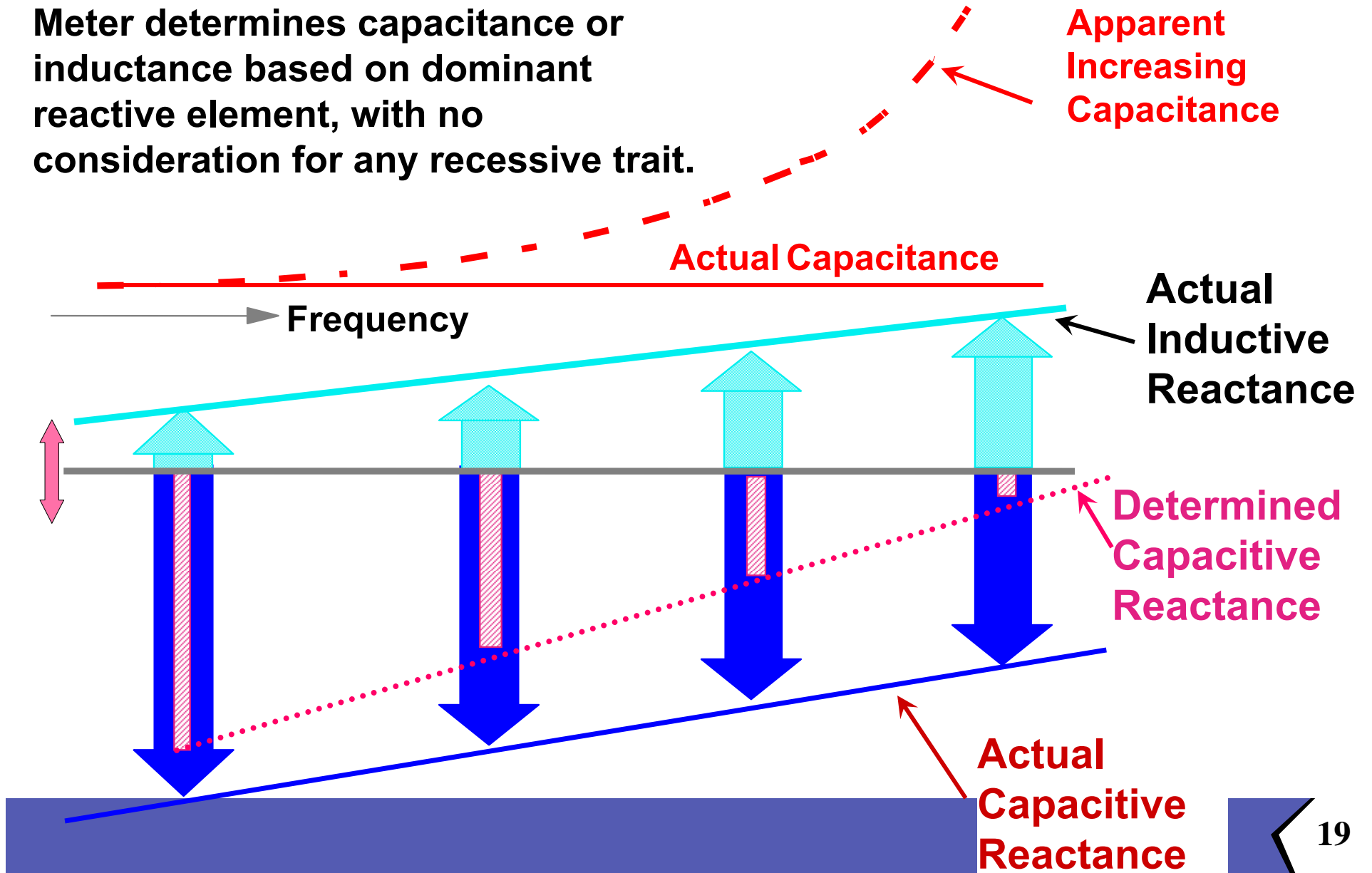
## Actual capacitance change - measured

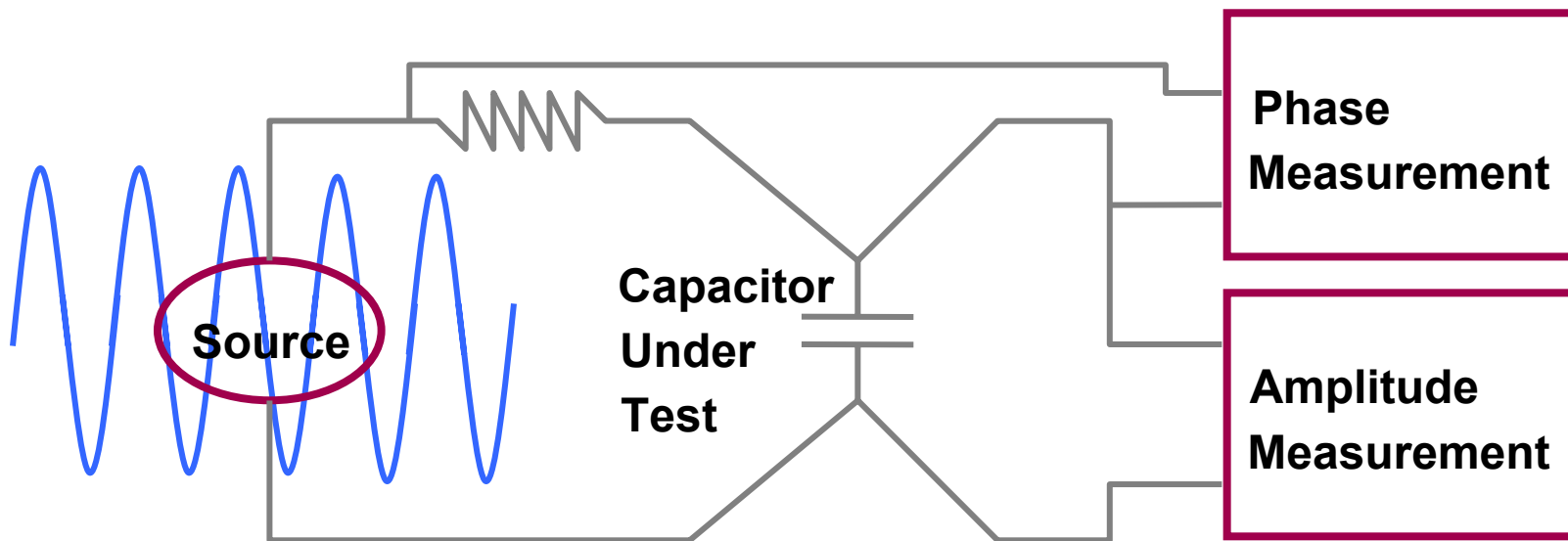
**4.7 uF Tantalum vs. Ceramic**  
**T491B475K010 vs. C700 Z5U 50 WVDC**  
**Capacitance vs. Frequency**



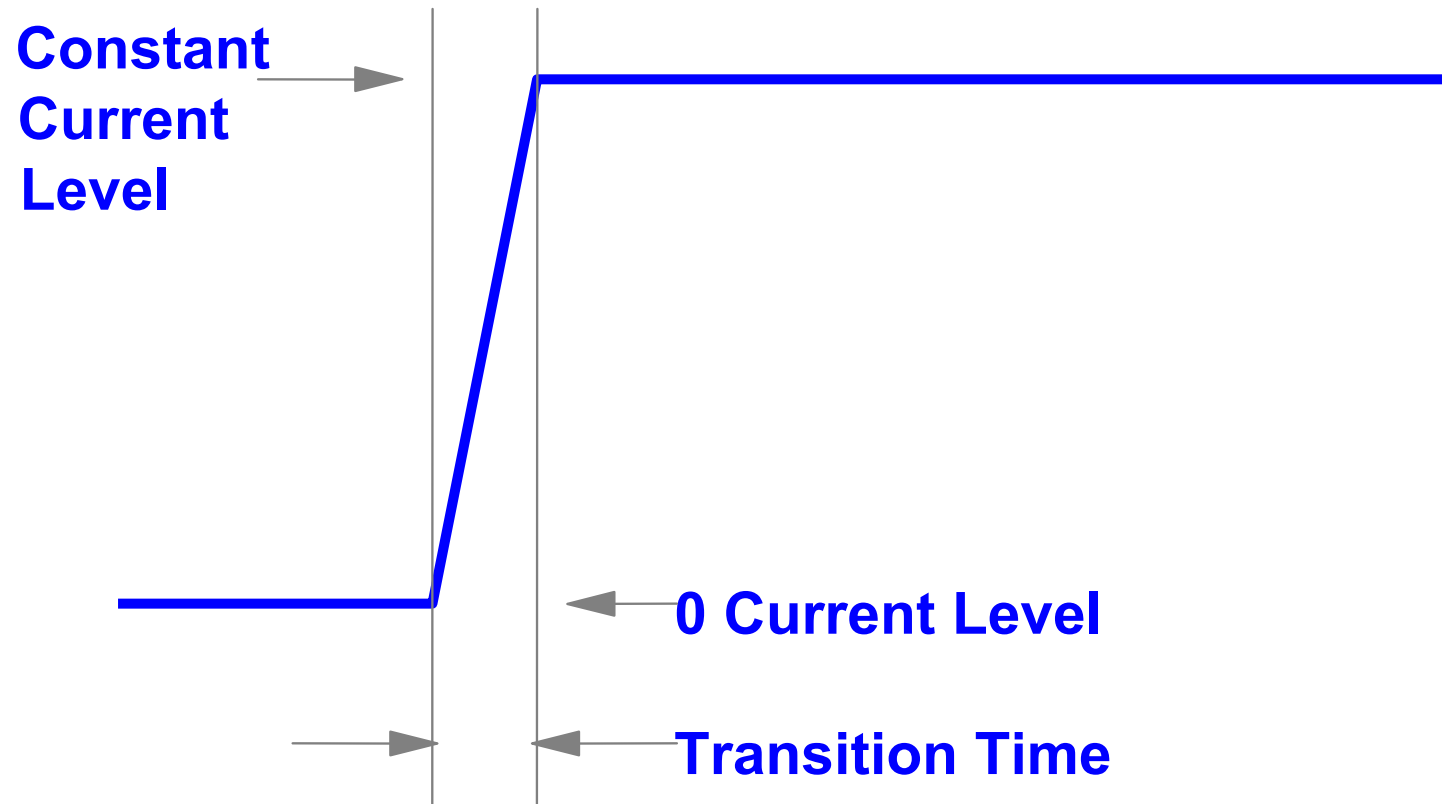
# False Capacitance Peaking

Meter determines capacitance or inductance based on dominant reactive element, with no consideration for any recessive trait.

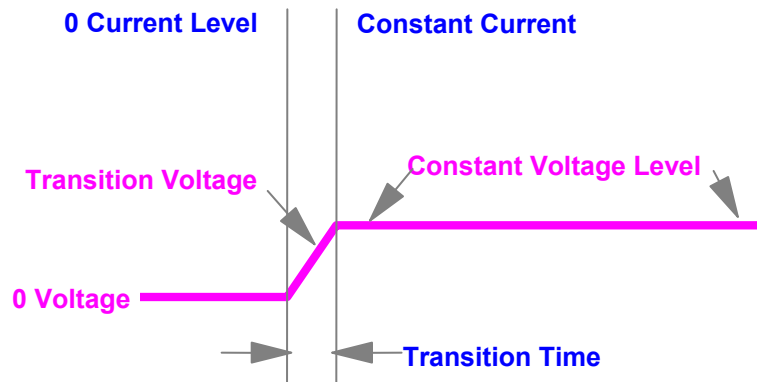




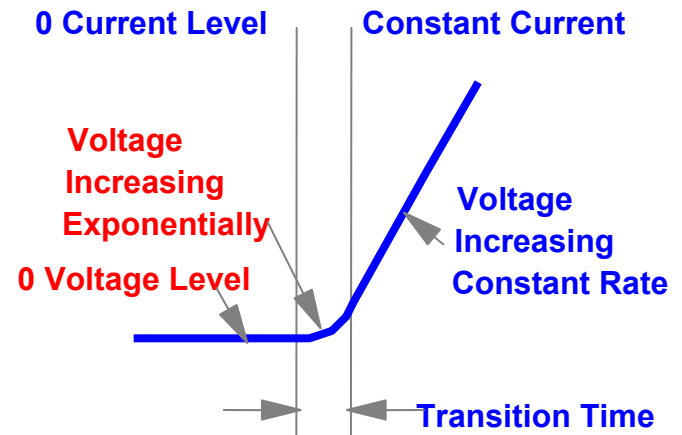
**Most equipment measures phase and amplitude resultants from sinusoidal source.**



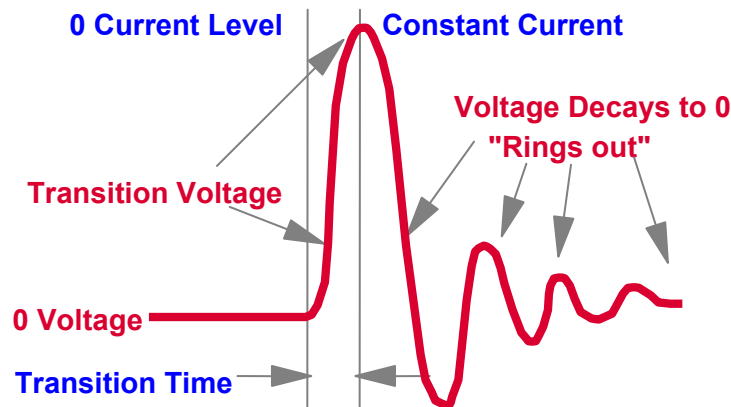
## Pure Resistor



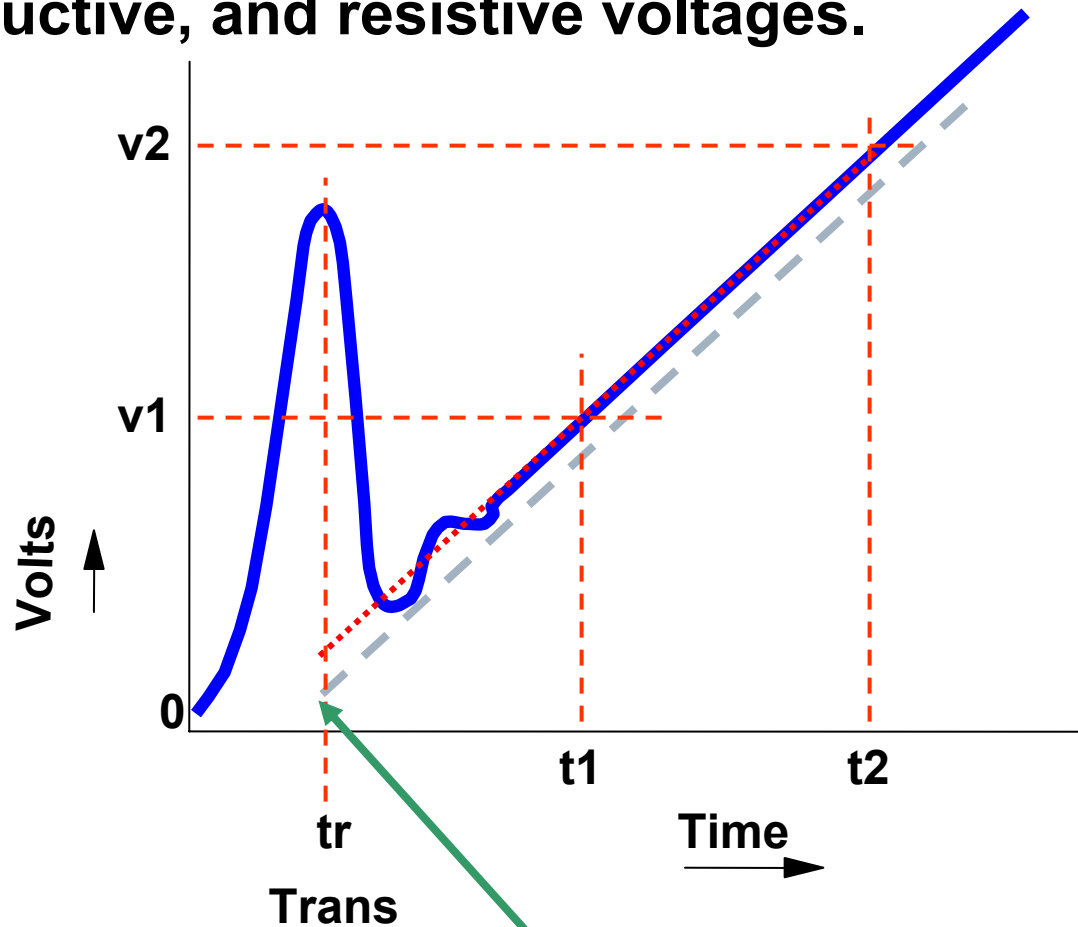
## Pure Capacitor



## Pure Inductor



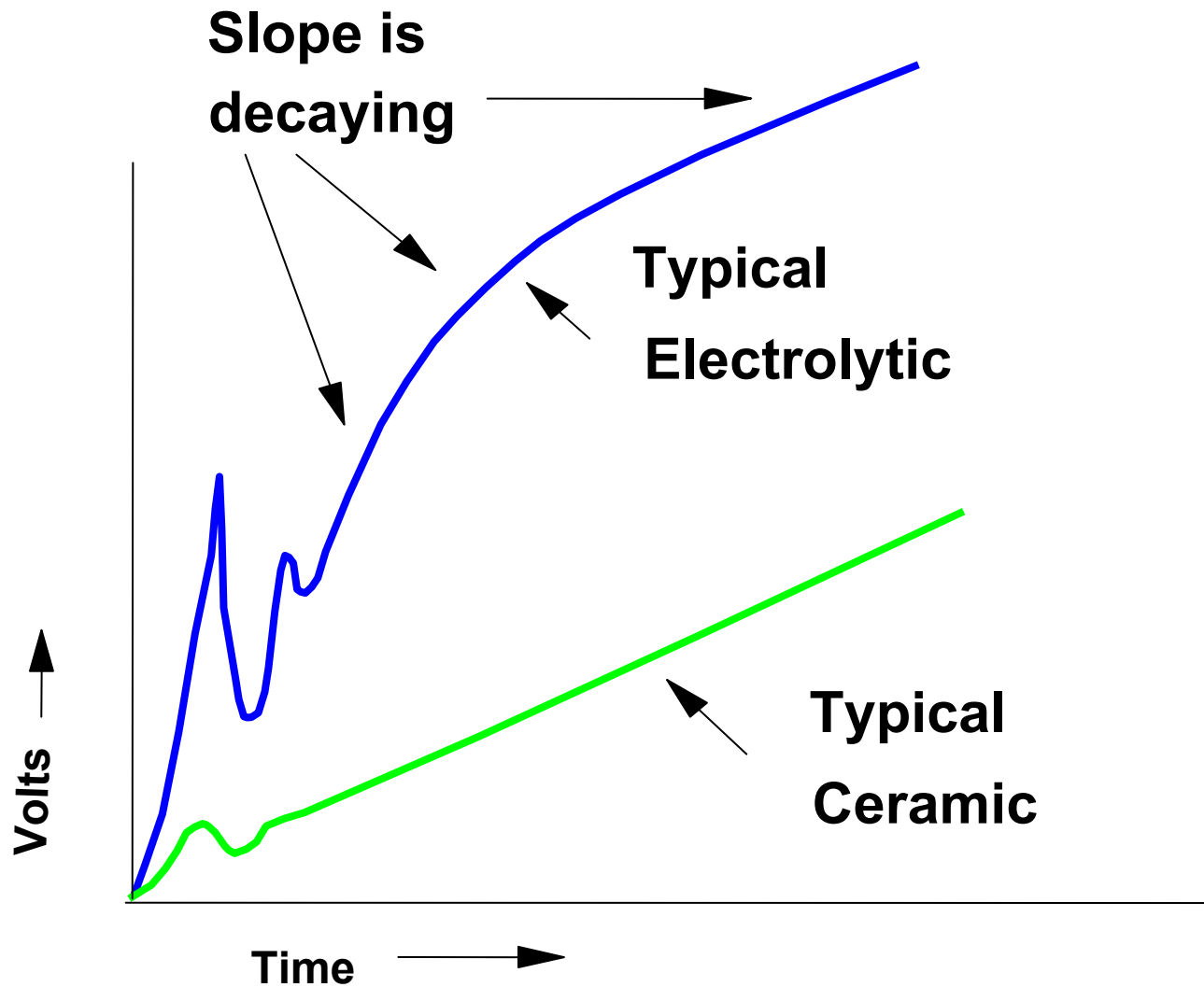
Pulse response is complex, combining capacitive, inductive, and resistive voltages.



$$C = \frac{I_{Constant} \times (t2 - t1)}{(v2 - v1)}$$

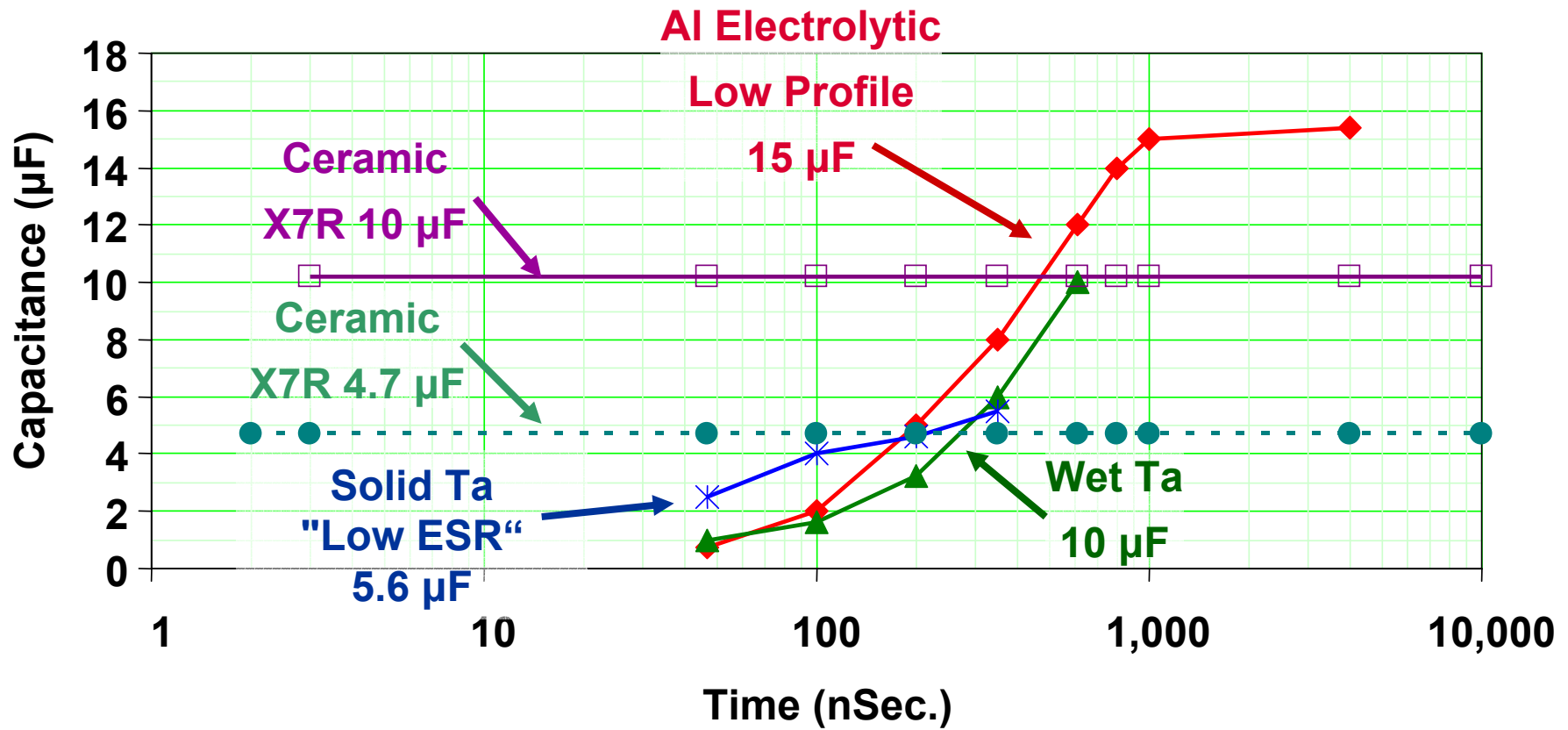
$$V_{C(tr)} = \frac{I_{Const}}{C} \times \frac{tr}{2}$$

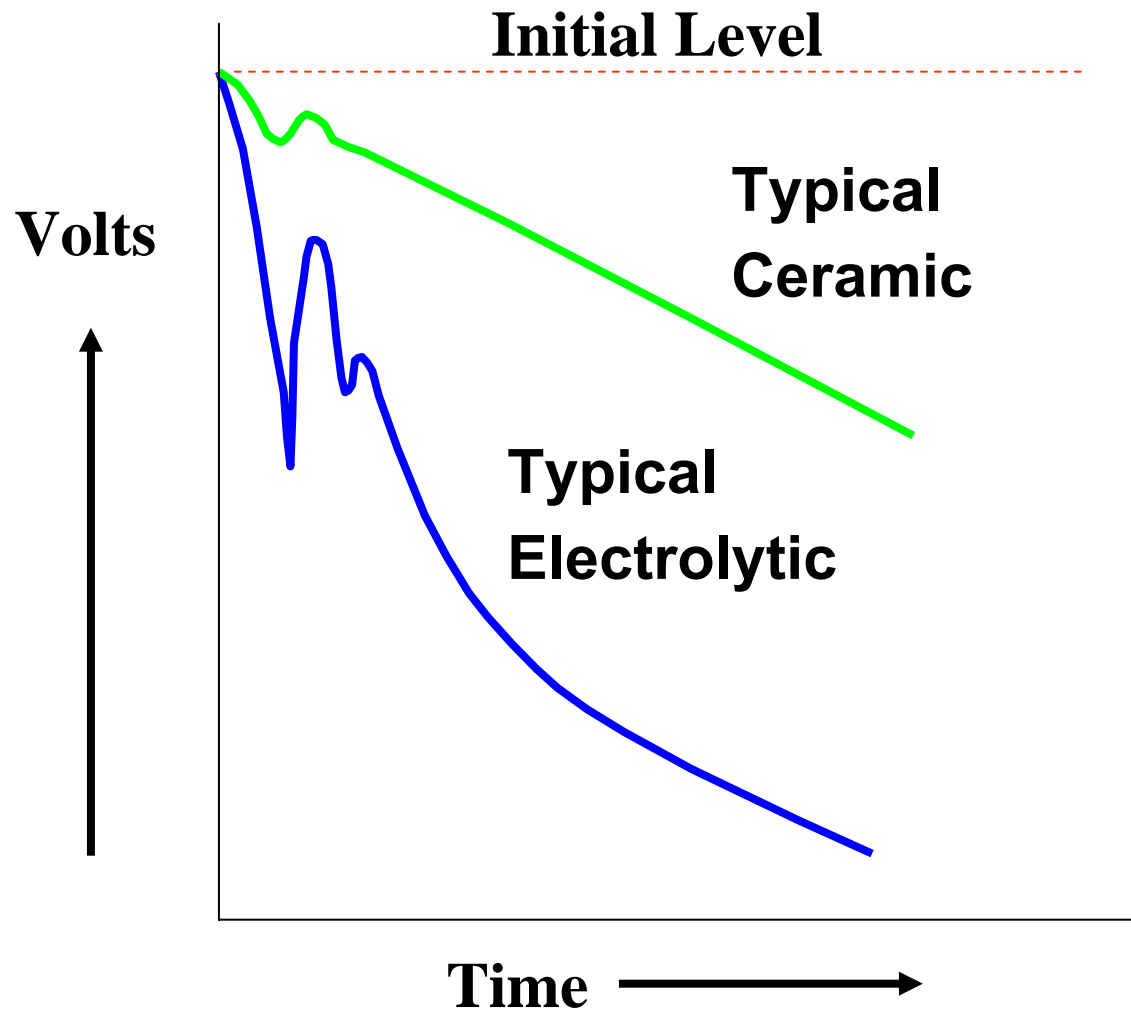
## Decaying Slope of Electrolytics

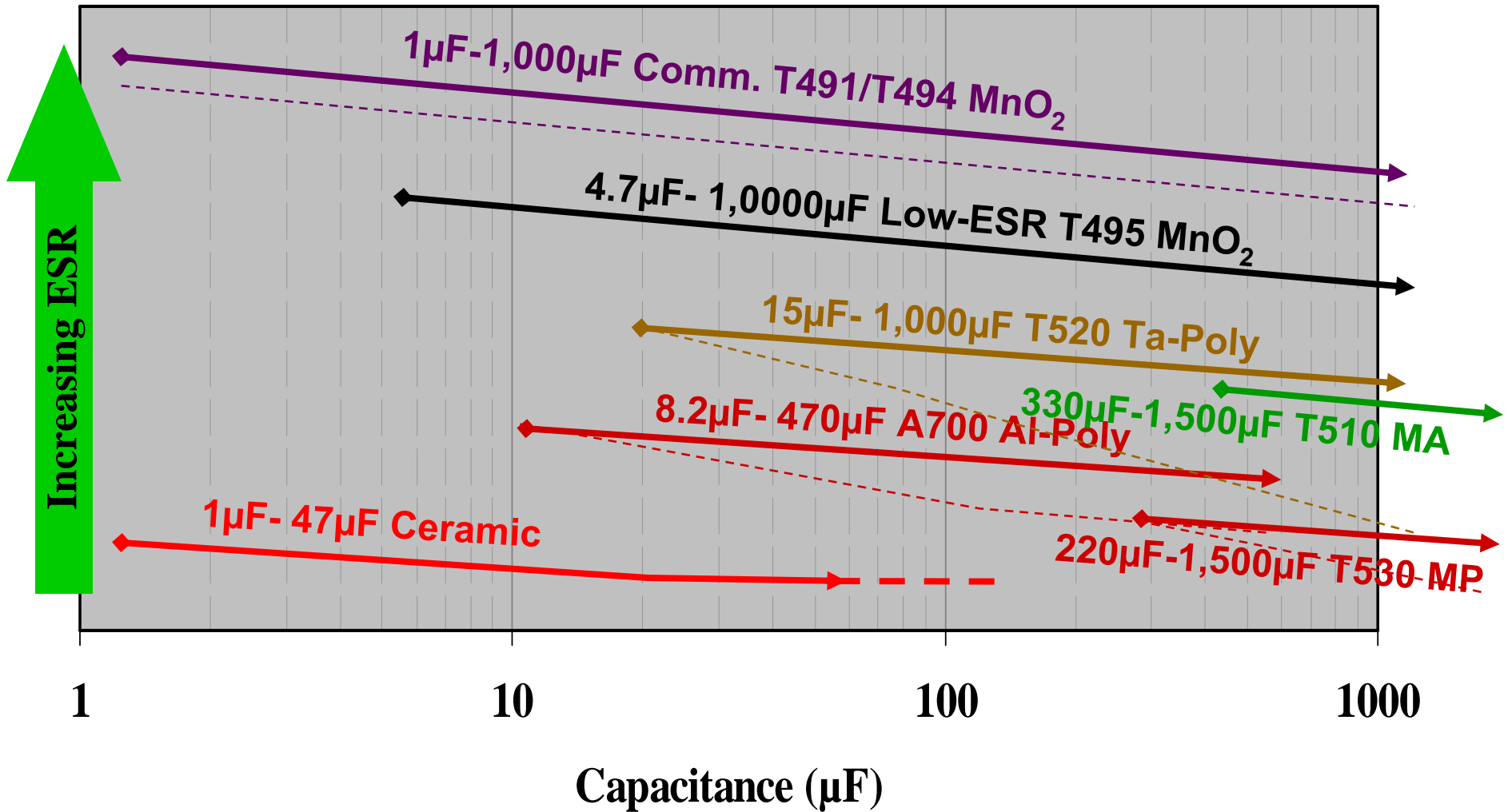




Capacitance vs. Time





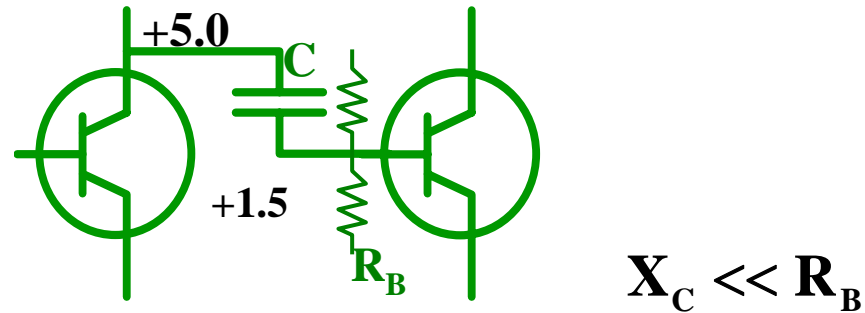


- **Power Applications**
- **Small Signal Processing**
  - (Decoupling, Bypass, Coupling)
- **Large Capacitance**
  - (Power Entry, low Current Hold-Up, low Frequency Bypass)
- **Small Capacitance**
  - High Freq., High Current (Oscillator, High Frequency Bypass)
- **Aluminum**
- **Film, Ceramic**
- **Tantalum**
- **Film**

- **Decoupling**
- **Filtering**
- Coupling
- Timing / Wave Shaping
- Oscillating

One of the first characteristics of capacitors:

*The capacitor allows an AC signal to pass, but stops DC.*

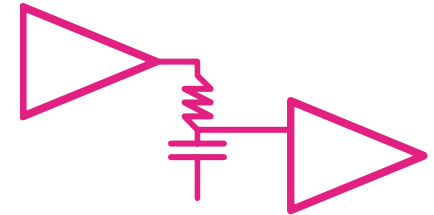


- Requirements
  - May have to handle wide frequency range
  - Must not cause large, unexpected phase shifts
  - May have to handle large currents
  - Capacitance stability not critical
  - Noise from capacitor critical

**By utilizing an exaggerated RC charge scheme, the subsequent functioning of a succeeding circuit can be manipulated to a controlled delay function of the RC constant.**

**Common experience can be found with:**

- **Vertical Sweep circuits in TV and computer monitors**
- **Delay wipers in automobiles**
- **Here the resistor is varied to allow the cap to charge quickly or at a slow rate**



**Timing circuits require fairly stable components. Many timing circuits are being replaced with digital counters.**

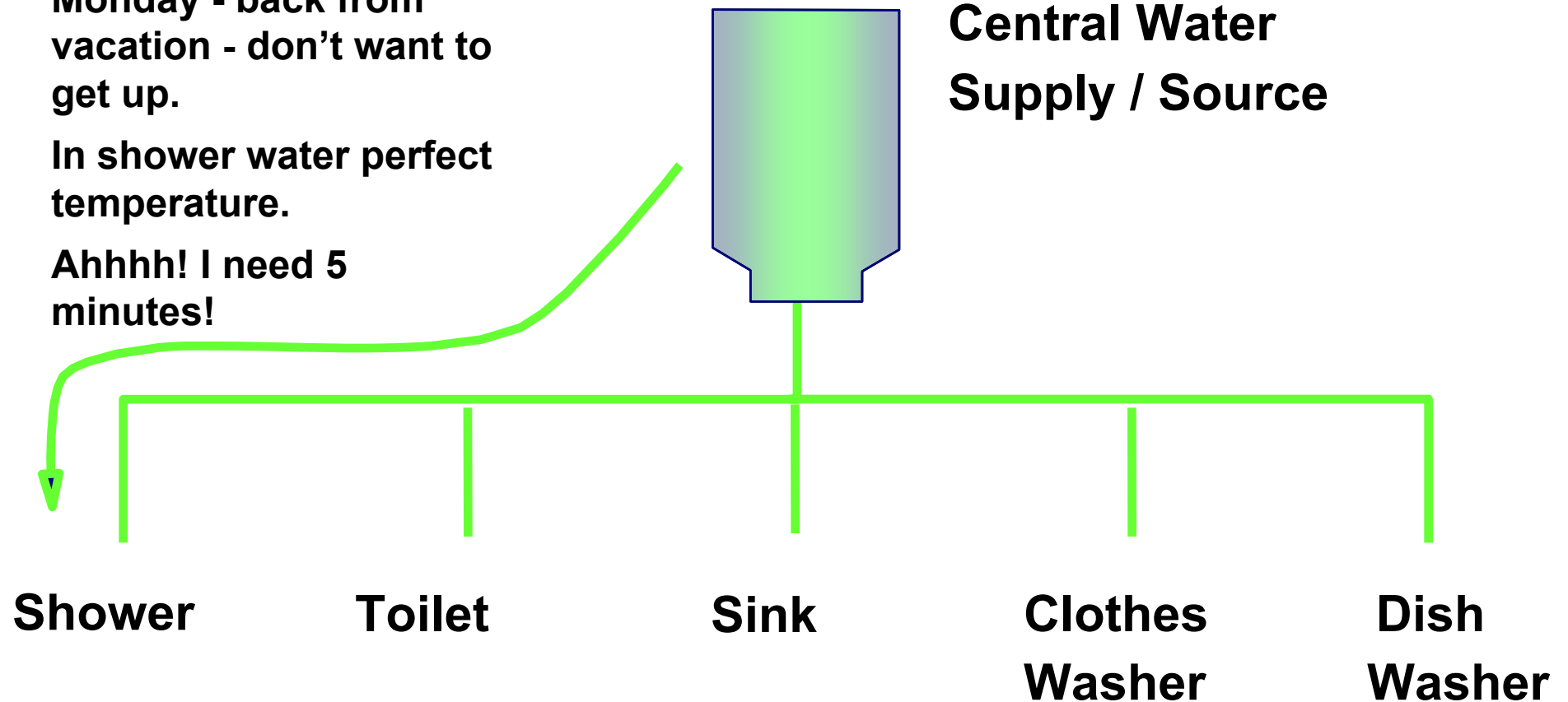
**Trying to satisfy all needs from a central-sourcing location**

**Monday - back from vacation - don't want to get up.**

**In shower water perfect temperature.**

**Ahhhh! I need 5 minutes!**

**Central Water Supply / Source**



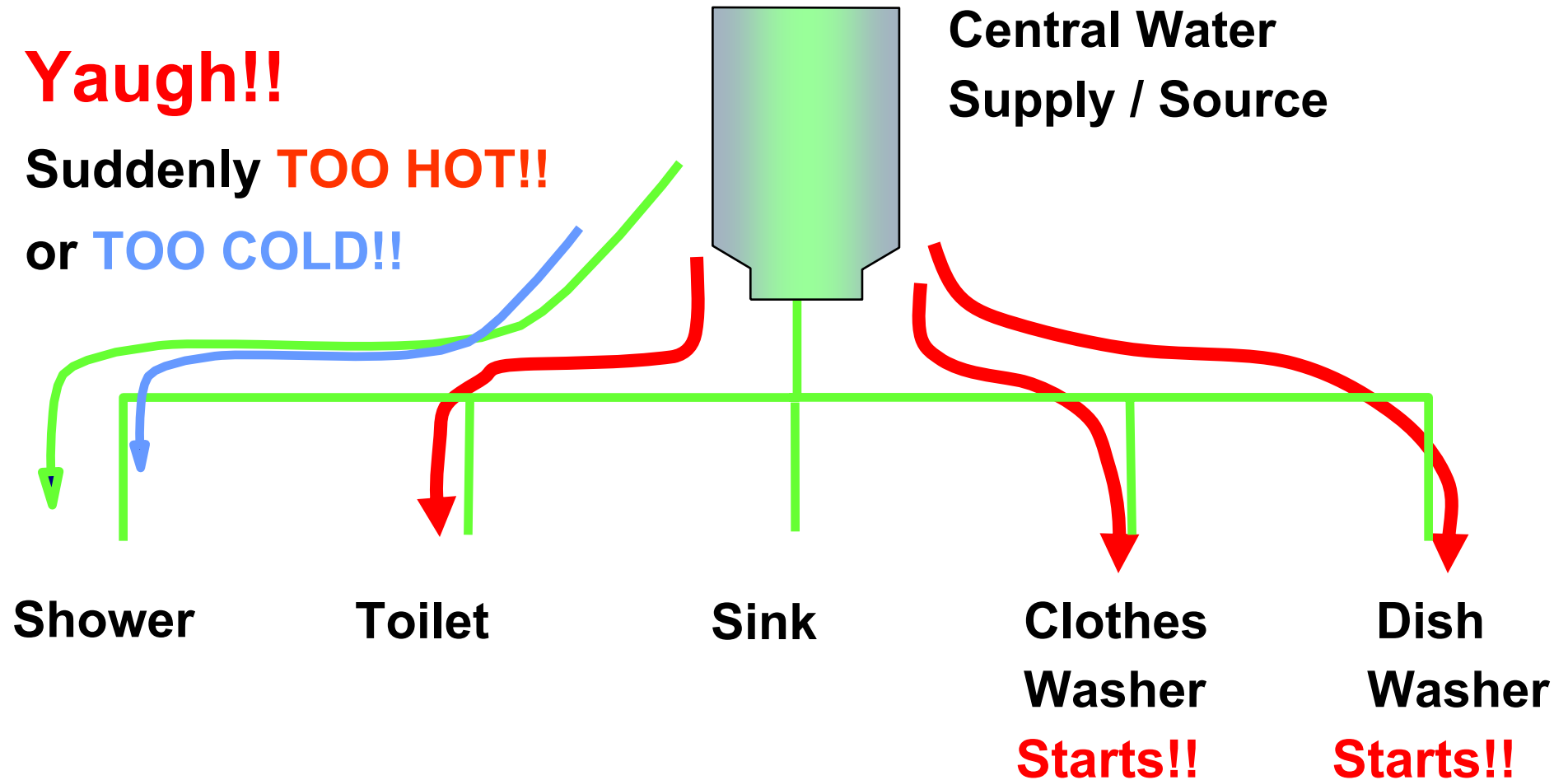


Suddenly a disturbance!

Someone (devilish), sleepy eyed flushes the toilet!

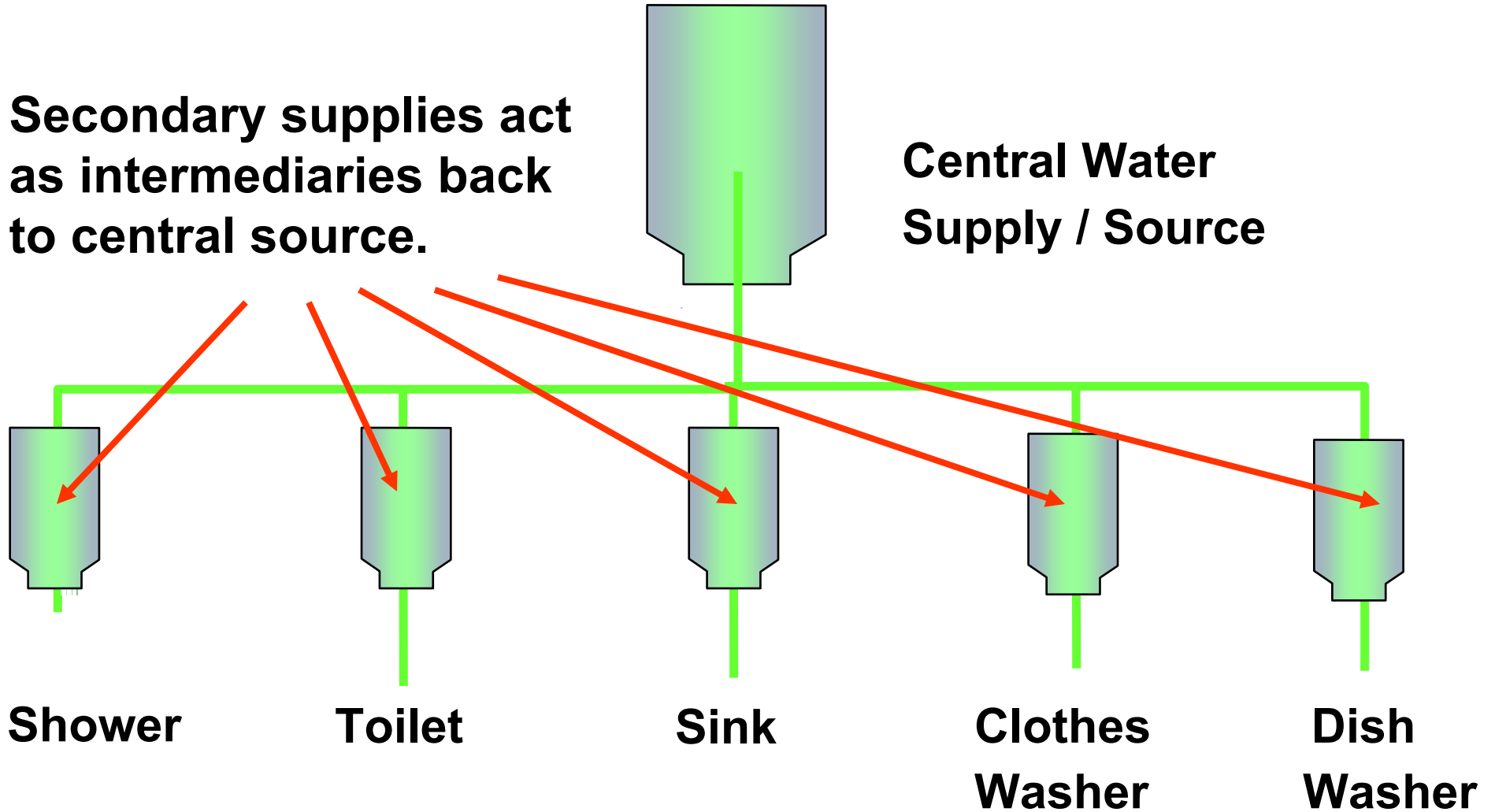
**Yaugh!!**

Suddenly **TOO HOT!!**  
or **TOO COLD!!**



**Secondary supplies act as intermediaries back to central source.**

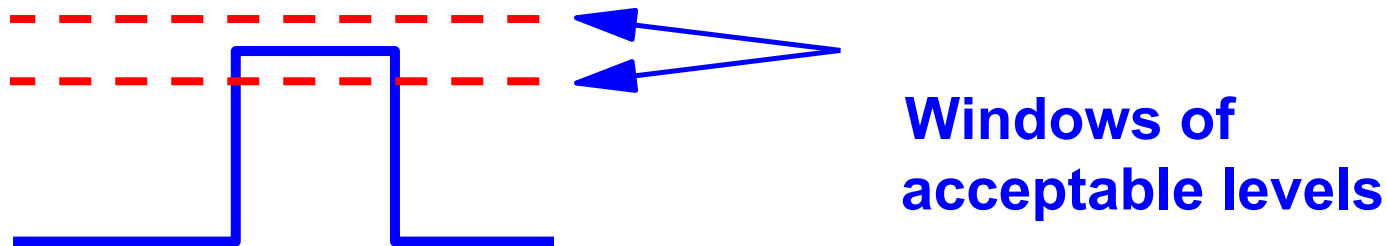
**Central Water Supply / Source**



## Water decoupling in Taipei



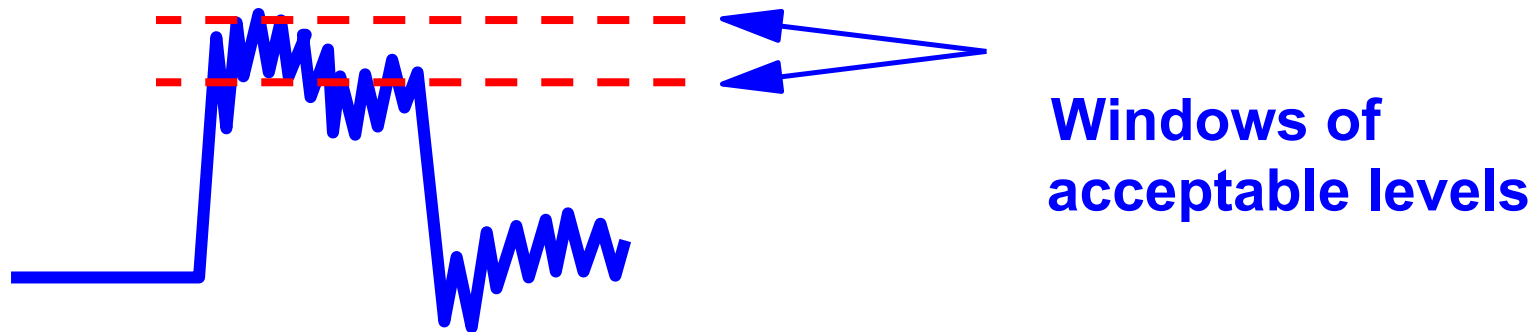
## Related to digital logic circuits



Binary logic allows for a high-low state, true-false, +V-0, that relate to voltage levels. One level is tested for – the absence assumes the alternative.

- ◆ Within the windows of acceptable levels, interpretation is 100% correct.
- ◆ Outside these windows, and the error rate increases - hardware induced errors.

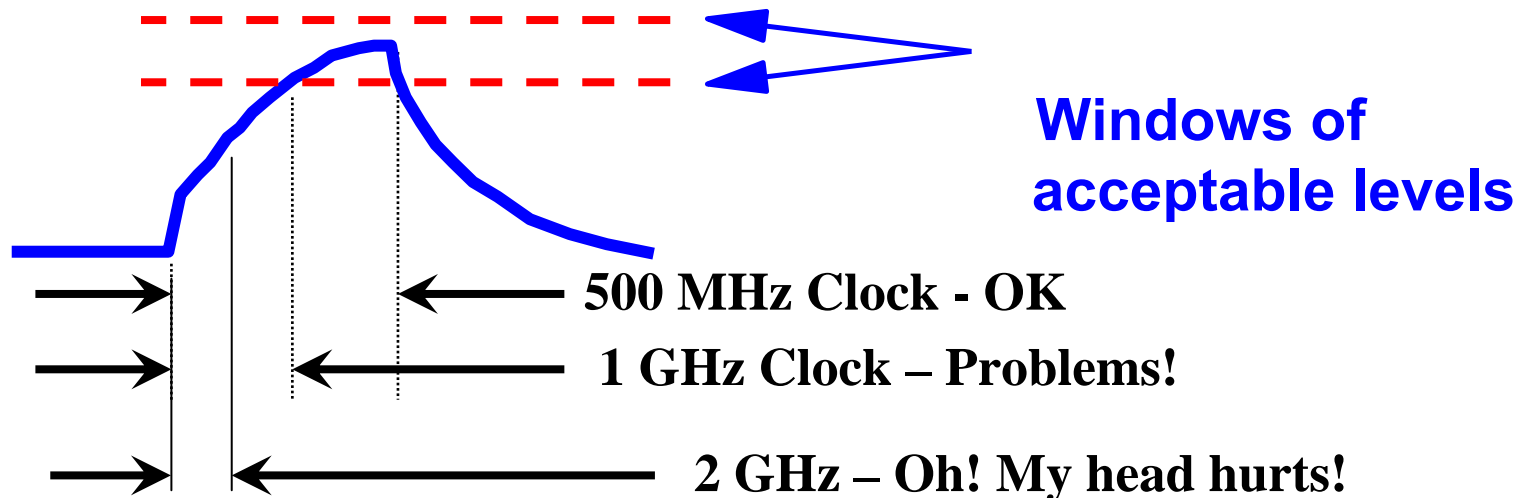
## Related to digital logic circuits



High frequency noise on the bus voltage may cause an error in the read state as it bounces in and out of the 100% "window of acceptable" limits.

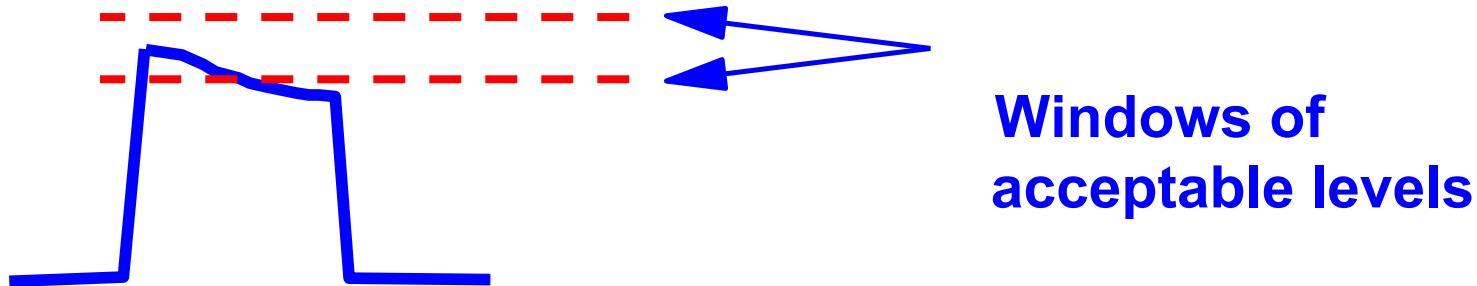
- Noise is generated by inductive elements within the traces as well as the IC and the capacitor.
- Multi-plane boards have greatly reduced external inductance, but have not eliminated it.

## Related to digital logic circuits

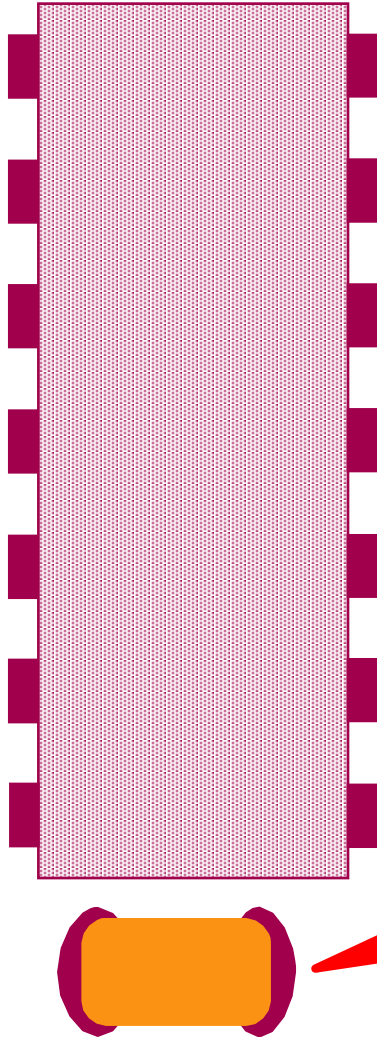


**Resistive elements also contribute to a delay in transmission. These elements could be in the power source to the board and contribute to a general lowering of the bus levels.**

## Related to digital logic circuits



**"Droop" occurs when the bus can not be held at the desired level when a multitude of devices are being switch on simultaneously. Overall capacitance needs to be increased.**

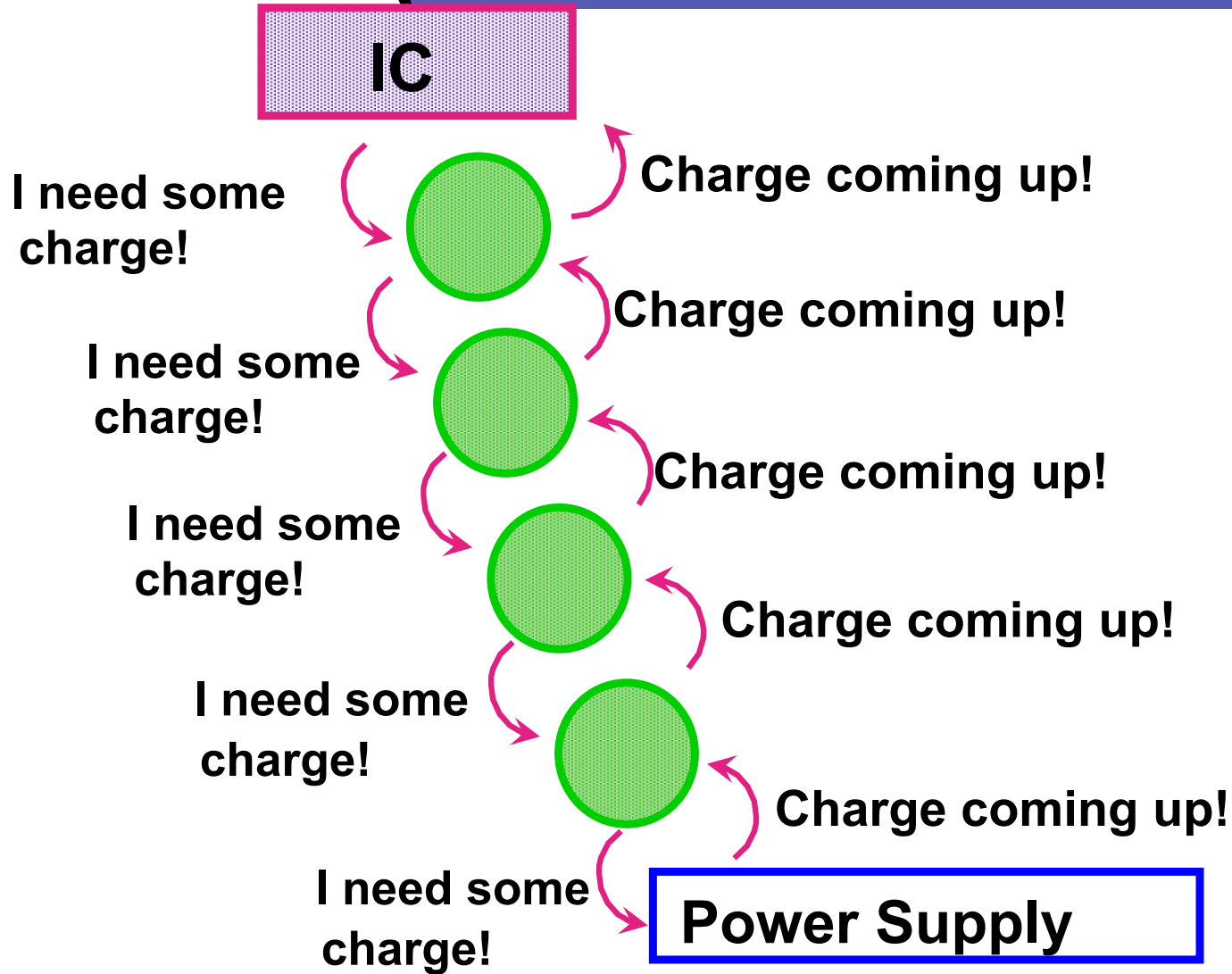


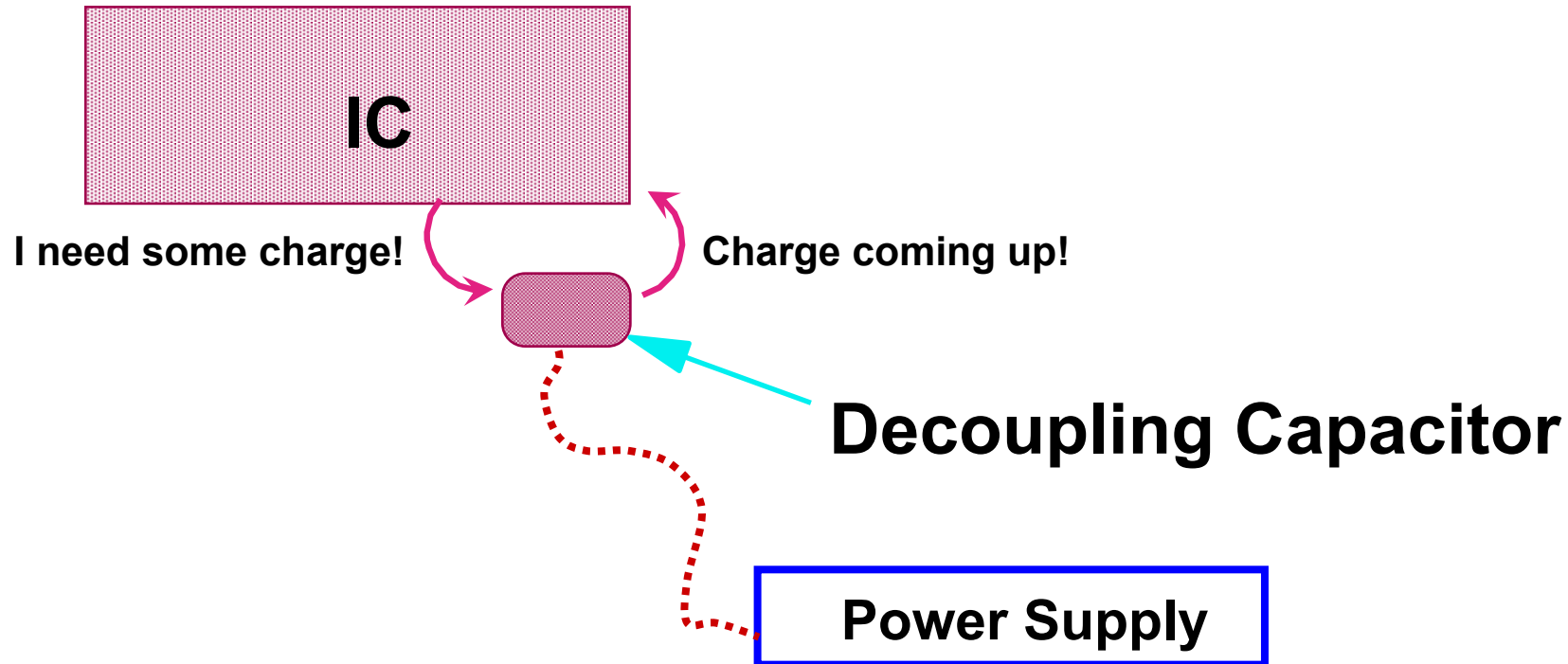
**Next to each and every IC,  
a capacitor is mounted.**

**The capacitor acts as an  
energy reservoir, that can  
replenish the IC thirst for  
a quick burst of joules.**



No decoupling creates delay





**Decoupling capacitor should be able to pass multiple energy bursts to IC without appreciable loss of voltage.**



## Decoupling is a hand-me-down system

⊕ The small capacitor next to the IC needs replenishments.

⊕ The larger capacitor located at interspersed locations on the board, feed the smaller.

⊕ Larger power entry capacitors located near the bus feed supply the previous group.

⊕ The filter capacitors feed the power entry capacitors.

**Filtering can have two distinctive functions that both remove unwanted signal or line variations:**

➤ **Frequency Selective Filtering**

- A low pass, high pass, or band pass configuration
- Most often used application is high frequency by-pass

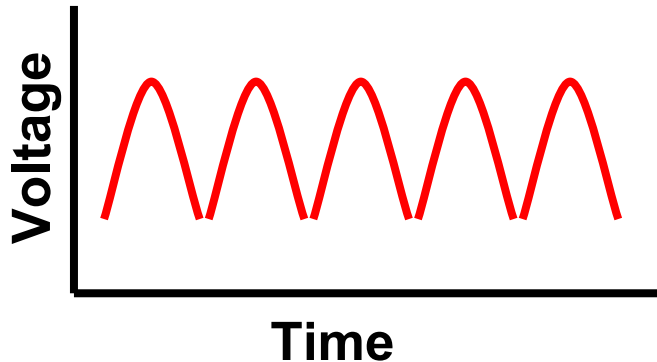
➤ **Rectified AC Smoothing**

- Eliminates the pulsing from low to peak by alternately absorbing energy during the peaks, and releasing it during the valleys.

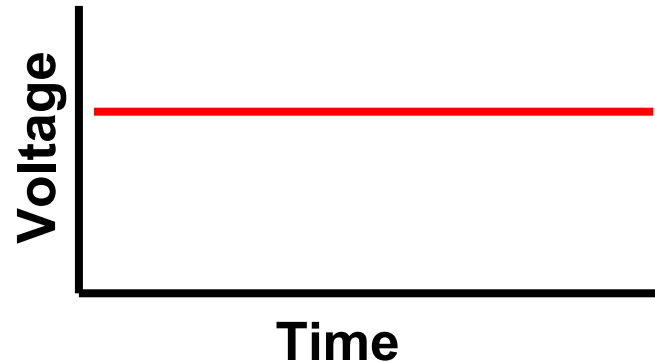


**As frequency increases, more of the signal chooses the alternative path, less goes to the load.**

**A variation of this circuit will allow only the higher frequencies to go to the load as the lower frequencies are channeled around it.**



*Voltage is pulsing with time*



*Voltage is steady with time*

**Capacitor charges as voltage attempts to go high, and discharges as voltage attempts to go low.**

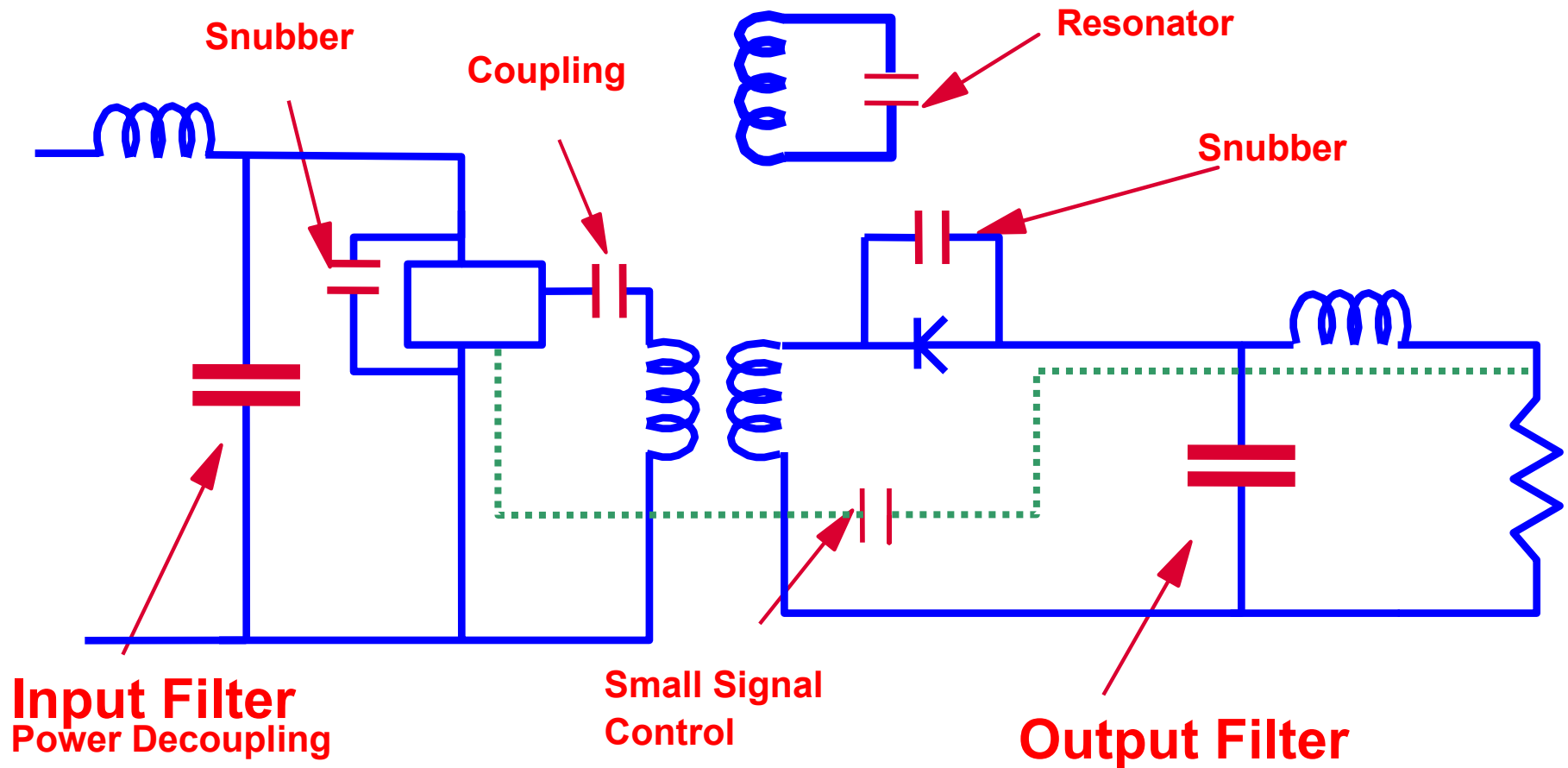
**Capacitance value is high as it must stabilize this voltage and feed current to circuit during discharge**

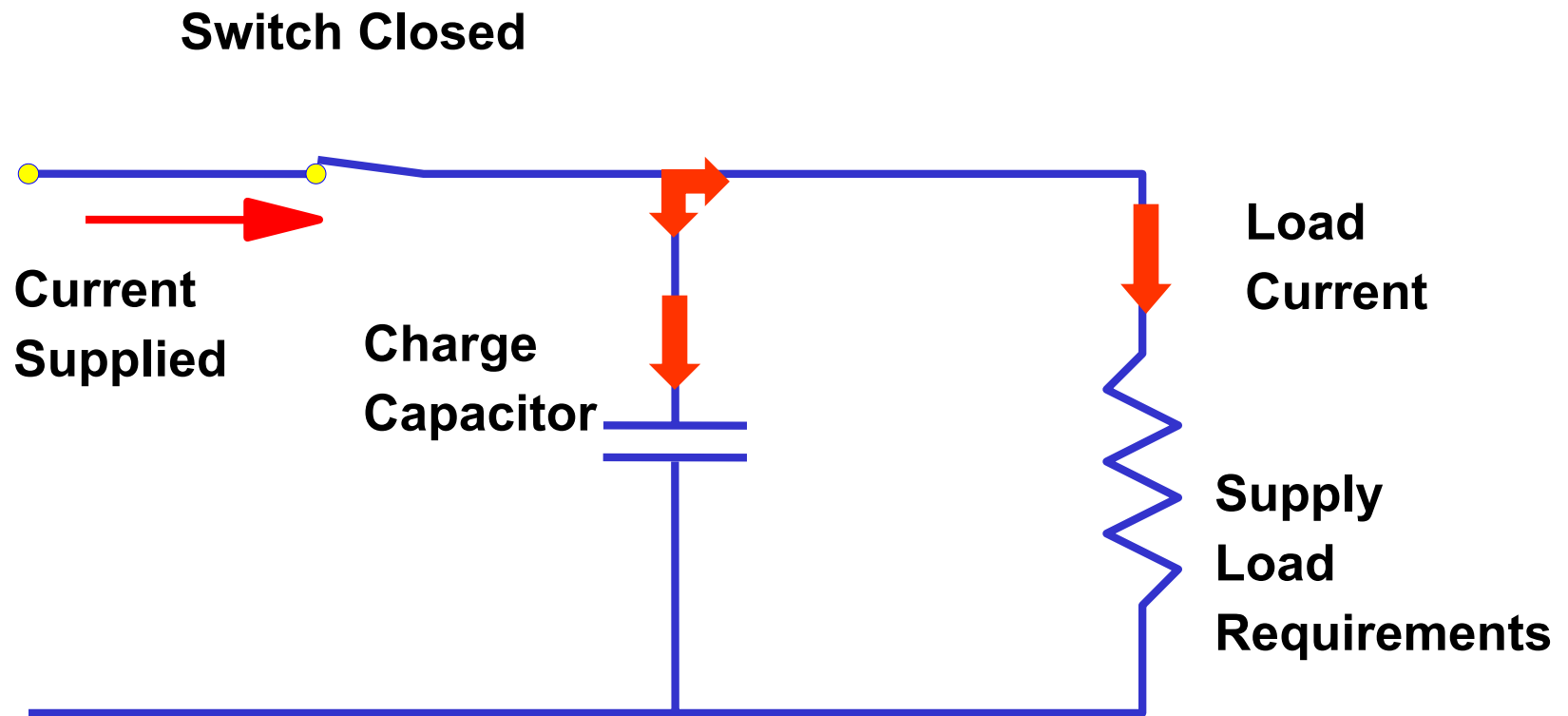
**High ripple currents!!**

**ESR is of critical importance (ripple voltage & heat - efficiency)**

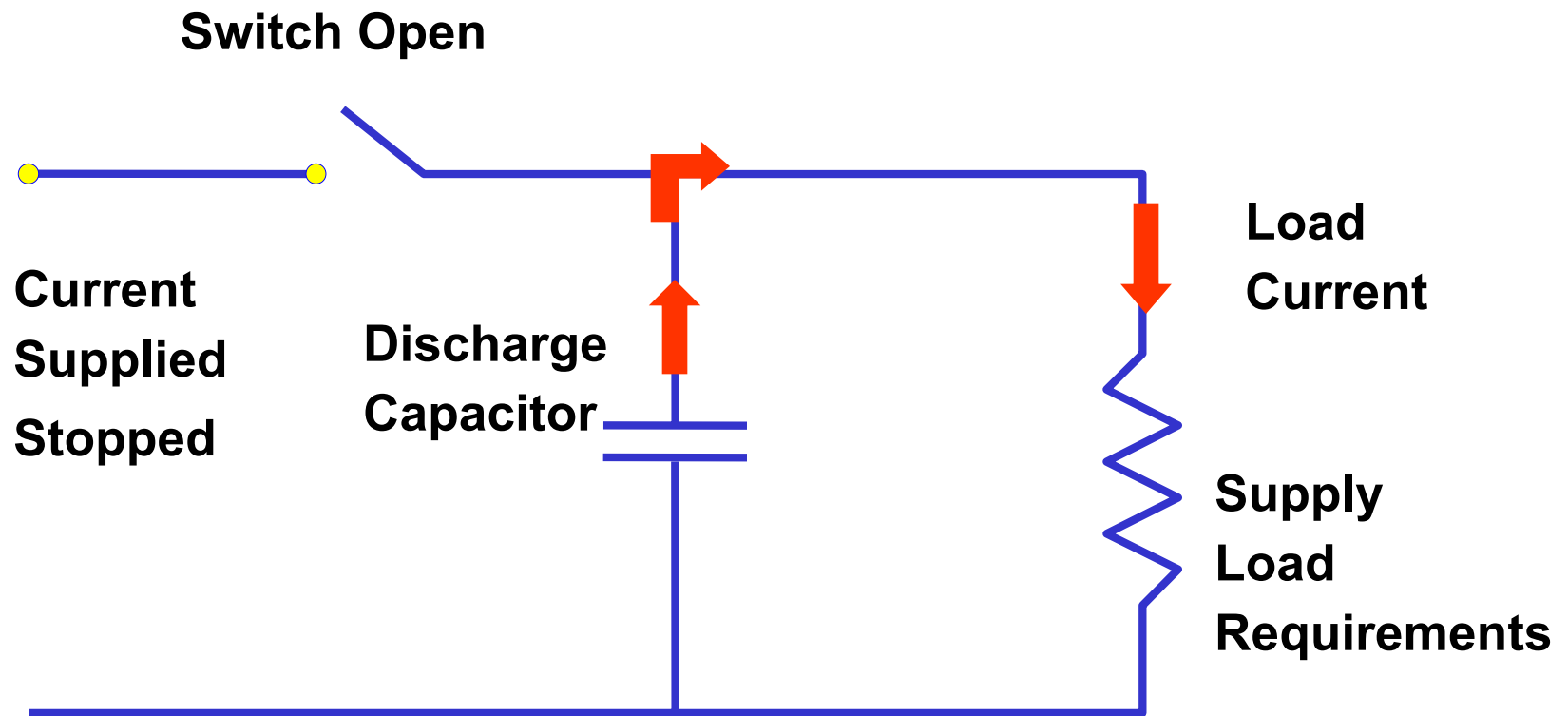
**Capacitance stabilization acceptable for  $\pm 20\%$  variations.**

# Capacitor Usage



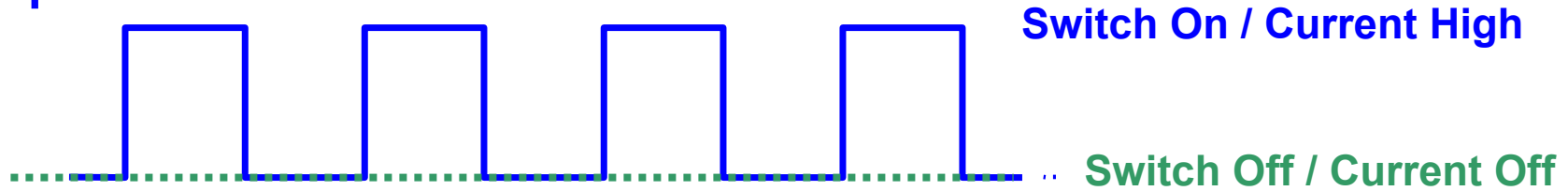




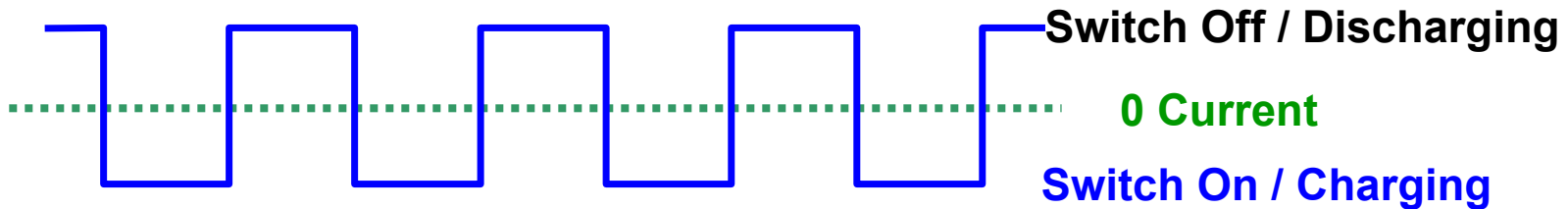


# SMPS Timing Diagram - Full Power

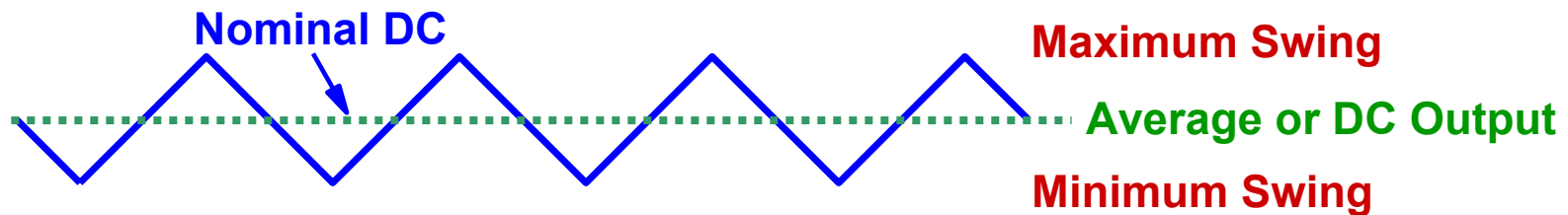
**Input Current**



**Capacitor Current**



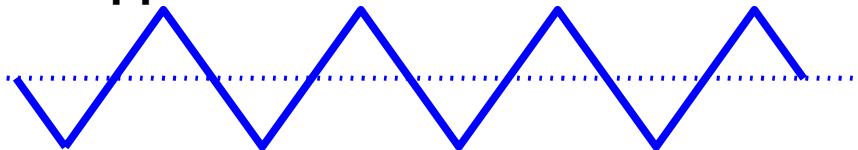
**Capacitor Voltage / Load Voltage / "RIPPLE"**



**The magnitude of the ripple is inversely proportional to the magnitude of the capacitance or the RC time constant.**

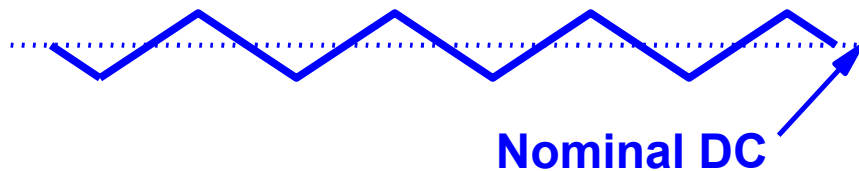
**If the load is kept constant and the ESR is ignored, then the amount of voltage the capacitor discharges to, is inversely proportional to the capacitance.**

**Higher ripple**



**Lower capacitance - lower RC time constant, or the more discharge in given time period.**

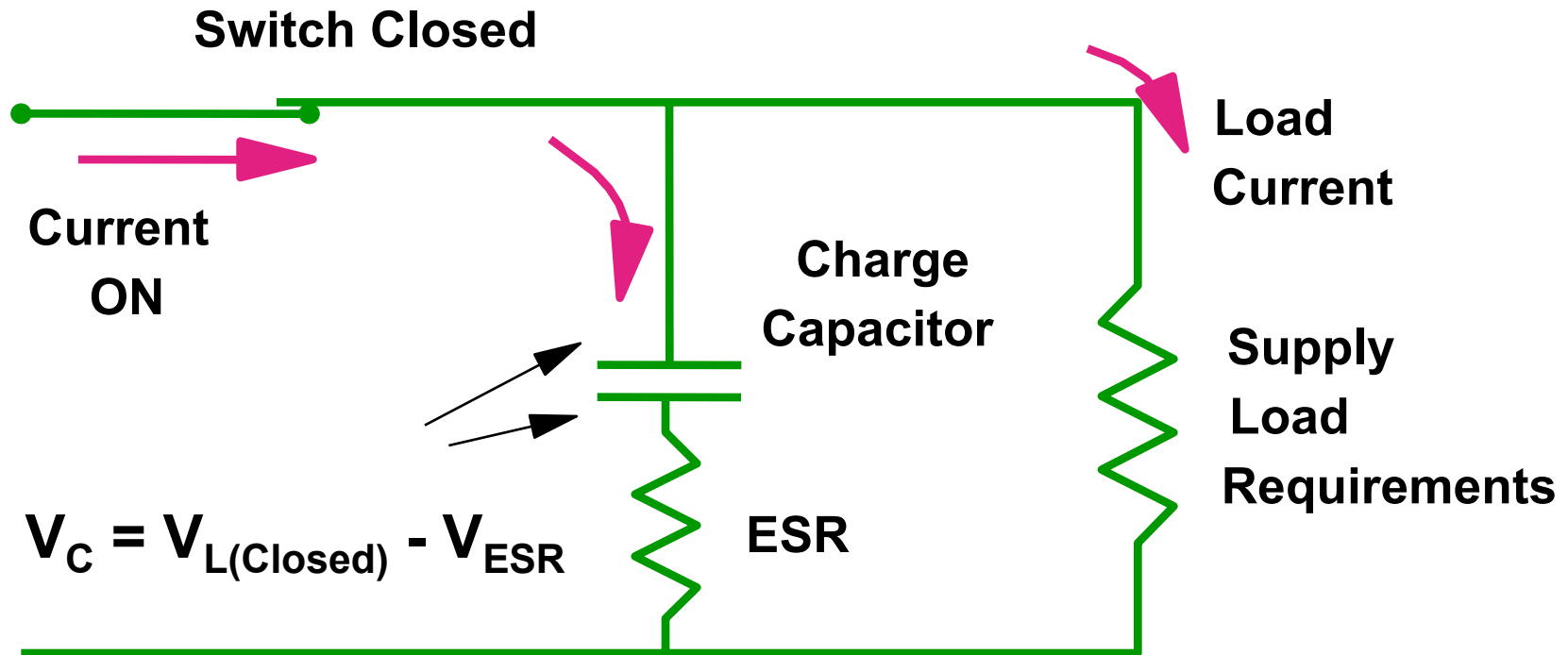
**Lower ripple**



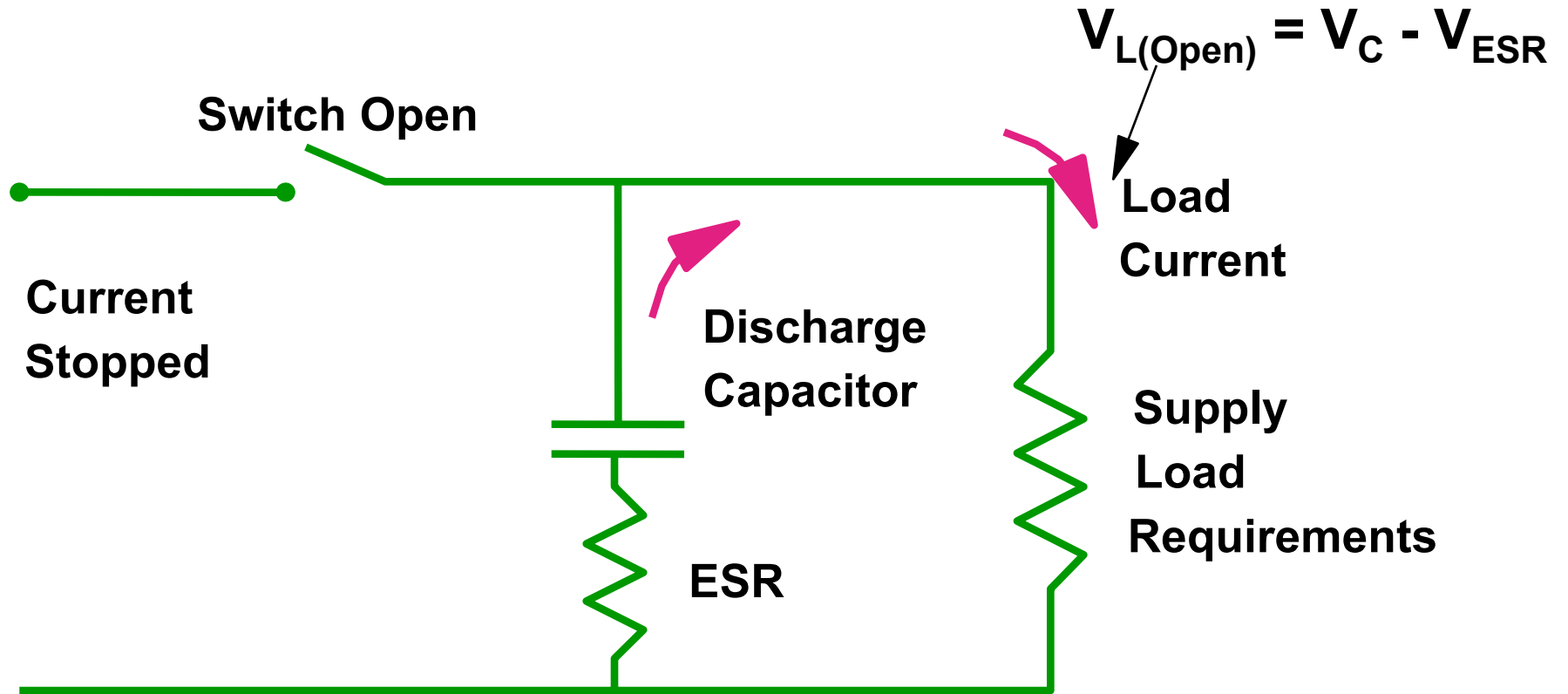
**Higher capacitance - longer RC time constant, or the lower discharge in given time period.**

**Nominal DC**

# ESR Inhibits Capacitor Charge

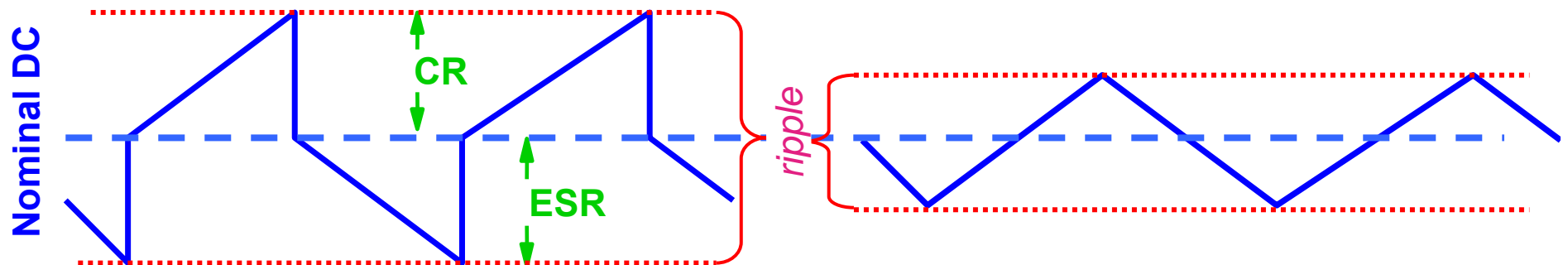


# ESR Robs Capacitor Discharge



The magnitude (peak-to-peak) of the ripple is proportional to the magnitude of the ESR above a critical level.

If the capacitance and load are kept constant and the ESR is increased, then the amount of voltage the capacitor charges to is a step less than the peak voltage noted during the "on cycle".



**High ESR ripple**

**High ESR - capacitor not charged, to continue voltage drops to lower level then discharges.**

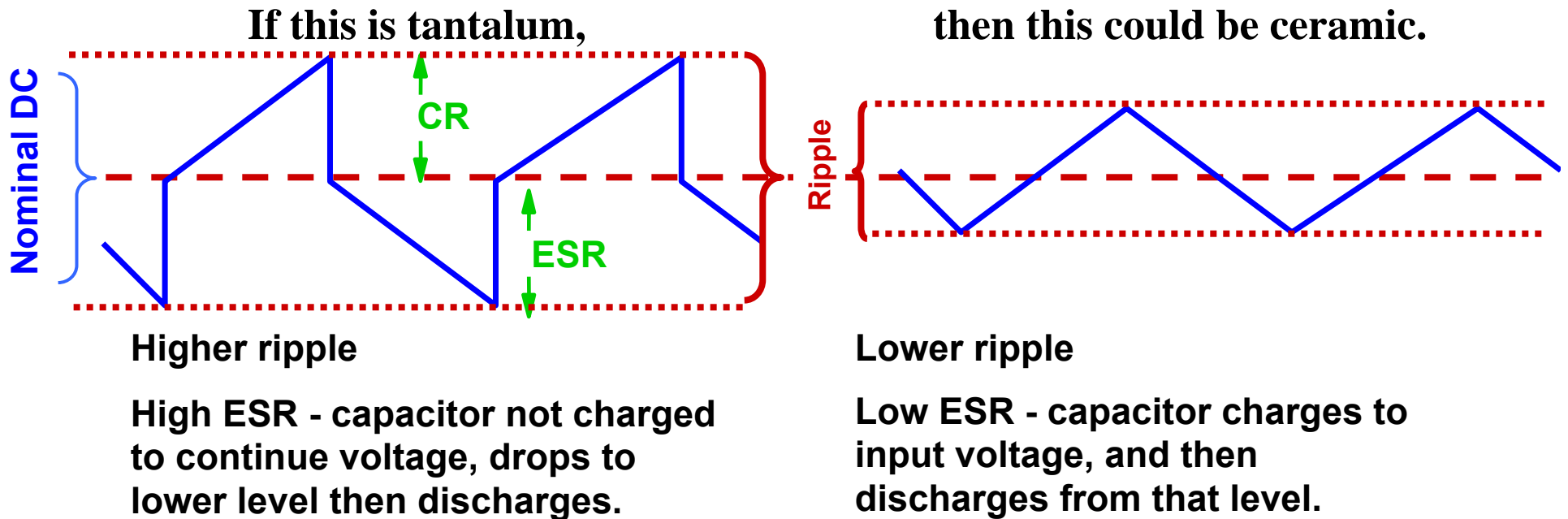
**Low ESR ripple**

**Low ESR - capacitor charges to input voltage, and then discharges from that level.**

at Room Temperature (~20°C)

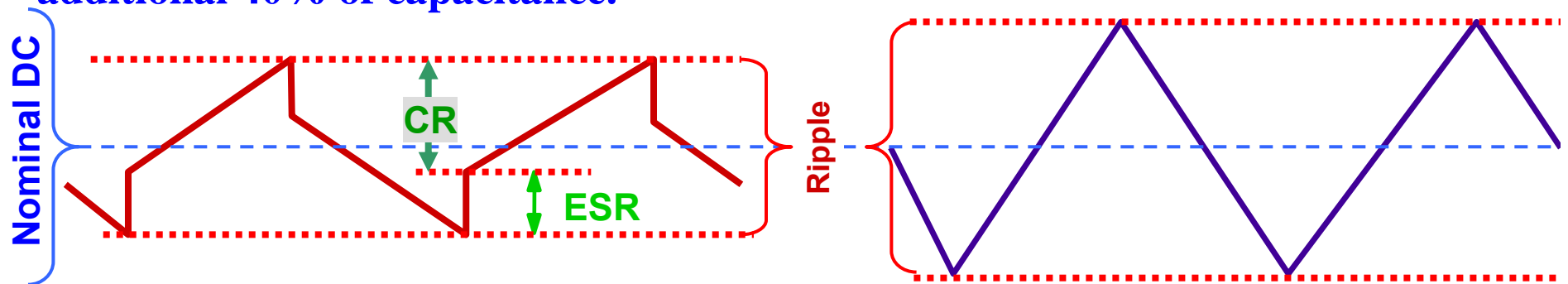
Based on *'measured'* values

If the capacitance and load are kept constant and the ESR step voltage adds to the overall ripple effect at room temperature, and the DC bias on the ceramic capacitor is low in relation to its rating : CR ripple slopes are equal & difference is ESR step voltage.



at DC Power & Temperature (~60°C)  
(Application Response)

The ESR step voltage for the tantalum decreases as ESR decreases with increasing temperature. The capacitance of the ceramic decreases with increasing temperature causing the CR - ripple to increase. If the bias is increased to 33% of rated from 10% of rated, the ceramic capacitor loses an additional 40% of capacitance.



Lower ripple (Tantalum)

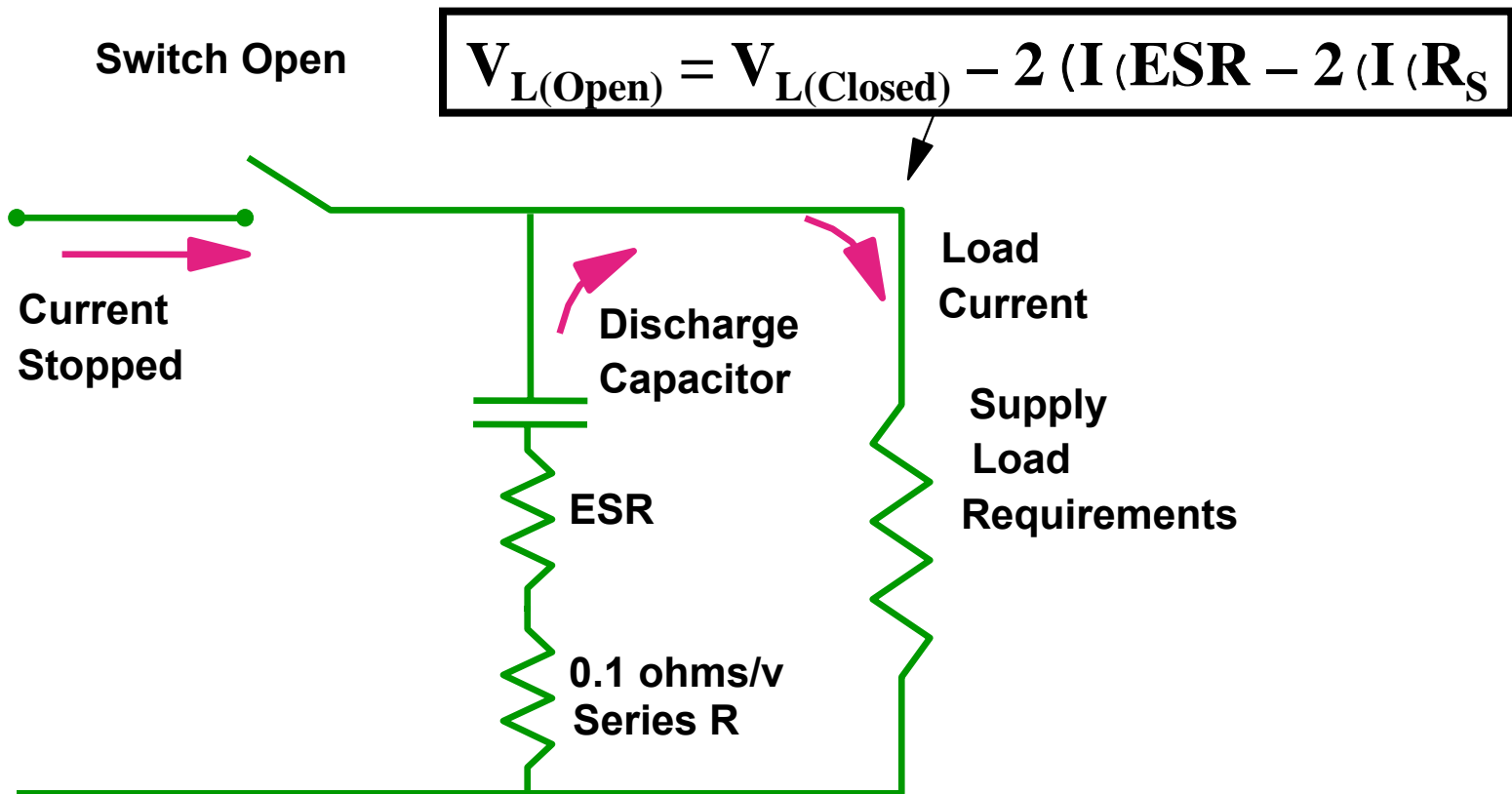
ESR step voltage decreases with increasing temperature, while CR ripple remains the same.

Higher ripple (MLC)

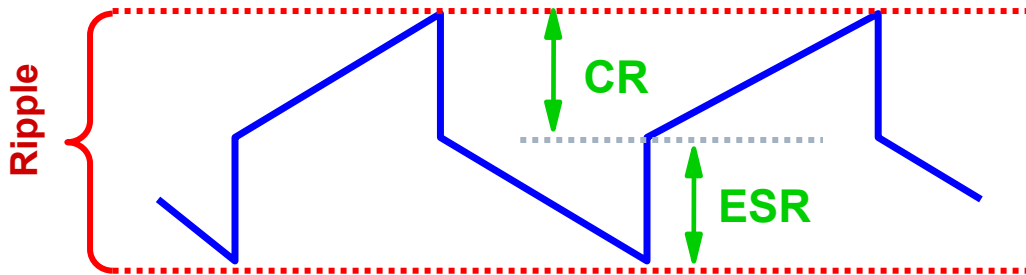
Lower ESR offers no advantage, lower capacitance because of bias and temperature causes increase in CR ripple.



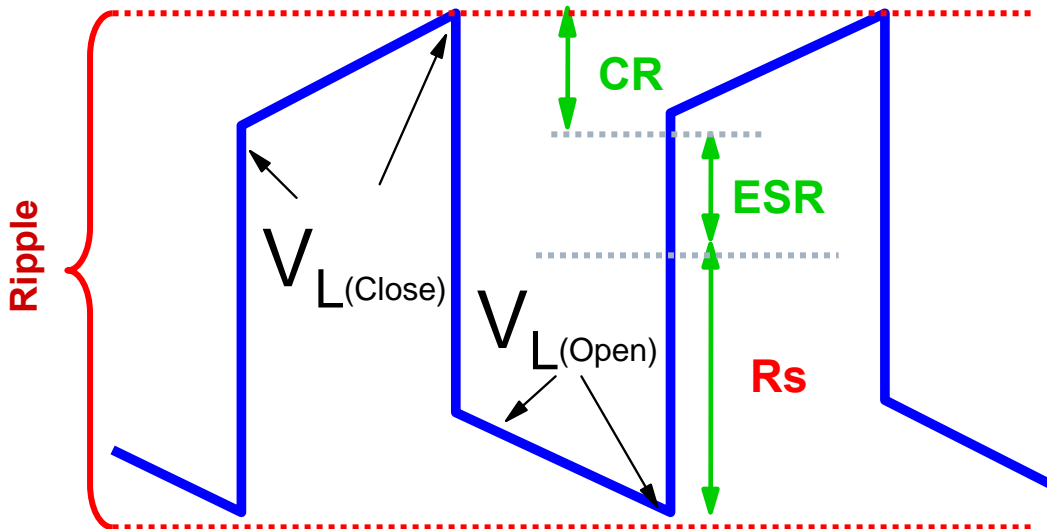
For commercial tantalum chips, required series resistance appears as additional ESR.



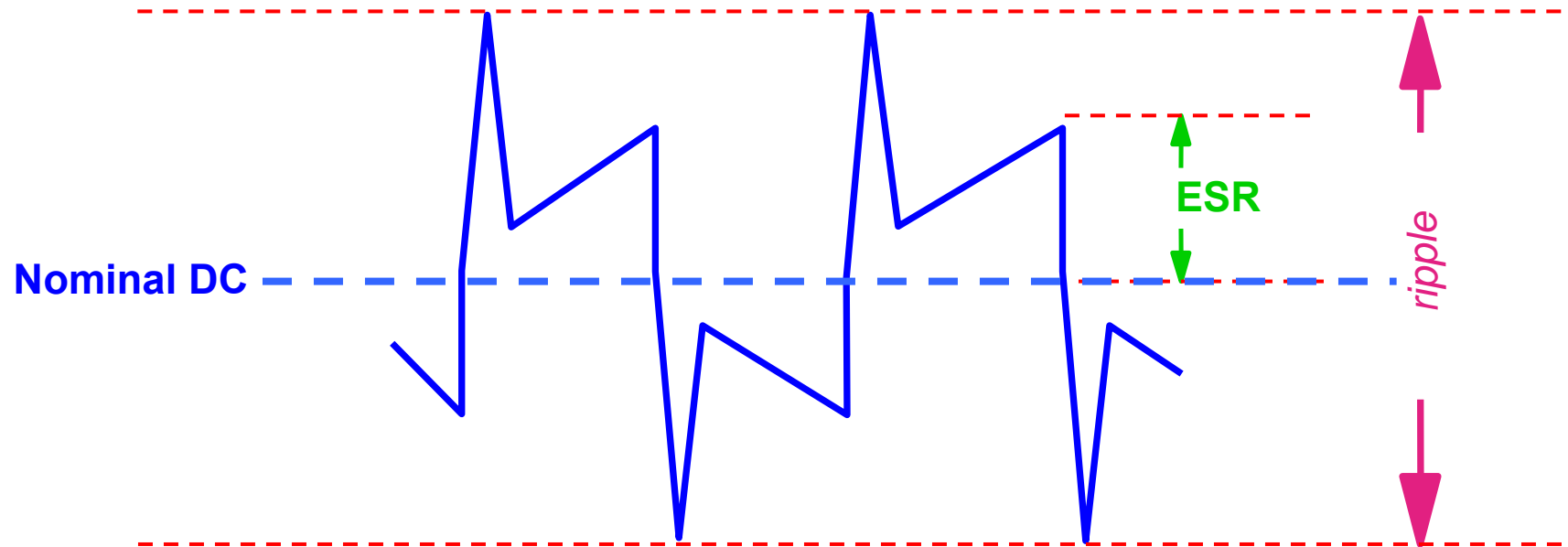
The magnitude (peak-to-peak) of the ripple is proportional to the **Summary ESR** and  $R_s$ .



T495, T5xx, A7xx  
Recommended Series  
 $R_s = 0$

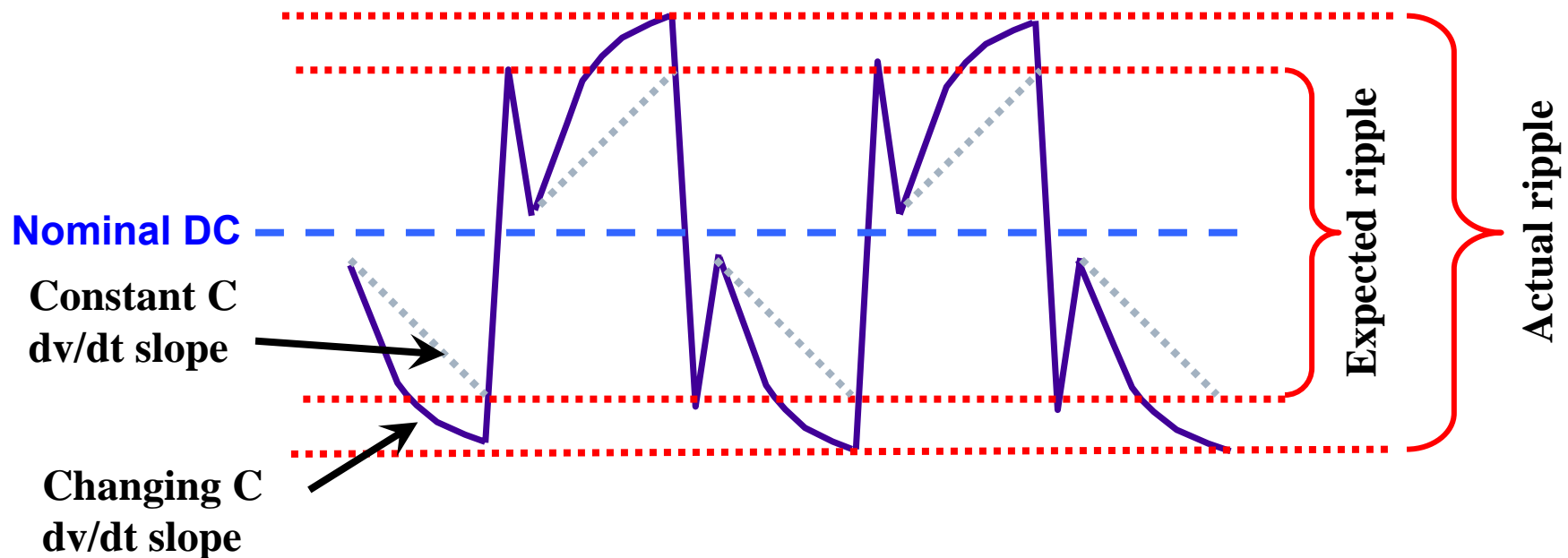


T491/T494  
Recommended Series  
 $R_s = 0.1$  ohms/volt



**Magnitude of inductive pulse is proportional to magnitude of ESL, and to the magnitude of the current and proportional to the switching speed.**

$$V = L \times di/dt$$



**If capacitance (C) decreases with frequency (shorter periods), then CR ripple has high slope at beginning and slope decays until it achieves stability in lower frequencies (longer periods).**

