Power-On Failures in Tantalum and Aluminum SMT Capacitors

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Abstract: *There are forces exerted on these encapsulated components during the solder mount process that can extend existing failure sites or generate new failure sites within the components. These failure sites can lead to failures well below the test voltages that these devices were exposed to during their 100% electrical testing in manufacturing. These forces are mechanical in nature but thermally created as the package is exposed to the reflow solder conditions. Once the part is soldered to the board, it is the subsequent electrical testing that now defines the proof capability of the device. Failures are uncovered when the stress applied is equal to or greater than the new breakdown capability of the dielectric. Factors influencing the number of failures include the condition and capability of the dielectric in its post-manufactured state, as well as those conditions experienced in the customers' solder process.*

Surge Voltage vs. Surge Current

All KEMET surface mount tantalum capacitors are 100% electrically tested prior to packaging. These tests include measurements of capacitance, DF, ESR, and leakage. They are also surge volt tested to 1.32 times the rated voltage. With surge voltage testing, series resistance is added to the circuit to aid in the self-healing effects within these devices.

The larger case styles of C, D, and X, are also surge current tested to 75% of rated voltage for the commercial T491, T494, and T496 products, while the T495 and T5xx series are surge current tested to 100% of rated voltage. The circuit resistance goal for surge current testing is to have as little as possible. In this test, we maintain the resistance between 0.2 and 0.3 ohms.

Removing Weak Components

Then why do some customers see initial power-on failures at voltages well below these screening limits?

First, we need to define what is accomplished with surge voltage and surge current testing. KEMET defines these as two distinct conditions and these distinctions may not be maintained across manufacturers. With surge voltage testing, the series resistance limits the peak surge current deliverable to the part, and defines a delay in the charge time of the capacitor.

If a fault is uncovered in the dielectric as the stress is increasing, the restricted current may allow the self-healing to take place [1]. The MnO_2 cathode plate in contact with the fault site raises the temperature enough to convert to a much higher resistive compound such as Mn_2O_3 - thereby restricting the current and effectively eliminating the fault site from the capacitor circuit. Multiple scintillations (as shown in Figure 1) can occur at multiple sites of the dielectric throughout the capacitor, thereby restricting the peak voltage that the capacitor sees during this testing. A pause between scintillation occurrences and the leakage may appear to be normal.
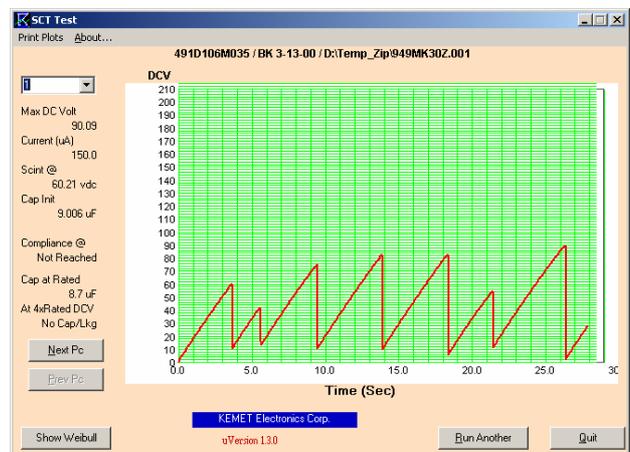
Figure 1. Multiple scintillations in tantalum capacitor. [1]

Leakage testing, also accomplished through an appreciable series resistance, is a one-time reading – if scintillations occur well before reading, no apparent fault is detected.

Surge current screening is KEMET's attempt to eliminate those devices that might undergo multiple scintillations during the previously discussed surge and leakage testing. The circuit impedance is kept as low as possible and the energy source has two parallel electrolytic capacitors of 12,000 uF across the output. The switching devices in this circuit are three FETs in parallel for the 'turn-on' portion, and two FETs in parallel for the 'turn-off' portion of the test. With the overall series resistances kept to a minimum, the attempt here is to obliterate the isolated fault into a massively expanded fault site with the unrestricted current [2]. A catastrophic, or ignition type of failure is the goal in this test.

With this potential and complicated mechanism of ignition readily present in tantalum-MnO_2 capacitors, the sequence of tests is important in exposing all the failures. We cycle the tests such that the surge voltage testing is followed by surge current screening, and then by leakage measurements. The surge voltage is in place to effectively heal most of the minor fault sites. The

surge current is to effectively expand the larger or remaining fault sites into a much worse condition. The magnitude of the voltage is measured just prior to the end of the current exposure period, and any decay below the preset voltage is one method of defining a failure in this test. The subsequent leakage measurement is a second method to find those capacitors with fault sites that may have been expanded by the surge tests.

The pieces placed in the reels are electrically sound with the weaker components eliminated, and if extracted from the tape and tested up to rated voltage will exhibit no failures.

How does testing *miss* the power-on failures?

After the testing, the pieces are cut out of the lead frame carriers and placed into the plastic tape and reels. Our process requires that any part that fails any of the electrical measurements be cut off the lead frame. The cut pieces are scrapped, as we have no provisions for handling loose pieces off the lead frame. If the pieces were taken out of the tape and glued onto the customers' PCBs, there would be no failures; but these capacitors are mounted to the PCBs using some type of solder process that introduces an extreme thermal exposure to the part.

The tantalum SMT capacitor is a composite structure of dissimilar materials that transforms the odd shape of the functional tantalum capacitor (pellet and wire) into a mechanically consistent package ideal for high speed handling. The materials present in the package include
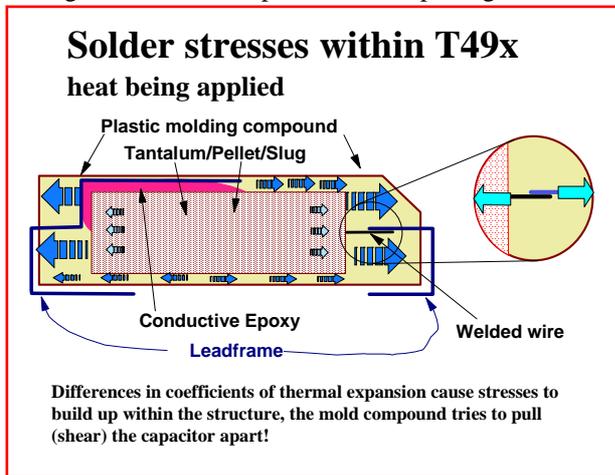
Figure 2. Mismatched CTE's.

the processed tantalum pellet and wire, the lead frame welded to the pellet's anode side and the lead frame attached with conductive adhesive to the cathode side. The plastic compound of the external package is added to the assembly as a final 'assembly' step. The metal constituents all have thermal coefficients of expansion (CTE) in the same relative magnitudes below 20 PPM/°C. The plastic compound of the case has a "glass transition" temperature where the CTE changes from one value to another. The CTE for this material below
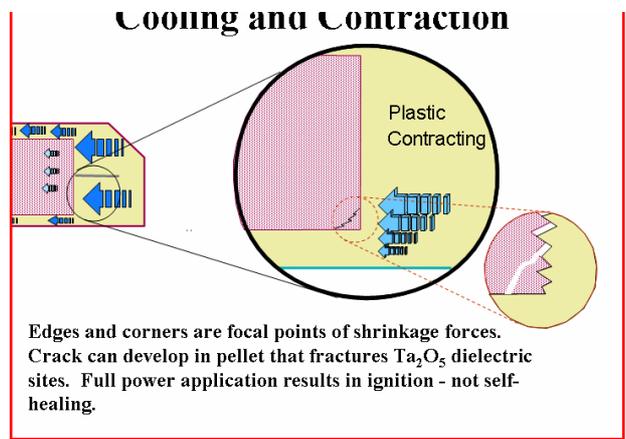
Figure 3. Contraction during cool-down.

~170°C is around 30 PPM/°C, while above this temperature; the CTE can approach 80 PPM/°C. The plastic casing which gives the mechanical components protection and the package mechanical consistency conforms to the shape of the internal structure and is in contact with all the surfaces. During the solder process, the heats are generated that are sufficient to exceed the glass transition and the plastic package at first tries to pull the package apart (as in Figure 2), then to compress it back together (as in Figure 3).

The physical forces generated do no direct harm to the lead frame or even the riser tantalum wire, but can do damage at the point the wire enters the pellet, as well as the pellet structure itself.

During the heating process, shear forces are exerted on the anode wire as the molded case pushes on the lead frame in one direction and the pellet in the opposite direction, generating forces that are pulling it away from the anode structure (Figure 2). This could generate a

high ESR failure, high DF failure, or possibly an intermittent failure.

Figure 4. Fault extension by force.

of the rated voltage would be applied. After electrical testing, there can be no fault sensitive to less than 132% of rated voltage.

In the solder process, these faults can grow, extending deeper into the dielectric and creating sites sensitive to the voltages they were originally susceptible to. As shown in the lower right of Figure 4, these sites are now susceptible to voltages that are 40%, 80%, and 140% of the rated voltage.

Shifted Distribution

When we incorporate a 100% screening in production, we subject the pieces to a voltage exposure that effectively defines the lower end of the distribution (the first or left-most drawing of Figure 5), creating a truncated distribution (the center drawing of Figure 4). From this point on up to the solder process by the customer, this truncated distribution defines that all these pieces are qualified and capable of sustaining a voltage defined by the limit utilized in screening. There may be a very small PPM failure rate if we were to screen this same lot at the same voltage, but for voltages below this screening level, there will be no failures.

The solder process develops forces within the components that may change this distribution (right-most drawing of Figure 5) to create pieces with breakdown levels below those previously screened out. The _closer the application gets to that screened level_, the _greater the propensity for failures_. The higher the screening level (T495 vs. T491), the lower the possibilities of finding failures at any given application voltage. The greater the forces developed during the solder process (excessive peak temperatures, or excessive time duration above +180°C), the greater shift of the "sorted" distribution, and the greater the percentage of failures will be realized.

Polymer replacing MnO$_2$

The new conductive polymer used in place of the

After peak temperature, the process requires a cool down and the component is now in contraction. The mismatch and forces generated during this cycle can be concentrated along the edges and corners of the anode structure. It is possible for a separation of plastic to mold contact is created, and when it comes back together, it may not fit as previously. A fault developed in a corner or along an edge can create a crack within the pellet (and dielectric). A crack in the dielectric at the corner or edge, when exposed to a high enough stress (voltage) and with unlimited current may lead to a catastrophic ignition type failure [3].

The failure site need not be created as in the corner-cracking scenario, but could be a case of the fault getting worse with these forces applied. Consider the illustration of Figure 4. On the left is the anode-dielectric-cathode structure with three faults within the dielectric. (It is important to note that the dielectric in these electrolytic capacitors is formed at 3 to 4 times the rated voltage, and the thickness is 300% to 400% of the required minimum.) In this structure there are three faults that have depleted the original 300% thickness to thick-

Figure 5. Original, clipped, and altered distributions of breakdown voltages.

nesses relegated to 250%, 200%, and 150% of the required thickness. Though the dielectric is formed to 300% of the required, once created, no more than 132%

MnO$_2$ replaces a hard, brittle substance in the anode channels with a soft compliant one. This material change may eliminate fractures from occurring within

Induced Process Stress - MnO₂

In tantalum anode pellet, areas of constriction exist where tantalum particles form a closed loop around an open channel. The MnO₂ filling this enclosure is a <u>hard</u>, <u>crystalline</u> material. Impregnation process involves dip at +25°C and conversion at +270°C. Stresses might be root of cracks *created* or *extended* in dielectric.
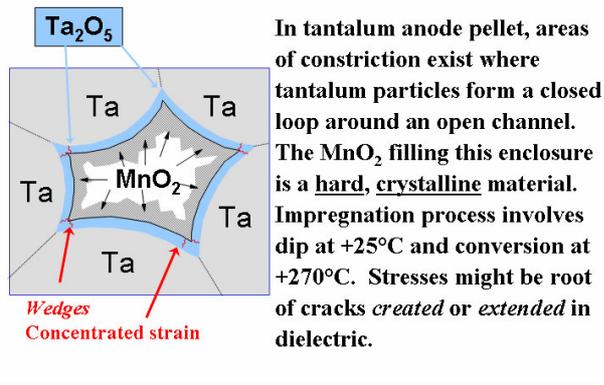
Figure 6. Tantalum-MnO₂ pore structure.

the structure of the anode (Figure 6). As the pellet utilizes pores and tunnels that channel into the pellet structure, the MnO₂ is deposited along the inner walls of the pore, creating a hard, brittle, almost metal-like core structure. The process of putting this material in (dip at 25°C, then heat to 270°C, then repeat multiple times) may actually be creating some of these faults in the glassy dielectric material.

We have seen an improvement of the voltage breakdown capability [4] with the new polymer parts (KO or T520, T530 series); but it does not eliminate all potential failures in this application. The addition of the polymer removes the oxidizing agent (MnO₂) and replaces it with very low oxygen content material that eliminates the 'ignition' sequence; but the package still consists of plastic surrounding metal. There is still a potential dielectric flaw created by the forces exerted in the internal pellet. Except for the MnO₂ and polymer exchange, the remainder of the materials and the properties of the pellet remain the same.

The structure of the pores in the polymer device is a

Reduced Process Stress - Polymer

The polymer material is soft and elastic. The forces generated because of mismatches in CTEs are insignificant when compared to MnO₂.
The process involves conversion at <u>room temperature</u> after each dip cycle -- *not* at any elevated temperatures.
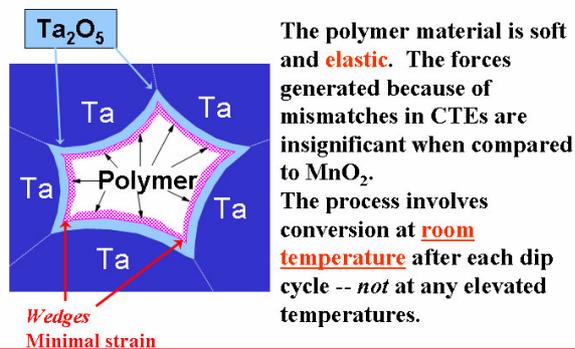
Figure 7. Pore structure in tantalum-polymer.

duplicate of the MnO₂ structure, with the difference being the material deposited along the inner walls of the tunnel structure. As shown in Figure 7, the polymer ma-

terial is processed near 25°C, and the soft, elastic material displaces itself if any forces of mismatch are created.

Aluminum Polymer Capacitors (AO or A700 series)

With this device, the central package is radically different from the pellet structure involved with the tantalum capacitors. The foils extending from the anode connection extend into the central length of the plastic package [4]. The dielectric is a very thin, glassy coating along the exposed surface of the aluminum (between the green and pink in Figure 8). It is because of this structure that there is still a potential for creating a flaw in the dielectric layer along the length of aluminum. Again the polymer is the first contact to the dielectric, and a self-healing mechanism is available to clear out all of the faults. Once again, there needs to be a time allowed for the healing to take effect before the current achieves levels to collapse the dielectric, extending the localized flaw to an ever-increasing area.
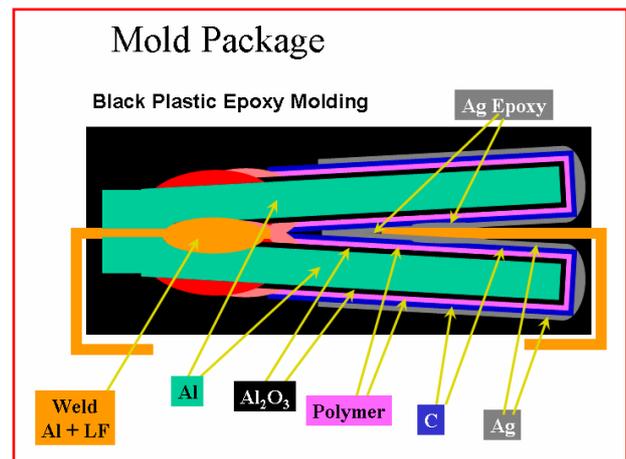
Figure 8. Aluminum-Polymer SMD capacitor.

Containment by KEMET

KEMET recognizes this possible failure scenario and is attempting to eliminate it. We are constantly looking for new mold materials, which can alleviate the forces encountered here. We have started to implement an in-line IR exposure in which the expansion and contraction forces are exercised on the finished product, prior to the electrical screening. The SMT parts pass through an IR oven with a peak temperature near 220°C, before the 100% electrical tests [5]. It is another attempt on our part to find those devices that might undergo a change in electrical properties before the customer uncovers them.

In-line IR Reflow

An attempt to exercise the package expansion/contraction prior to customers solder process.

Assembly

In-line IR-Reflow

Final Electrical Test
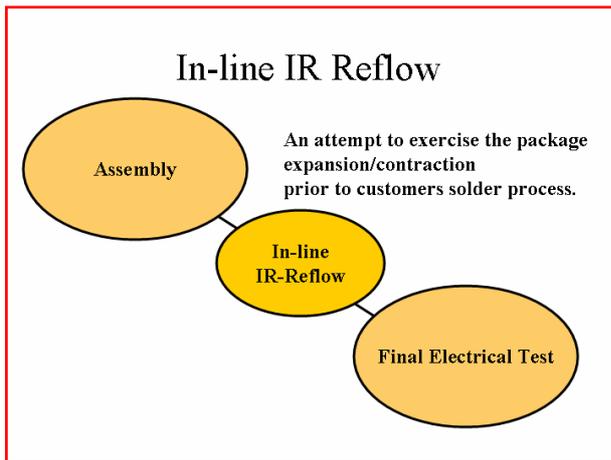
Figure 9. In-line IR Reflow in capacitor manufacturing.

The power supply capacitors, being more robust and likely to be placed in high current applications, are surge current tested up to 100% of rated voltage. Remember that surge current testing is through minimal impedance 0.3 ohms, whereas surge voltage testing is through a pre-defined resistance greater or equal to 30 ohms.

This test is not always 100% effective because we cannot control how our customer processes the solder reflow. We cannot control the number of reflow cycles the customer may expose the parts to. When our customers note failures, we attempt to not only establish at what electrical conditions did the faults appear, but we review the solder process or processes that were involved prior to the fault detection.

KEMET is also continuing to develop the Scintillation [1] and Surge Step Stress Testing (SSST) [2], as possible tools in uncovering answers as to batch variation and susceptibility. Both of these tests require that the part be surface mount soldered to a PCB prior to testing. The scintillation test applies a constant current to the device (usually less than 100 uA), and monitors the voltage increase -- looking for step-drop in the voltage ramp, or a scintillation (results shown in Figure 1). We test a sample and use the first level of scintillation as an indication of the weakest spot in the device, or as the point of failure (projected). We use weibull analysis to look at the cumulative percentage of "failures" versus the scintillation voltage level, and we stress the part up to 4 times rated voltage to force the failures. From this data we can project the percentage failure for any application voltage, as well as determine the voltage level that would generate 100 PPM (or any other level) of failure. This test does not apply a high inrush current to the part, and its premise for correlation to power-on ignitions dictates the assumption that the first scintillation voltage level will <u>not</u> undergo any self-healing, but would generate an ignition type of failure. We know that this assumption is not entirely correct, because we've infrequently observed scintillations actually oc-

curring during oscilloscope monitoring of surge current testing.

The SSST test exposes the part to the same surge current circuit of ~0.3 ohms impedance, but the voltages are applied across the capacitor in an increasing step condition. We first expose the capacitor to 5 pulses at ½ rated voltage, then increment the voltage and repeat the 5-pulse exposure. The voltage is incremented until catastrophic failure results. We repeat this test for several pieces in a sample, and do the cumulative percentage weibull analysis, the same as mentioned in the scintillation testing.

This test does do incremental application, unlike any of our customers' actual applications. In the same vein that the scintillation test erroneously assumes each scintillation to be an "ignition", an argument might be made that with this test, different level (voltage) fault sites are exposed incrementally up to a specific voltage level. The results might be different from a quick one-step exposure to that specific voltage level. Neither of these tests are an exact duplication of the power-on applications that our customers experience, but we're using these in an attempt to effect improvements related to these applications.

There are additional materials and process modifications that KEMET is experimenting with that may have an appreciable impact on this failure mode. This is part of the ongoing Quality improvement efforts to make sure that we offer the best product available.

Containment by Users

Through years of study, we've concluded that once a part is exposed to a voltage level and survives, then additional exposures to that same level will not produce a failure. Only with the exposure to extreme environmental stress or to higher voltages, will additional failures occur. Parts tested at KEMET and packaged are all capable of never generating failures. We believe that most of the failures are generated by environmental stress. The higher or more numerous the stresses, the higher the resultant failures count.

Control of soldering conditions.

The solder profile is extremely important in the analysis of this type of failure. Frequent temperature profiles achieved using a "mole" that travels through the process is an invaluable tool. Settings on the IR or any other system do not give a true presentation of the temperatures experienced in this process. Control limits are assumed to be a given, but I've seen facilities that run daily profiles with large variations evident, yet no corrective actions are taken. A window of acceptable temperature and time must be defined and used as a guide to control this process and results outside of this window must dictate that some action be taken.

When we review a reflow profile, we look at the time above 180°C. It is in this time, that the greatest expansion forces are created in the mold compound. Ideally, we like to see this exposure kept below 90 seconds. The lead-free solder profiles are of concern if the profile is adjusted with the same ramps to higher temperatures because this will increase not only the time above 180°C, but the peak temperatures as well. For our part, we would like to see the higher peak temperatures reached but keep the total exposure above 180°C at less than 90 seconds.

Wave solder does not usually present any problems, except in one instance where the preheat was ramped up at an agonizingly slow rate to 200°C, and the time above 180°C was close to 120 seconds.

REWORK is a four-letter word.

Additional cycles through the reflow heat can exacerbate the potential flaw sites in a tantalum capacitor. Uncontrolled solder iron rework should develop the same response as dragging fingernails on a blackboard. It might not be avoided, but at least maintain identity for those boards that are subjected to rework.

Controlled, Initial Power – "Proofing"

Some customers know that they violate the recommended solder profiles, but other circuit considerations leave them no choice. Additionally, there are customers who put capacitors in high stress applications where they are operated closer to the rated voltage of the parts with no de-rating (not applicable to AO). In order to overcome high failure rates (ignitions) at initial power-up, some will include a series resistance from the power supply for the initial power application only (1000 ohms is typical). All subsequent applications of power at the same or lower voltages are without the series resistance, but the initial application may have activated the self-healing effect in these capacitors. (The 1st exposure "proofs" the capacitor.) The 1st voltage (through the resistance) should also be higher than or as high as any voltage the circuit will experience in its life.

The following steps detail the recommended "Proofing" method for eliminating any high incidence of power-on failures:

1. Define the absolute maximum voltage level the components may see in their circuit application. (e.g., A 12 VDC application might see voltages as high as 13.6 VDC would use 13.6 as this level)

2. Pad this voltage with a safety margin. (e.g., With the 13.6 VDC, add 1 VDC, and round it up to 15 VDC.)

3. Apply this voltage to the capacitor(s) through a 1–kOhms resistor, ensuring the appearance of 15 VDC for 5 seconds. (The capacitor has been proofed to 15 VDC.)

4. Any subsequent application of voltage is made through no series resistance, and will not fail as long as the voltages remain below 15 VDC.

The capacitors are now cleared of any dielectric defects that would trigger a fault avalanche at voltages up to 15 VDC.

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