Investigation on Using Solid Tantalum Capacitors

(Individual and Parallel Configurations)

28th of June 2005

TEC-EPC
F. Tonicello & O. Mourra

AVX meeting

Passive WG meeting

Outline of the presentation

1. **Objectives of the Test Campaign**
2. **Initial Characteristics**
3. **Individual Capacitors Tests**
   a. Limit of Utilisation
   b. Tests performed on single capacitors
      . *Surge Current Tests*
      . *Over-voltage Tests*
      . *Over-current Tests*
4. **Capacitors Used in Parallel Configuration**
   a. Issues of Utilisation
   b. Tests Performed on different capacitor banks
5. **Conclusions**
6. **Questions and Discussion**

1. Objectives of the Test Campaign

The objectives of the present investigation were:

- to clarify the limits of utilization, in particular regarding the maximum allowable RMS current.

- to check capacitors robustness with respect to their rated limits.

- to check the long-term reliability of solid tantalum capacitors when used in a parallel configuration.

- to check if the present ECSS de-rating rules do define a safe envelope of application.
(De-ratings:Voltage: 60%, Power dissipation: 50%, surge current: 40%).

To this purpose, several capacitor banks were life–tested in different current regime conditions to simulate real-life applications and some sample capacitors were tested individually with different electrical stresses.

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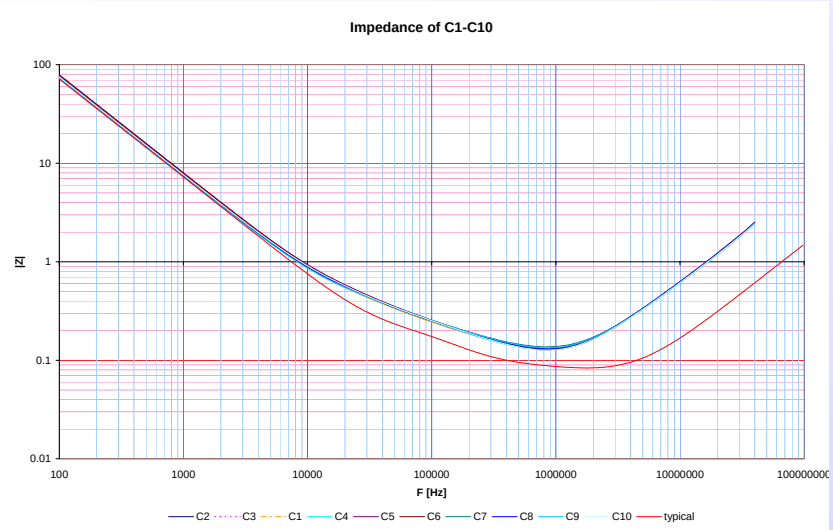
2. Initial characteristics (1/2)

- Impedance

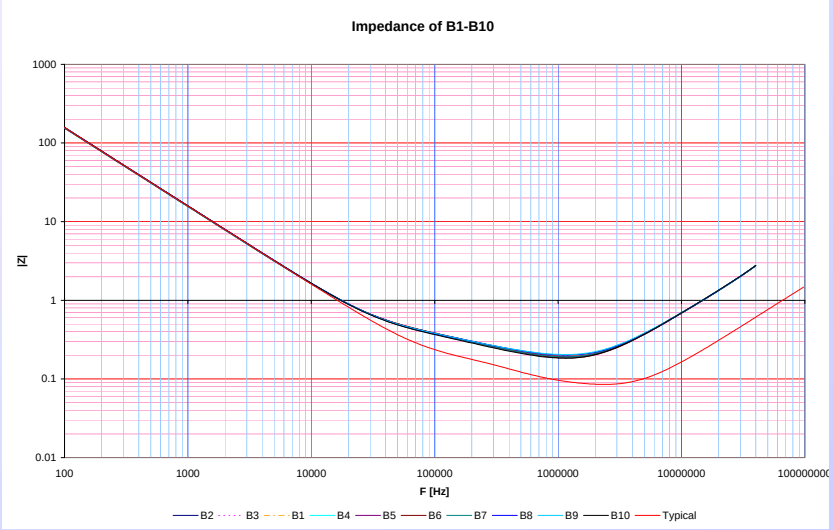
Conditions of measurements: Bias: 2.2V, osc: 0.5Vrms - Clip connection

Before and after each characterization, the test set up was validated by the characterisation of a "stable" PM90SR.

TAJD226M035RNJ -> TAJ, case D, 22uF, 35V



TAJD106K035RHJ -> TAJ, case D, 10uF, 35V



Red curve is the typical impedance given by AVX

2. Initial characteristics (1/2)

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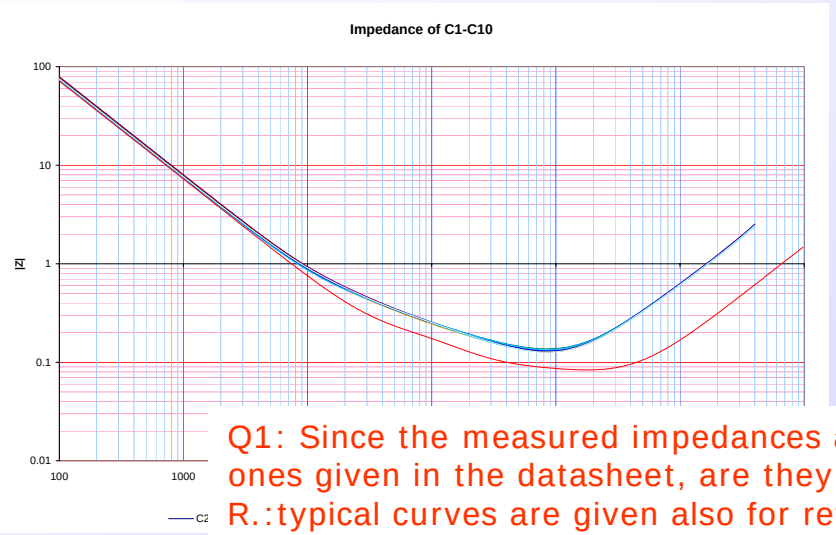

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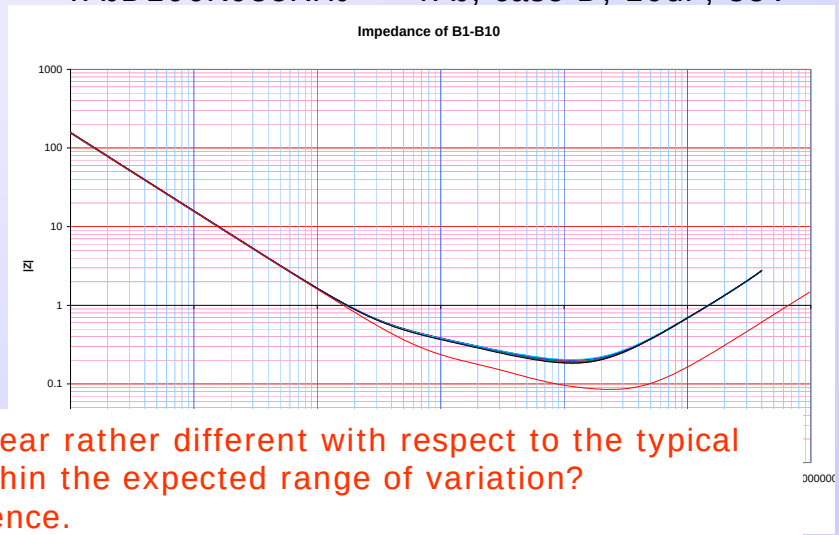
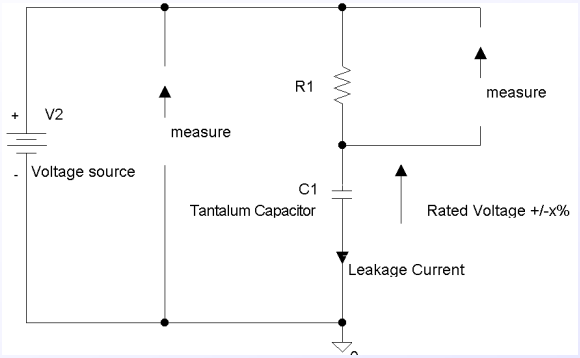


Q1: Since the measured impedances appear rather different with respect to the typical ones given in the datasheet, are they within the expected range of variation?
R.:typical curves are given also for reference.
How wide is this envelope?
R.: ESR(100KHz) is the key parameter to be analysed statistically
Does it change with applied DC voltage?
R.: No appreciable variation is expected.
AVX have ESR(f), with f=100KHz, as a parameter of known statistically

2. Initial characteristics(2/2)

- Leakage Current

Conditions of measurement: room temperature - rated voltage +/-2% - after 4.30 minutes – 100k Ohms in series – Clip connection.



Leakage Current	Min	Max	Datasheet Max
50 TC TAJ D 22uF 35V (surge current tested)	60nA	230nA	7.7uA
50 TC TAJ D 10uF 35 V (surge current tested)	20nA	140nA	3.5uA

Q2: What are the minimum and typical leakage current of the capacitors (TAJD226M035RNJ AND TAJD106K035RNJ) ?
Why is the datasheet maximum leakage current much higher than the tested one?

R.: reflow/humidity and the other enviromnetal conditions are affecting the specified leakage, and a guard band is applied as an industry standard.
Typical test at AVX is done after 3'.

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3. Individual Capacitors Tests

a. Limit of Utilisation (1/3)

- In the datasheet, or in the space procurement specification, the rated voltage is specified but the rated RMS Current is not specified.

  Instead, the "power" limitation is specified in terms of maximum allowable power dissipation per package.

- In practical application, how can we establish the corresponding maximum allowable RMS Current?

Note
The design is made such to allow 10 degC increase in open air when capacitor is connected electrically by needle connections.
This leads to the capacitors rated power capability given in the datasheet.

3. Individual Capacitors Tests

a. Limit of Utilisation (2/3)

For example, the guidelines of AVX for **one single capacitor** are the following:

The current waveform applied to the capacitor shall be decomposed in Fourier series. AVX provides the typical ESR values in function of frequency, and it is then possible to calculate the typical RMS power dissipation at each harmonic.
Root-square sum of the individual harmonic contributions gives the **typical** RMS power dissipation for **one** capacitor.

*Ex: For one single TAJ, 10uF, 35V, case D, assuming to apply **a square current waveform** with duty cycle=0.5,*
⇒ the RMS current at 25°C has to be lower than 1A RMS to respect the rated power dissipation for that package(150mW)

*But… this approach is NOT the WC one, since the **TYPICAL** ESR=f(F) is used :*
-> the power dissipated by the capacitor may be HIGHER than calculated…

3. Individual Capacitors Tests

a. Limit of Utilisation (3/3)

The same approach was used with the maximum ESR available in the datasheet, and the ESR=f(F) measured in our laboratory:

	TAJ		TPS	
	10uF	**22uF**	**10uF**	**22uF**
Maximum Esr at 100kHz	1Ω	0.9Ω	0.3Ω	0.2Ω

	RMS Current* per type of tantalum capacitors			
Type / **ESR**	**TAJ**		**TPS**	
	10uF, 35V, K, RHJ, case D	22uF, 35V, M, RNJ, case D	10uF, 35V, K, R0300, case D	22uF, 35V, M, R0200, case D
Typical from AVX @25degC	1A RMS	1.12A RMS	0.9 A RMS	1.19 A RMS
Max at 100Khz	0.39A RMS	0.41 A RMS	0.71 A RMS	0.87 A RMS
Measured at @25degC	0.74A RMS	0.93 A RMS	0.93 A RMS	0.91 A RMS

*•Assuming to apply a **square current waveform** with duty cycle=0.5 at 130KHz*
•Power Dissipation of 150mW (cases D)

3. Individual Capacitors Tests

a. Limit of Utilisation (3/3)

The same approach was used with the maximum ESR available in the datasheet, and the ESR=f(F) measured in our laboratory:

	TAJ		TPS	
	10uF	22uF	10uF	22uF
Maximum Esr at 100kHz	1Ω	0.9Ω	0.3Ω	0.2Ω

	RMS Current* per type of tantalum capacitors			
Type	TAJ		TPS	
@25degC				

•*Assuming to apply a **square current waveform** with duty cycle=0.5 at 130KHz*
•*Power Dissipation of 150mW (cases D)*

Q3: Question to the manufacturer: in absence of the envelope ESR(f) shall the user make use of the ESR maximum value given in the datasheet? Note that this may lead to a poor utilisation of the devices….

R.: not surprised by the results. Key design has to be the guaranteed ESR limit at 100KHz. Full stop. Reason being that the ESR(f) distribution is subject to process and manufacturing modifications.

PSPICE model for max (and not only typical) impedance is in the plan of AVX – very good !

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3. Individual Capacitors Tests

b. Tests Performed on single capacitors (SCT 1/7)

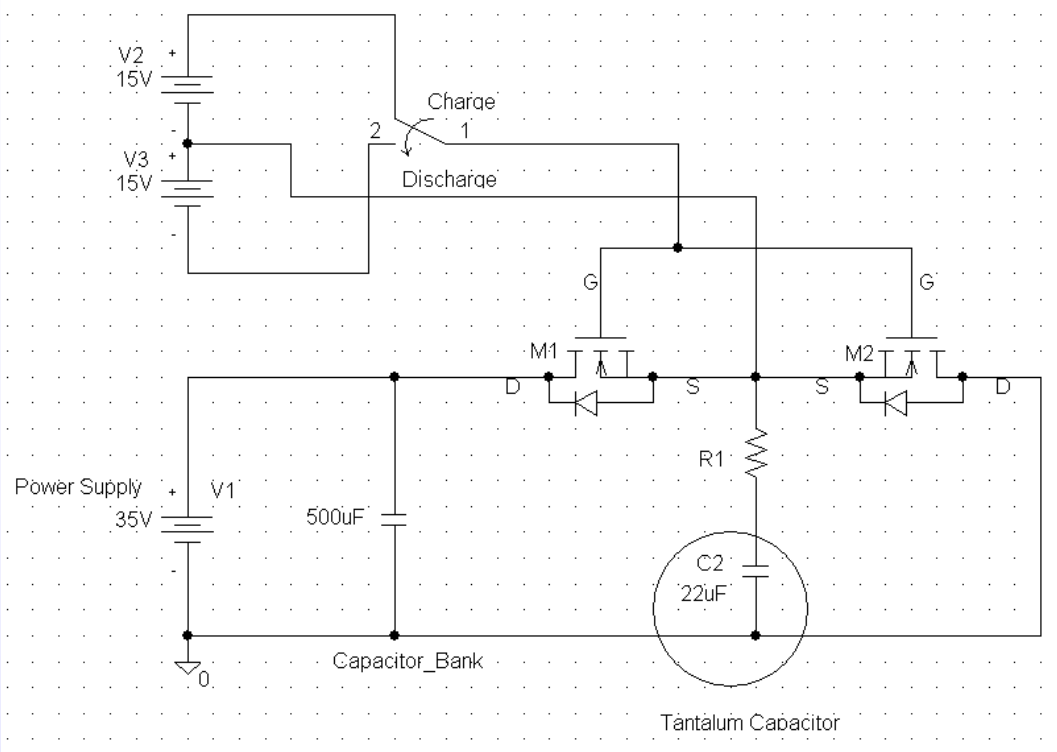
- *Tests focus only on the tantalum capacitors:*
  - *TAJD226M035RNJ -> TAJ, case D, 22uF, 35V* ***COMMERCIAL SAMPLES***
- Electrical Tests:
  - Surge Current Tests
    - Test 1: 10 surge current peaks (55A)
    - Test 2: 3600 surge current peaks (55A)
    - Test 3: 3600 surge current peaks (110A)
  - Over-Voltage Tests
  - Over-Current Tests

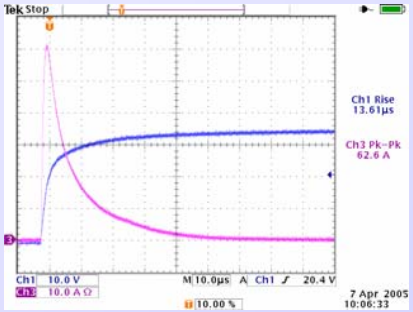
  During the tests, the leakage currents and impedances of the single capacitors were measured in steps at different levels of the electrical stress.

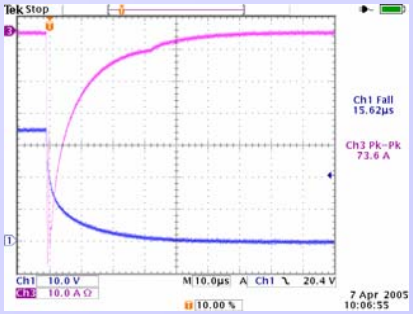
3. Individual Capacitors Tests

b. Tests Performed on single capacitors (SCT 2/7)

Surge Current Tests: TEST SET-UPS according to ECSS 3011 p 27A







3. Individual Capacitors Tests

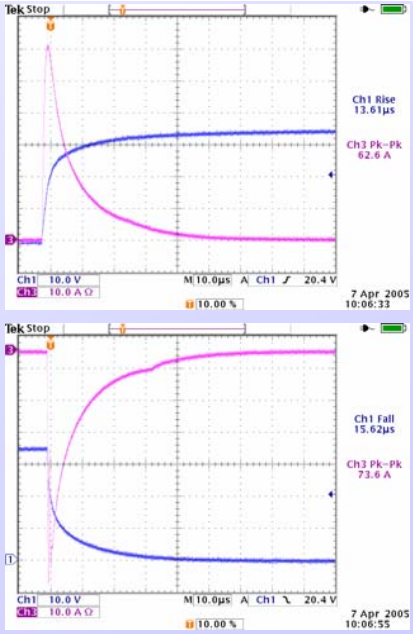
b. Tests Performed on single capacitors (SCT 3/7)

Note
AVX reckons that the most critical conditions for failure under surge are within the for two pulses !

Surge Current Tests: TEST 1

Conditions:

- Each capacitor was tested individually.
- The 10 current peaks (5 charges, 5 discharges at the rated voltage) were **higher than 55A**.
- The rising and falling times were **lower than 20us**.
- The tests were performed at room temperature and pressure.
- Before and after the SCT, the leakage current and the impedance of the capacitor under test were measured and compared.
- The capacitor was fixed by a clip on the breadboard (it was **not soldered**).



3. Individual Capacitors Tests

b. Tests Performed on single capacitors (SCT 4/7)

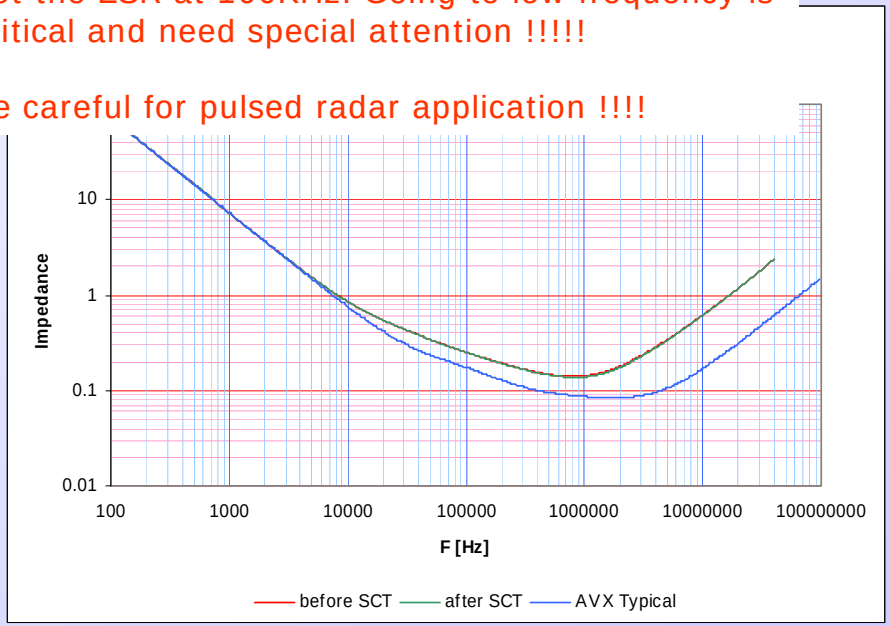
Surge Current Tests: TEST 1

ONE CAPACITOR FAILED !

Capacitor	LC before SCT [A]	LC after SCT (2 days) [A]	Ratio
T1	6.01E-08	6.01E-08	1.00
T2	6.31E-08	6.41E-08	0.98
T3	9.62E-08	9.32E-08	1.03
T4	7.01E-08	7.21E-08	0.97
T5	6.81E-08	6.51E-08	1.05
T7	7.51E-08	7.61E-08	0.99
T9	6.71E-08	6.51E-08	1.03
T10	1.46E-07	1.40E-07	1.04
T11	7.51E-08	7.31E-08	1.03
T12	7.31E-08	7.21E-08	1.01
T13	7.11E-08	7.01E-08	1.01
T14	7.21E-08	7.01E-08	1.03
T15	9.72E-08	9.02E-08	1.08
T16	7.41E-08	7.01E-08	1.06
T17	7.86E-08	7.51E-08	1.05
T18	6.91E-08	6.51E-08	1.06
T19	6.61E-08	6.71E-08	0.99
T20	2.18E-07	2.00E-07	1.09
T21	8.01E-08	7.81E-08	1.03
T22	1.90E-07	1.75E-07	1.09

Note
Repeated application of surge pulse: AVX recommends using the DF figure at 120 Hz and not the ESR at 100KHz. Going to low frequency is critical and need special attention !!!!!

Be careful for pulsed radar application !!!!



For all capacitors but the failed one, their signature (leakage current & impedance) did not change.

3. Individual Capacitors Tests

b. Tests Performed on single capacitors (SCT 5/7)

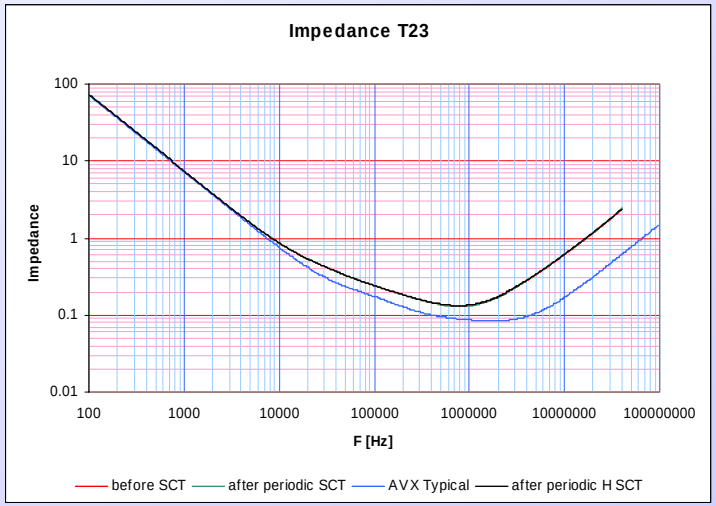
Surge Current Tests: TEST 2 (repeated test 1 -> 3600 current peaks >55A)

=> No failure

Leakage Current

		Leakage Current		
		before SCT	after SCT (2 days)	after the tests of T23-T27 SCT nominal 30 minutes
ref	T1	6.01E-08	6.01E-08	5.41E-08
ref	T2	6.31E-08	6.41E-08	6.51E-08
ref	T3	9.62E-08	9.32E-08	9.12E-08
ref	T4	7.01E-08	7.21E-08	6.81E-08
ref	T5	6.81E-08	6.51E-08	6.51E-08
tested	T23	6.71E-08		6.21E-08
tested	T24	9.52E-08		8.41E-08
tested	T25	7.01E-08		6.31E-08
tested	T26	1.01E-07		9.02E-08
tested	T27	7.01E-08		6.31E-08

Impedances



For all capacitors but the failed one, their signature (leakage current & impedance) did not change.

3. Individual Capacitors Tests

b. Tests Performed on single capacitors (SCT 6/7)

Surge Current Tests: TEST 3 (repeated test-> 3600 peaks of current >110A)

Conditions:

- Each capacitor was tested individually.
- The tests were performed at room temperature and pressure.
- The current peaks (charge, and discharge at the rated voltage every second during 30 minutes) were **higher than 110A**.
  -> 1800 positive current pulses and 1800 negative current pulses
- The rising and falling times were lower than 20us.
- Before and after the SCT, the leakage current and the impedance of the tested capacitor were measured and compared.
- The capacitor was clipped (**not soldered**) on the breadboard.

3. Individual Capacitors Tests

b. Tests Performed on single capacitors (SCT 7/7)

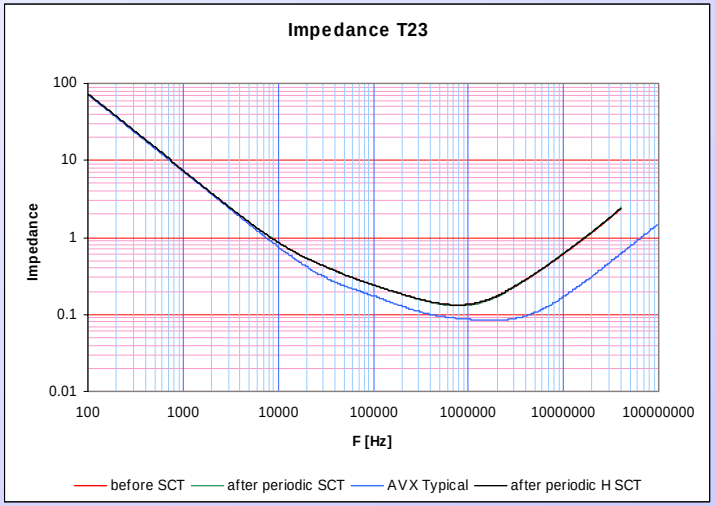
Surge Current Tests: TEST 3 (repeated test-> 3600 peaks of current >110A)

No failure

Leakage Current

		Leakage Current			
		before SCT	after SCT (2 days)	after the tests of T23-T27 SCT nominal 30 minutes	after the tests of T23-T27 SCT high level 30 minutes
ref	T1	6.01E-08	6.01E-08	5.41E-08	5.81E-08
ref	T2	6.31E-08	6.41E-08	6.51E-08	6.51E-08
ref	T3	9.62E-08	9.32E-08	9.12E-08	9.52E-08
ref	T4	7.01E-08	7.21E-08	6.81E-08	7.01E-08
ref	T5	6.81E-08	6.51E-08	6.51E-08	6.81E-08
tested	T23	6.71E-08		6.21E-08	6.11E-08
tested	T24	9.52E-08		8.41E-08	8.62E-08
tested	T25	7.01E-08		6.31E-08	6.41E-08
tested	T26	1.01E-07		9.02E-08	9.02E-08
tested	T27	7.01E-08		6.31E-08	6.51E-08

Impedances



When the capacitor didn't fail, the signature of the capacitor remained the same.

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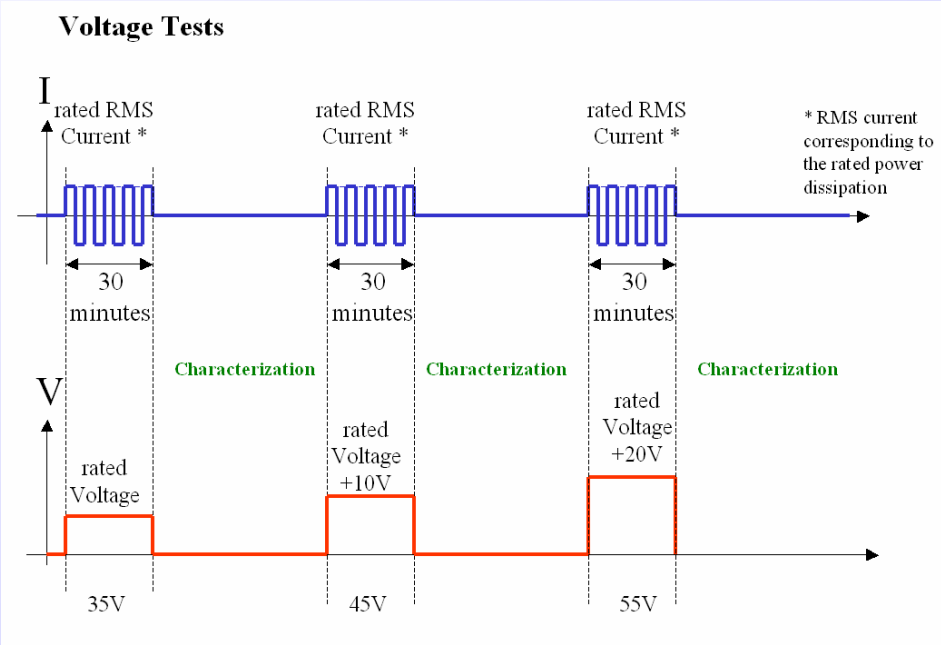
3. Individual Capacitors Tests

b. Tests Performed on single capacitors (Voltage Test 1/2)

Over-voltage Tests:

- Each capacitor was tested at **different levels of voltage** during periods of 30 minutes. The tests started at the rated voltage (35V).
- At the end of each testing period, after minimum 12 hours of rest time, the capacitor signature was taken (leakage current and impedance). The voltage was then increased, and the test repeated.
- The test was stopped when the capacitor failed.
- During the test, the capacitor was stressed at the **rated power dissipation** (150mW). To reach this power dissipation the current injected in the capacitor was almost square waved (duty cycle 50%, frequency 130KHz) with an RMS value of **1Arms.**
- The tests were performed at room temperature and pressure.
- The capacitor was connected to the breadboard by a clip **(it was not soldered)**.



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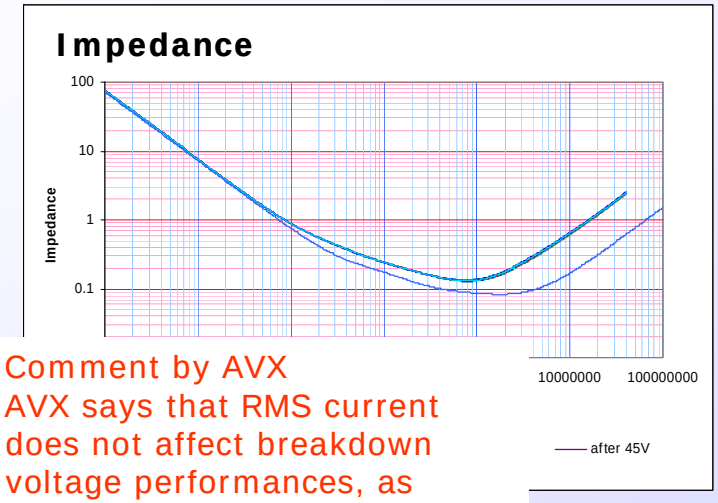
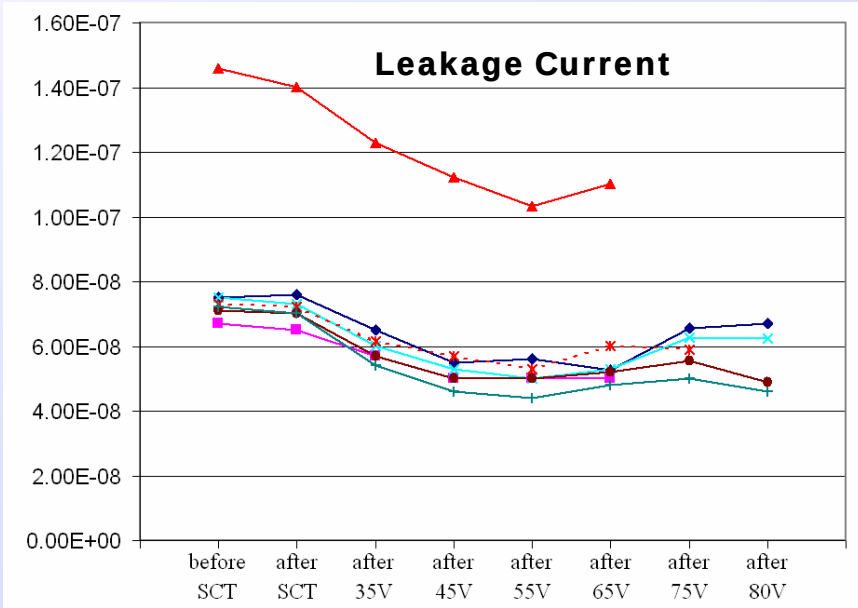
3. Individual Capacitors Tests

b. Tests Performed on single capacitors (Voltage Test 2/2)

The capacitors were tested at 35V, 45V, 55V, 65V, 75V, 80V and 85V.

RESULTS: 2 failures at 75V, 1 failure at 80V, 2 failures at 85V. 2 capacitors survived at 85V.





Comment by AVX
AVX says that RMS current does not affect breakdown voltage performances, as expected.
The BV performances are as expected.

d stable until the failures occured.
ıge failure was 75V (more than twice the rated voltage).

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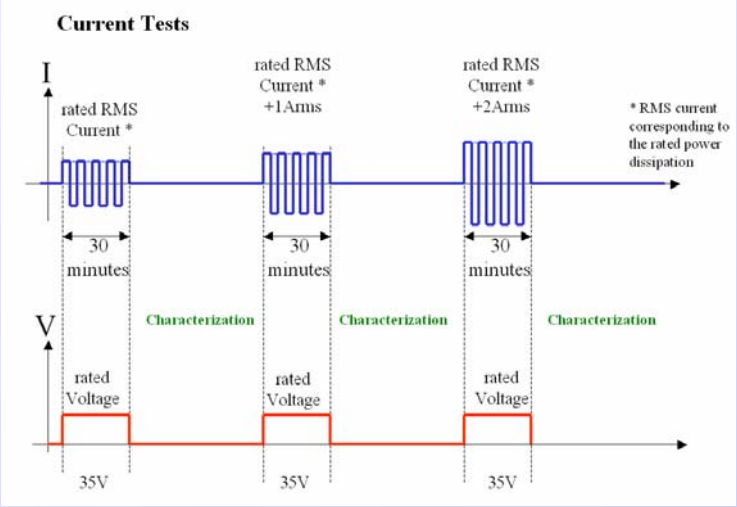
3. Capacitor Used Individually

b. Tests Performed with one single capacitor (Current Test 1/2)

Over-current Tests:

- Each capacitor was tested at **different levels of current**, at the **rated voltage** (35V) during periods of 30 minutes.
- The tests started injecting a current (1Arms) corresponding to the rated power dissipation (150mW). At the end of each testing period, after minimum 12 hours of rest time, the capacitor was characterized (leakage current and signature).
- The RMS current was then increased by a **step of 1A rms** for the next period of test. The test was stopped when the current reached 4 times the one corresponding to the rated power dissipation.
- The tests were performed at room temperature and pressure.
- The capacitor was connected to the breadboard by a clip **(it was not soldered)**.

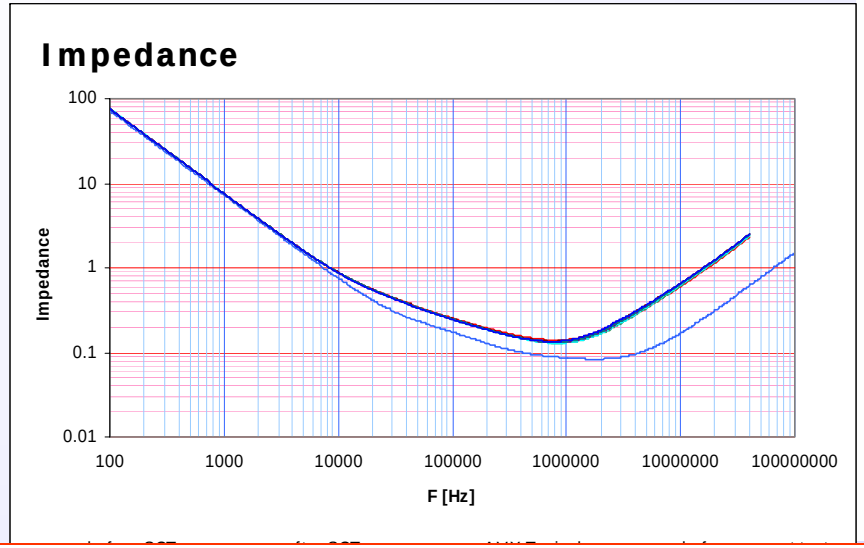


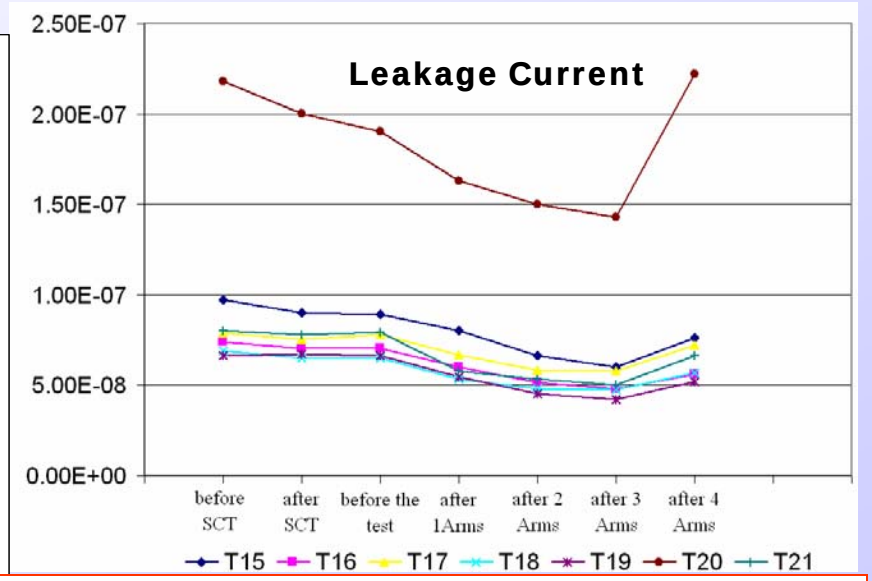
3. Capacitor Used Individually

b. Tests Performed with one single capacitor (Current Test 2/2)

Over-current Tests:

The capacitors were tested at 1 Arms, 2 Arms, 3 Arms and 4 Arms.
No capacitor failed.





Signature: the leakage current and the impedances did not change, with exception of one capacitor, for which the leakage current increased appreciably at 4 Arms.

A similar test was performed on another type of capacitor (TAJ, 10u, 35V, case D) and in that case the leakage current increased before an over-current failure (more than 4 times the current corresponding to the rated power dissipation).

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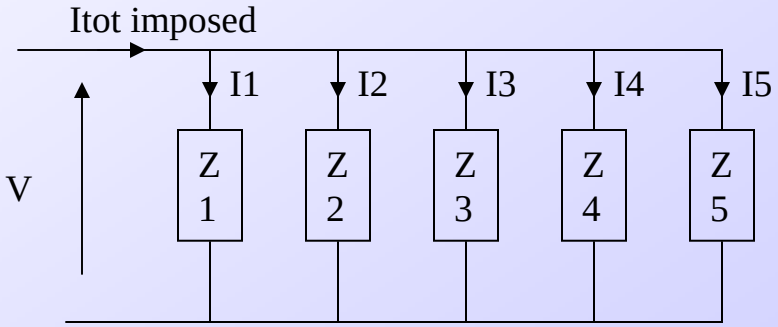
3. Capacitor Used in parallel Configuration

a. Issues of utilisation (1/11)

- In the datasheet, or in the space procurement specification, the rated voltage is specified but the RMS Current is not specified. The limitation is instead specified in terms of maximum allowable power dissipation per package.

- How can we establish the maximum allowable RMS current that a capacitor bank can absorb, without exceeding the maximum allowable dissipation of each capacitor?



-> Analysis with an impedance model of each capacitor

3. Capacitor Used in parallel Configuration

a. Issues of utilisation (2/11)

-> Which Impedance model of each capacitor can be used?

- **ESR=ESR(f) model**
- **Simple RLC series model**
- **Complex manufacturer model**

Common assumption for performed analyses:

Square wave with 50% duty cycle, 130 KHz.

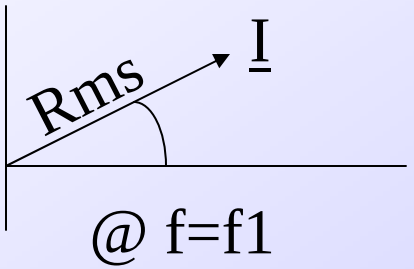
3. Capacitor Used in parallel Configuration

a. Issues of utilisation (3/11)

-> Which Impedance model of each capacitor can be used?

- **ESR=ESR(f) model applied to a CB of 10 caps (22uF)**

From the characterisation of each capacitor ESR=ESR(f), the RMS current into each capacitor has been calculated at the harmonic frequencies, in order to respect the de-rated power dissipation.



Amplitude of the square wave current in C11

Modules of the current vectors of C11 at each harmonic frequency

SQUARE WAVE CURRENT		AMP				Before sol
		0.64				ESR C11
Freq	Harmonic	Amplitude	RMS	RMS^2	POWER	Real part
128571.08	1	0.818289975	0.57861839	0.334799242	0.06477605	0.193477
384873.84	3	0.272763325	0.192872797	0.037199916	0.005634182	0.151457
644764.02	5	0.163657995	0.115723678	0.01339197	0.001885836	0.140818
919300.39	7	0.116898568	0.08265977	0.006832638	0.000931571	0.136341
1189867.6	9	0.090921108	0.064290932	0.004133324	0.000554942	0.134261
1443874.8	11	0.074389998	0.052601672	0.002766936	0.000369478	0.133533
1696505.6	13	0.062945383	0.044509107	0.001981061	0.000264528	0.133529
1993338.4	15	0.054552665	0.038574559	0.001487997	0.00019927	0.133918
2267783.8	17	0.048134704	0.034036376	0.001158475	0.000155699	0.1344
2498141.8	19	0.043067893	0.030453599	0.000927422	0.000125162	0.134957
2751899.3	21	0.038966189	0.027553257	0.000759182	0.000102992	0.135662
			sqrt of sumsq	0.64		
				Power total	0.074999711	
				Power limit	0.075	
				Diff	2.8909E-07	

ESRc11=f(F)

RMS value of the current injected in C11

Power dissipation for C11

3. Capacitor Used in parallel Configuration

a. Issues of utilisation (4/11)

-> Which Impedance model of each capacitor can be used?

- **ESR=ESR(f) model applied to a CB of 10 caps (22uF)**

Then the RMS current of the capacitor bank at each harmonic frequency is calculated by summing the individual RMS current contributions (summation of the individual rms current vectors at each harmonic frequency).

square Root of the sum square of the harmonic sums gives the overall RMS current than can be injected in the CB.

Sum of the individual capacitor current vectors at each harmonic frequency

freq	Sum real	Sum Img	RMS Value	RMS value ^2
128571.1	4.728985	2.884294	5.539174448	30.68245356
384873.8	1.747998	0.456981	1.806745447	3.264329111
644764	1.058287	0.016263	1.058411717	1.120235362
919300.4	0.723853	-0.151493	0.739536232	0.546913839
1189868	0.522616	-0.2175	0.566069001	0.320434114
1443875	0.394502	-0.234625	0.458999674	0.2106807
1696506	0.306876	-0.234861	0.386435733	0.149332576
1993338	0.241004	-0.231343	0.334069322	0.111602312
2267784	0.194625	-0.221242	0.294663451	0.086826549
2498142	0.162101	-0.208118	0.263798663	0.069589735
2751899	0.136018	-0.196477	0.23896436	0.057103965
			sqrt of sumsq	**6.051404946**

Square-root of the sum square of the RMS harmonic contributions

RMS value of the capacitor bank current

Result:
The CB current can reach 6 Arms to satisfy a 50% de-rating on the capacitor's rated power dissipation.

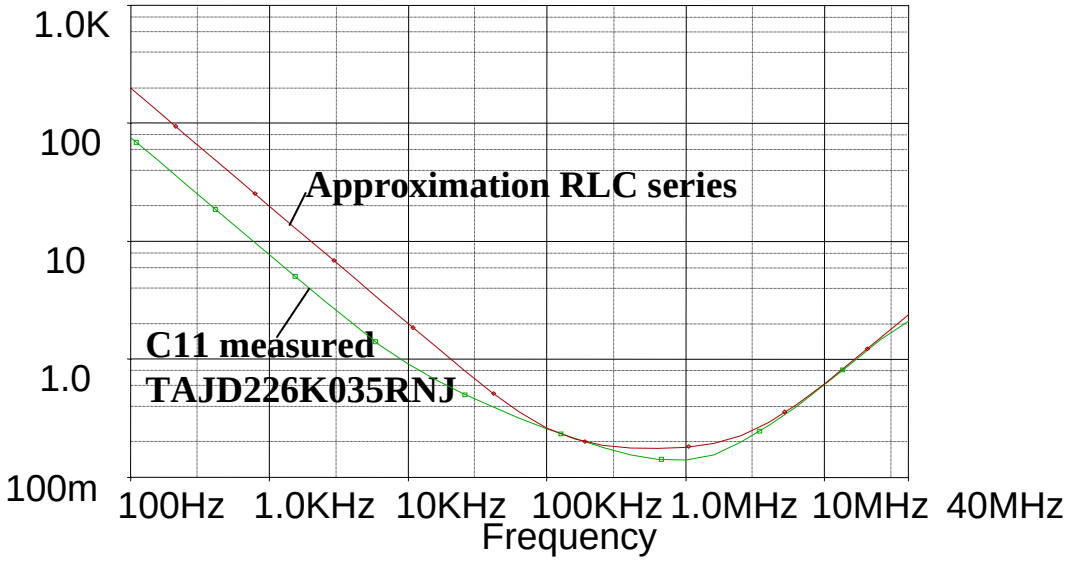
Drawbacks:
. The impedances measured may be not stable during all the period of test.
. We assume that the individual currents are all Square Waves !!!

3. Capacitor Used in parallel Configuration

a. Issues of utilisation (5/11)

-> Which Impedance model of each capacitor can be used?

- **Simple RLC series model**



3. Capacitor Used in parallel Configuration

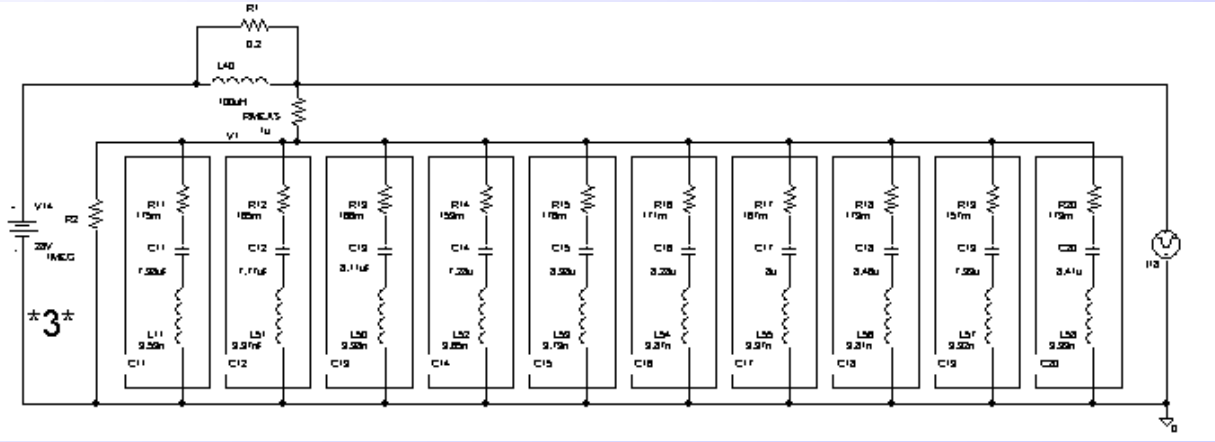
a. Issues of utilisation (6/11)

-> Which Impedance model of each capacitor can be used?

- **Simple RLC series model**

With a frequency analyzer the impedances of the single capacitors were measured and their equivalent RLC circuits identified.

With the RLC circuits, a simulation was performed to find the maximum total rms current, which doesn't exceed the de-rated power dissipation for each single capacitor.



3. Capacitor Used in parallel Configuration

a. Issues of utilisation (7/11)

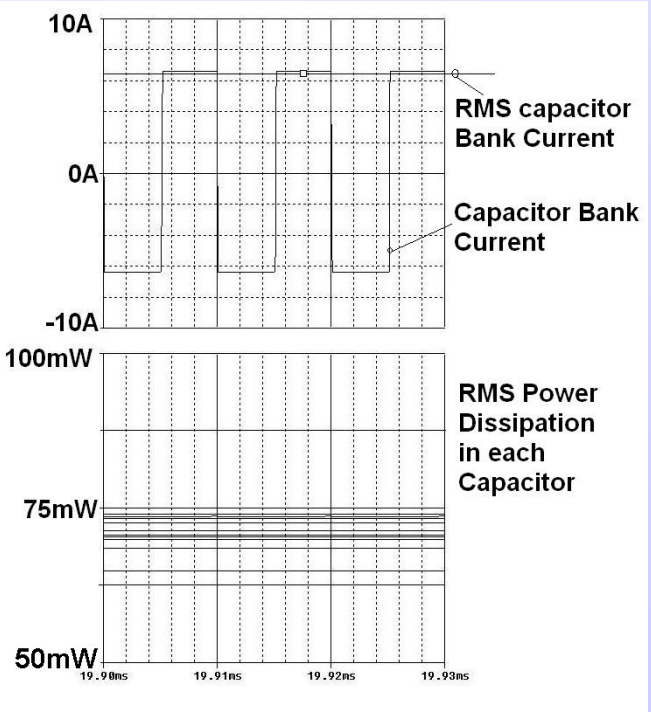
-> Which Impedance model of each capacitor can be used?

- **Simple RLC series model**

Result:

the current can reach 6.5 Arms at the capacitor bank level to satisfy a 50% de-rating on the capacitor's rated power dissipation.

Drawback: RLC model is poorly representative

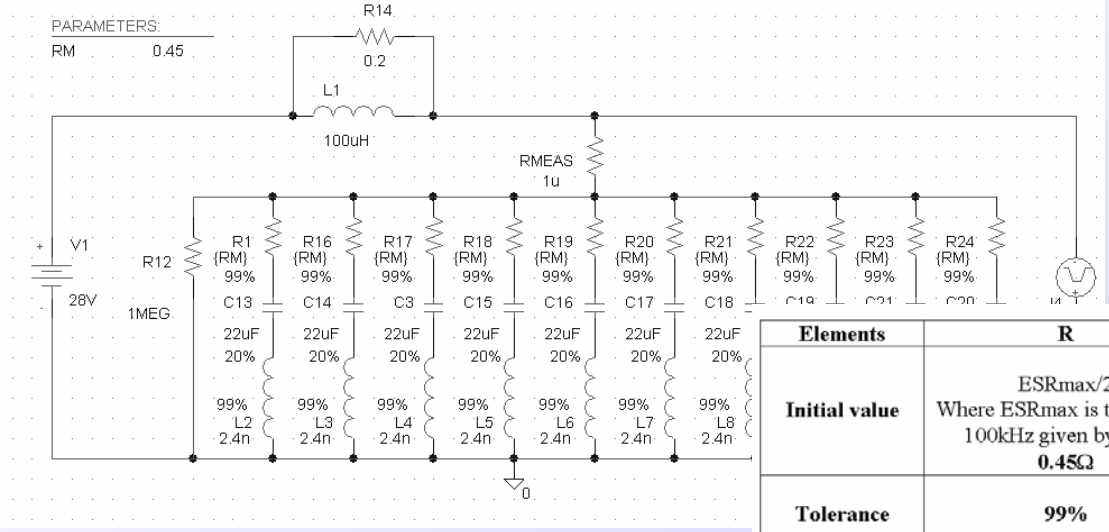


3. Capacitor Used in parallel Configuration

a. Issues of utilisation (8/11)

-> Which Impedance model of each capacitor can be used?

- **Simple RLC series model to perform a Worst Case Analysis**



Monte Carlo Analysis with 1000 runs

Elements	R	L	C
Initial value	ESRmax/2 Where ESRmax is the max at 100kHz given by AVX **0.45Ω**	Typical parasitic inductor given by AVX **2.4nH**	Capacitance of the single capacitor **22uF**
Tolerance	**99%**	**99%**	Tolerance of the capacitance of the single capacitor **20%**
Comments	To cover the range of values between 0 and ESRmax	To cover the range of values between 0 and 2 times the parasitic inductor	-
Range of value	**[0+, 0.9Ω]**	**[0+, 4.8nH]**	**22uF +/- 20%**

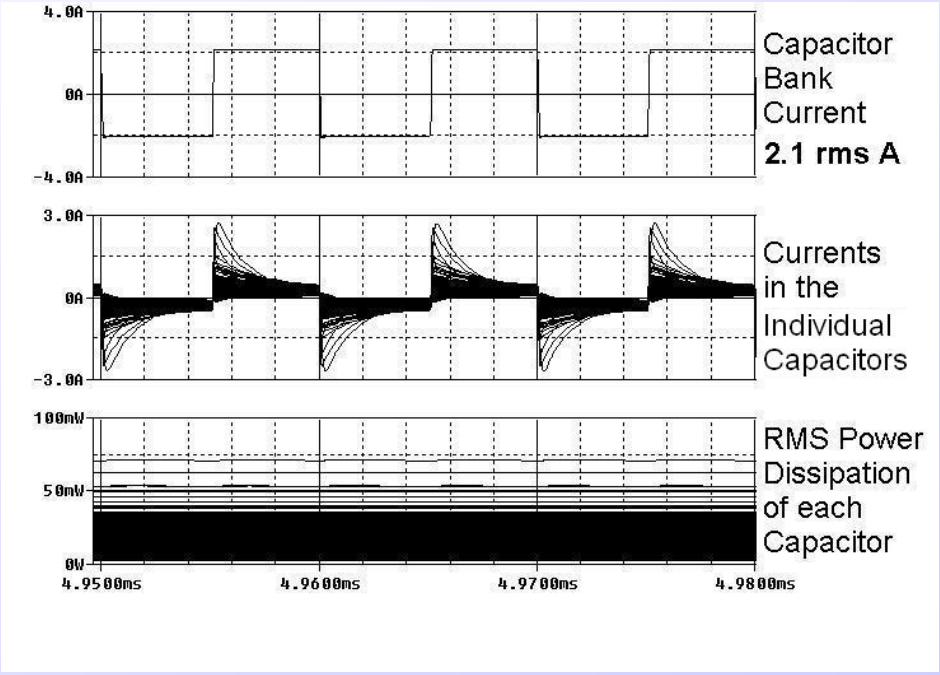
3. Capacitor Used in parallel Configuration

a. Issues of utilisation (9/11)

-> Which Impedance model of each capacitor can be used?

- **Simple RLC series model to perform a Worst Case Analysis**

Results: 2.1 Arms for the capacitor bank
Drawback: based on RLC models (poorly representative)



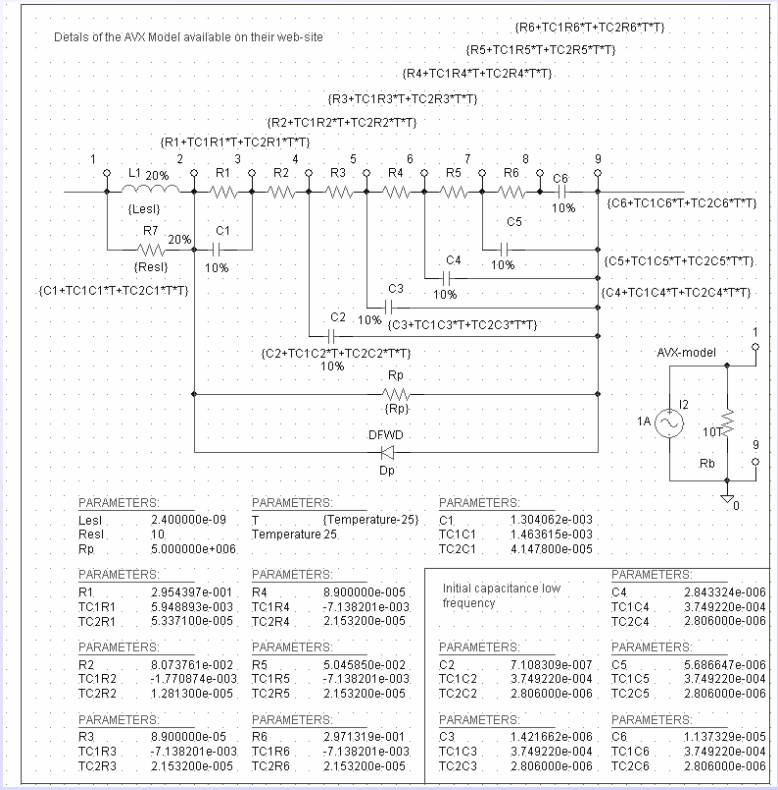
Monte Carlo Analysis with 1000 runs

3. Capacitor Used in parallel Configuration

a. Issues of utilisation (10/11)

-> Which Impedance model of each capacitor can be used?

- **AVX model**



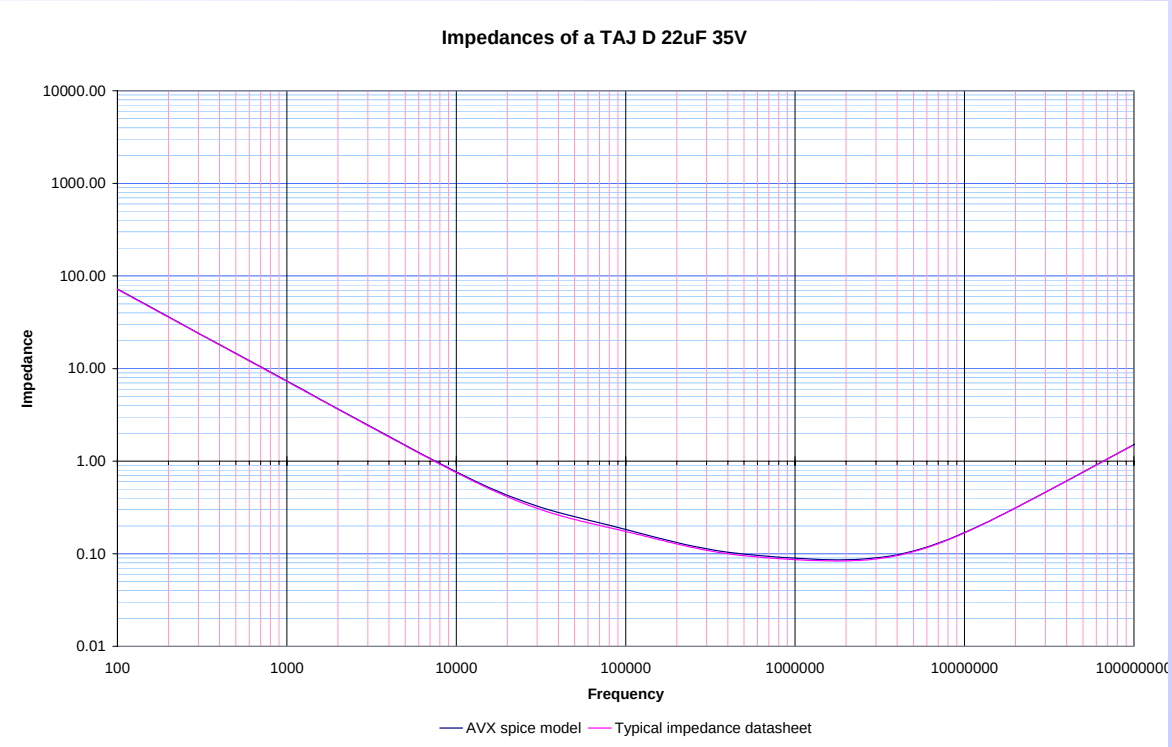
3. Capacitor Used in parallel Configuration

a. Issues of utilisation (11/11)

-> Which Impedance model of each capacitor can be used?

- **AVX model**

Results: WC analysis is not possible if the range of variation of individual model elements is not known
Advantage: accurate model (wrt typical impedance given in the datasheet).
Drawback: the range of variation of individual model elements is not known



3. Capacitor Used in parallel Conf

a. Issues of utilisation (

-> Which Impedance model of each capacito

- **AVX model**

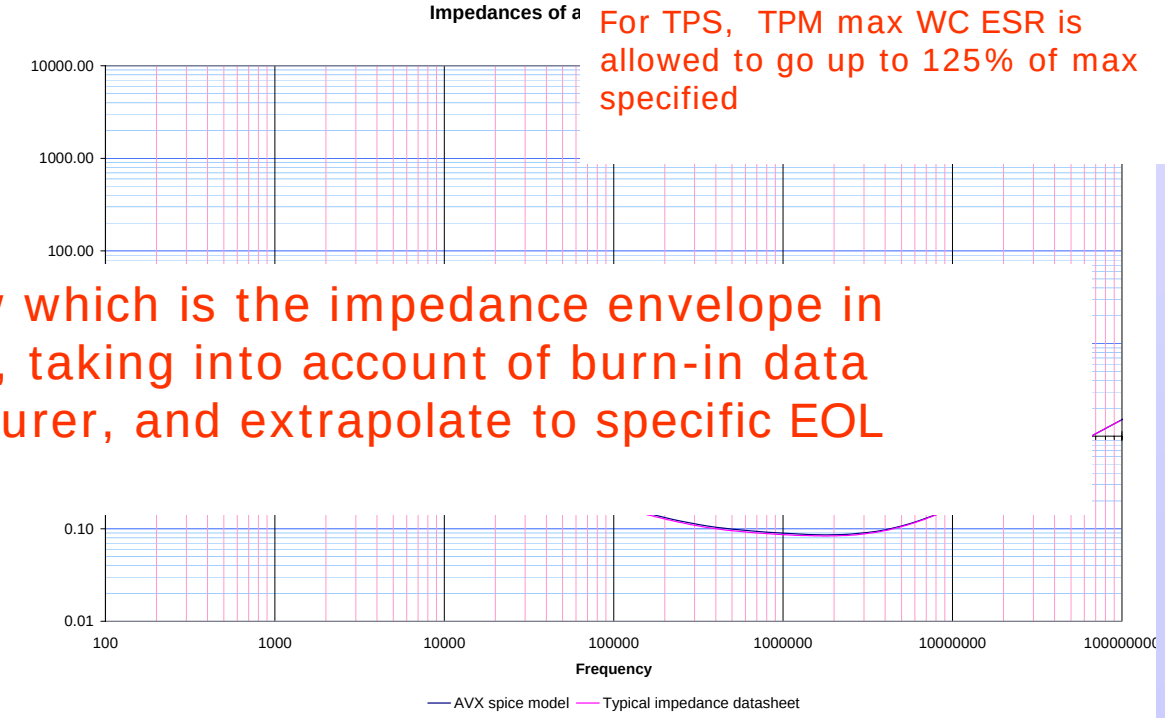
Comment by AVX

On L-R-C series model

Try to reduce ESR min by 20% wrt typical and ESR max equal to datasheet.
LSR put from 50% to 200% of typical.

For TPS, TPM max WC ESR is allowed to go up to 125% of max specified

Results: WC analysis is not possible if the range of variation of individual model elements is not known



Q4: Is it possible to know which is the impedance envelope in function of the frequency, taking into account of burn-in data available to the manufacturer, and extrapolate to specific EOL conditions?

3. Capacitor Used in parallel Configuration

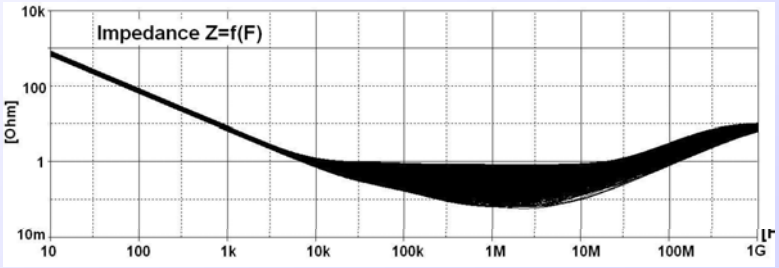
a. Issues of utilisation (11/11)

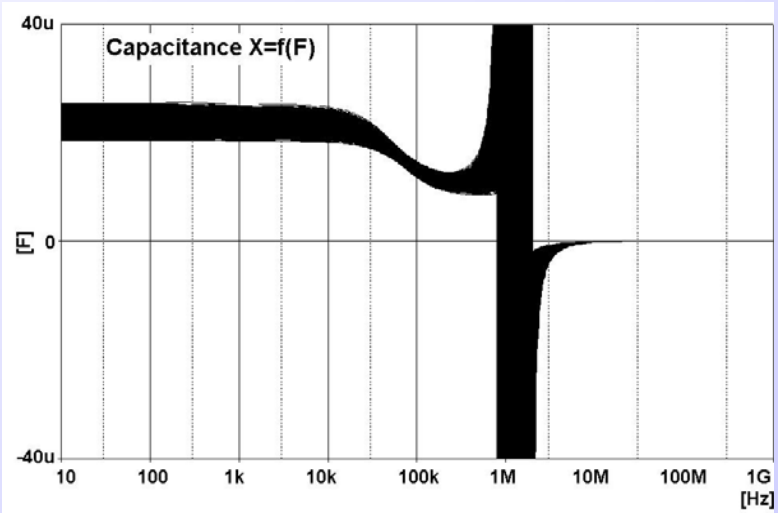
-> Which Impedance model of each capacitor can be used?

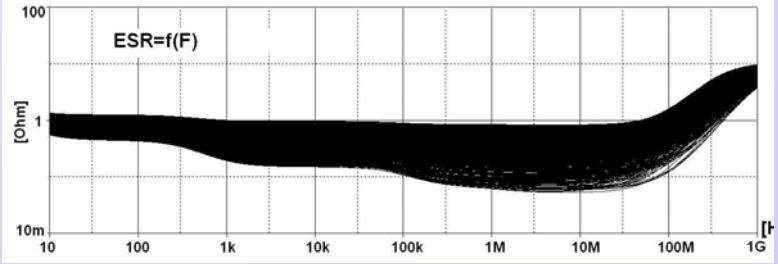
ESA Statistical model developed around the capacitors AVX model

Laws	ESR at 100kHz	ESL	X at 100Hz
Typical	139mOhms	2.4nH	22uF
Range of possible values of the model	[80% of the typical ESR, ESR max*]	[50% of the typical ESL, 200% of the typical ESL]	Initial Tolerance +/-20%
Values	[111mOhms, 900mOhms]	[1.2nH, 4.8nH]	[17.6uF, 26.4uF]

* ESRmax is the max at 100kHz given by AVX







3. Capacitor Used in parallel Configuration

a. Issues of utilisation (11/11)

-> Which Impedance model of each capacitor can be used?

ESA Statistical model developed around the capacitors AVX model

Results: 2.2 Arms for the capacitor bank

Drawback: model only for AVX capacitors

Outline of the presentation

1. **Objectives of the Test Campaign**
2. **Initial Characteristics**
3. **Individual Capacitors Tests**
   a. Limit of Utilisation
   b. Tests performed on single capacitors
      . *Surge Current Tests*
      . *Over-voltage Tests*
      . *Over-current Tests*
4. **Capacitors Used in Parallel Configuration**
   a. Issues of Utilisation
   b. Tests Performed on different capacitor banks
5. **Conclusions**
6. **Questions and Discussion**

3. Capacitor Used in Parallel Configuration

b. Tests performed on different Capacitor Banks (1/5)

General Conditions of stress

- 4 capacitor banks of 10 caps TAJD 22uF 35V were stressed at **85°C** ± **3°C** , ambient pressure, and **de-rated voltage** (21V).
- Another CB (CB13) was kept as a **reference** and not stressed.

- The frequency of operation of the converter to generate the RMS current through the capacitor bank was **131 KHz** ± 5%.
- Each capacitor bank was tested for overall leakage current and impedance at the beginning of the test campaign (after the soldering process) and at fixed intervals during the life testing (every 100 hours).

3. Capacitor Used in Parallel Configuration

b. Tests performed on different Capacitor Banks (2/5)

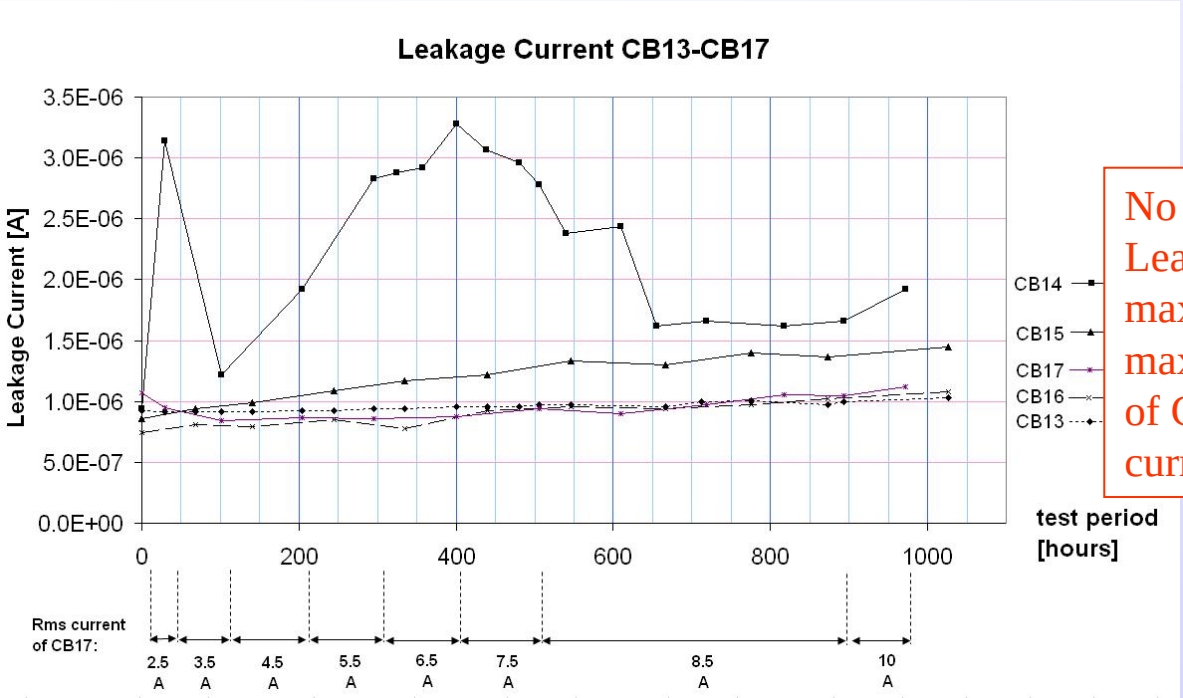
Specific Conditions of stress

- CB13 was kept as a **reference** and not stressed.
- CB14 was stressed continuously at **7Arms**.
- CB15 was stressed continuously at **2.5Arms**.
- CB16 was stressed by **intermittence** (period on: 2.5 minutes stressed, 2.5 minutes not stressed, off) at **2.5Arms**.
- CB17 was stressed continuously at **2.5 Arms**, and then the current was increased **by steps of 1 Arms** after the periodic check (100 hours).

3. Capacitor Used in Parallel Configuration

b. Tests performed on different Capacitor Banks (3/5)

- **Leakage current**



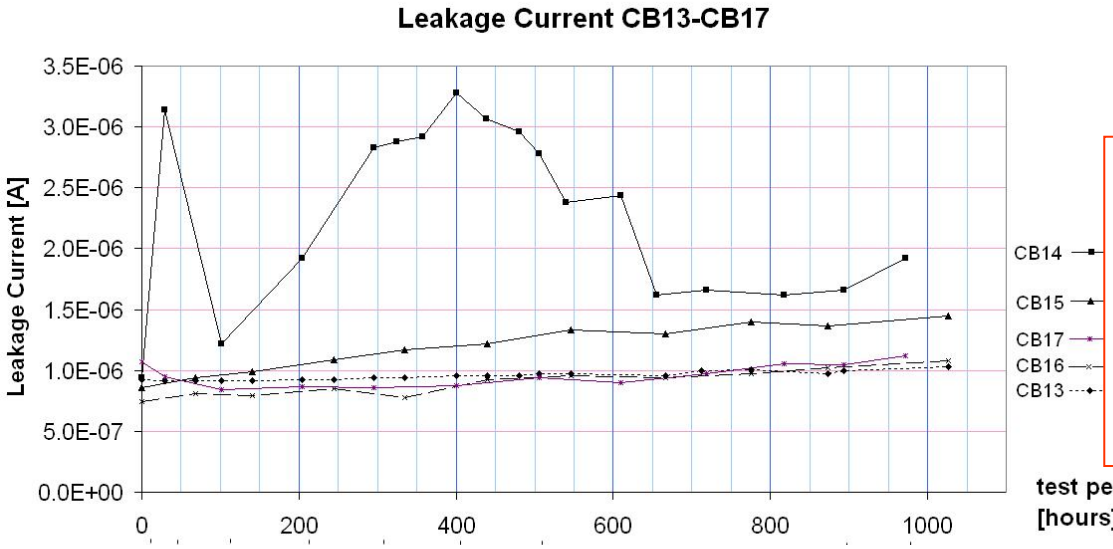
Maximum leakage current: 7.7uA per caps

No failure.
Leakage current always lower than the maximum expected (sum of individual max). Nevertheless the leakage current of CB14 – subject to the highest RMS current - shows rather large variations.

3. Capacitor Used in Parallel Configuration

b. Tests performed on different Capacitor Banks (3/5)

- **Leakage current**



Maximum leakage current: 7.7uA per caps

No failure.
Leakage current always lower than the maximum expected (sum of individual max). Nevertheless the leakage current of CB14 – subject to the highest RMS current - shows rather large variations.

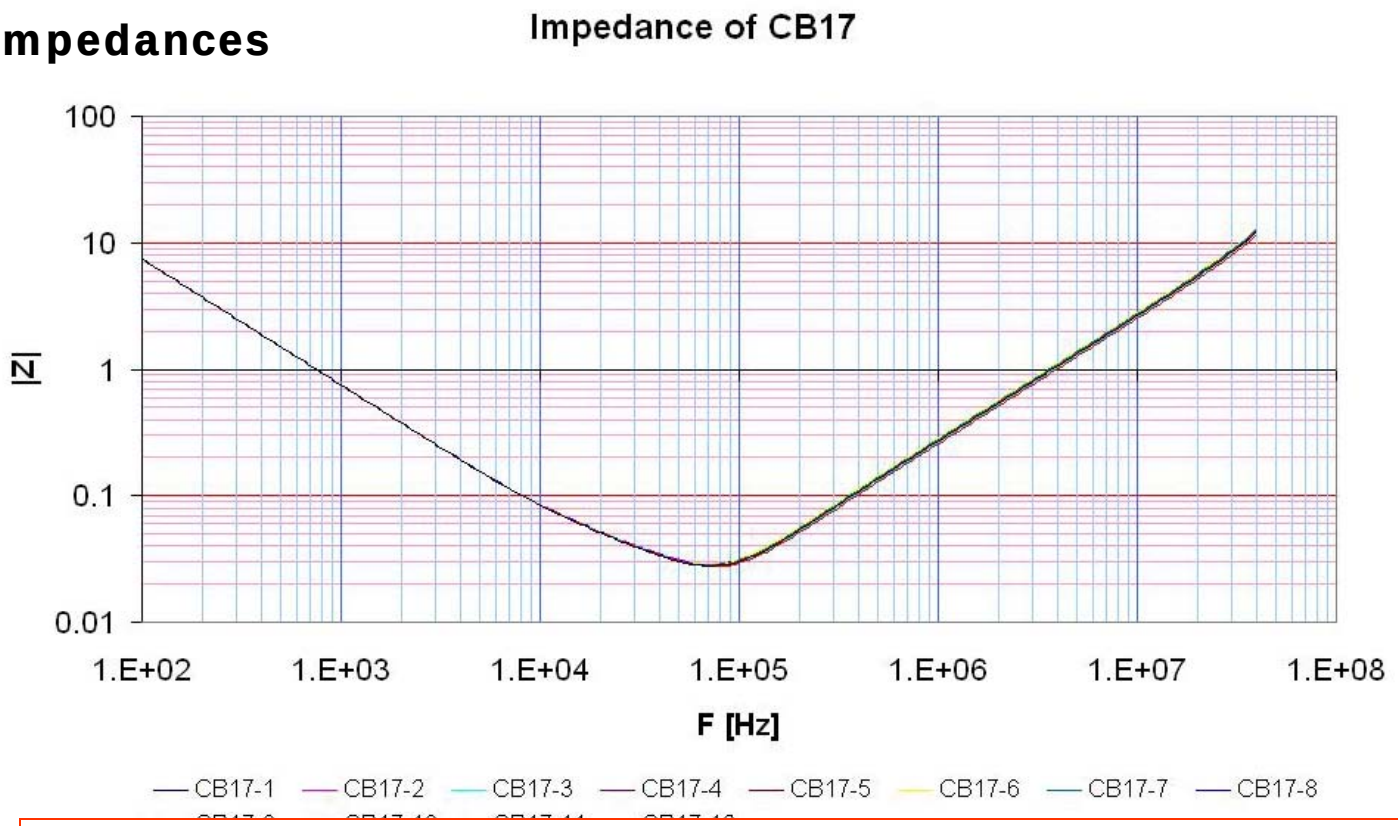
Q5: Why? Can AVX explain why there is a current increase and then decrease? Is there a self healing occurring?

R.: AVX reckons that fluctuation might be self healing

3. Capacitor Used in Parallel Configuration

b. Tests performed on different Capacitor Banks (5/5)

- **Impedances**



The impedances did not change. No major variation was observed.

Outline of the presentation

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5. Conclusions (1/4)

- **Single capacitor tests:**
  - The **surge current test** appears to be an important screening to be performed for hi-reliability space applications. One capacitor failed in such a test.
  - Concerning the **over-voltage** stress, the performances of the capacitor do not get worse until the failure occurs. The voltage failures occurred at >75V, ie **more than twice the rated voltage**.
  - For the **over-current** stress, the performances of the capacitor do **not to degrade when a current up to 4 times** the current corresponding to the rated power dissipation is applied.
  - When the capacitor fails:
    - it fails in **short-circuit** (a few hundred of mΩ).
    - The sound emitted by the capacitor due to a voltage failure is different than the one for a current failure. For voltage failure, a crack is visible on the capacitor: it appears as a dielectric failure. For the current failure, the destruction can be explosive and can damage the PCB on which the capacitor is mounted.

5. Conclusions (2/4)

- **Parallel configuration tests:**
  - No failure was observed during the parallel configuration tests.
  - The impedances remained the same
  - The leakage current of one capacitor bank changed but was still lower than the maximum from the datasheet.
- **In general (1/2):**
  - In absence of detailed impedance data, the **calculation of the maximum current expected on each capacitor in a bank is an issue, and the relevant reliability too**. The very conservative ESR maximum value given by the manufacturer can be used, but the capacitors will be used much below their potential range.
  - All practical and theoretical information to be able to resolve the question marks on the capacitors impedance range **are more than welcome**.

5. Conclusions (3/4)

Comment by AVX

TPM types are recommended for low imp applications, even more than TPS

- **In general (2/2):**
  - The presented tests were performed on only a few capacitors, and for this reason **any generalization** of the results of this study should be **taken with great care**.
  - TPS capacitors, which have a lower maximum ESR, seem likely to be used in the future for space application. For the same volume and weight, they can indeed absorb higher rms currents than the TAJ capacitors.
  - The **soldering process** was not part of this study but may have an impact on the performances of the tantalum capacitors and on the explanation of the failures occurred in ESA programs.

5. Conclusions (4/4)

Comment by AVX

Soldering conditions: at least 30 degC over melting point (185 degC) is recommended now. Recommended is 220 degC; 235 degC maximum can be a proposal.

Officially AVX DOES NOT recommend hand soldering for these capacitors types.
We (ESA) have to think if we have to prohibit hand soldering of TC altogether !!!!

- **Future activities:**
  - Soldering process issues and verification of perfor

    - **Parallel configuration**:
      ”n” capacitor banks will be soldered with 1. slight a
      from the soldering {T,t} envelope recommended by
      checked according to a profile similar to the one applied so far;

    - **Single capacitors, repeated surge current capabilities**:
      ”n” capacitors will be soldered with 1. slight and 2. severe deviation from the soldering {T,t} envelope recommended by the manufacturer and life-checked for repeated surge current pulses application.

Manufacturer comments and suggestions are really welcome!

6. Questions and Discussion