VISHAY SFERNICE

Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chips Resistors and Arrays (P, PRA etc.) (High Temperature Applications)

ABSTRACT

On our thin film chips resistors and arrays the main path for the heat, more than 90 %, is conduction through the body of the component, the solder pad, the PCB and then, from there, convection to the ambient.

Maximum junction temperature and internal thermal resistance of the surface mounted components are the only inputs from the component supplier in the thermal management approach.

All other parameters are in the hands of the equipment designer: Ambient temperature, cooling system, thermal behaviour of the PCBs, maximum temperature of the solder joints etc.

In this technical note we give customers some guidance on the way to get the best from high precision thin film chip resistors and arrays.

THERMAL MODEL
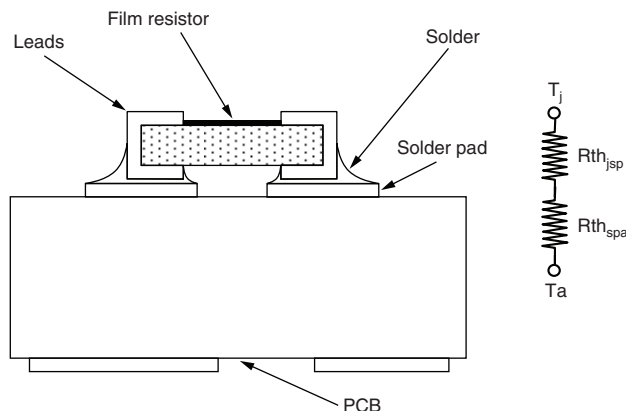
On miniaturized surface mounted components the heat generated within the resistor is removed to the surrounding environment in the following way:

• Conduction from the resistive layer, or junction, through the body of the chip, to the solder pads

• Spreading by conduction within the PCB

• Convection from the PCB to the ambient

The components are so small compare to the PCB that heat removal from direct convection and/or radiation from the resistor body is just ignored in the here below very simple but well recognized model.

1. $T_j = T_a + Rth_{ja} \times Pd = T_a + (Rth_{jsp} + Rth_{spa}) \times Pd = T_a + Rth_{jsp} \times Pd + Rth_{spa} \times Pd$

2. $T_{sp} = T_a + Rth_{spa} \times Pd$

where

• T_j is the temperature of the resistive layer, or junction

• T_a is the ambient temperature around the PCB

• T_{sp} is the temperature of the solder pad, underneath the solder joint, it is almost equal to solder joint temperature

• Pd is the power dissipation of the resistor

• Rth_{ja} is the thermal resistance between the resistive layer and the ambient

• Rth_{jsp} is the thermal resistance between the resistive layer and the solder joint

• Rth_{spa} is the thermal resistance between the solder joint and the ambient

• Rth_{spa} takes into account the conduction within the PCB and the convection from the PCB to the ambient

We can just take care of Rth_{jsp}.

APPLICATION NOTE

Application Note

Vishay Sfernice

Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chips Resistors and Arrays (P, PRA etc.) (High Temperature Applications)

We look carefully about the choice of material, the resistor pattern, the terminations etc.

We are also keen on improving the thermal stability of our resistors, by way of consequence the resistors can withstand higher and higher temperatures without undergoing significant drifts, T_j limitation is pushed away.

The control of all the others parameters, namely T_a, Pd, Rth_{spa}, shall be addressed by customers assembly designers.

They have to take into consideration the PCB material, the thickness and the layout of the copper tracks, the cooling system, the interaction between surrounding components etc.
Their design is more and more computer aided, this is the only way to face the more and more stringent requirements of new electronic equipments in terms of miniaturization, density of power dissipation, temperature exposure, reliability etc.
A poor thermal management might induce:

- Melting of the solder joints

- Lack of reliability of the solder joints

- Loss of PCB performances even burning out

- Loss of chip resistor performances mainly too high reversible or irreversible drifts

This is why thermal management is so important.

DATA

The information from standard chip resistor datasheets, nominal power Pn and derating curves, does not allow customers to take the best from chip resistor.
Moreover this information might mislead them.
In order to allow customers using the here above thermal model we shall provide them with:

- Rth_{jsp} for standard parts and enlarged terminations parts

- Experimental data relevant to chip resistors of standard sizes mounted on various PCBs.

These PCBs have been chosen to be representative of, the standard and the best cases in terms of thermal resistances.

This is mainly to help designers who can not calculate thermal resistance by themselves or to complete their CAD approach.

Meaning of the abbreviations of the here below data:

- PCB sCu stands for a PCB of thickness 1.6 mm, double sided, 35 µm thick copper (minimum), at least 50 % copper coverage both sides

- PCB MCu stands for a PCB of thickness 1.6 mm, double sided, 70 µm thick copper (minimum), at least 80 % copper coverage both sides

- MCM stands for alumina substrates with thick film metallization, at least 50 % conductor coverage. It is equivalent to MCu for the thermal dissipation.

Enlarged wraparound (W/A) are equipped with bottom metallization covering their backside at the exception of a 0.5 mm width insulation path.

Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chips Resistors and Arrays (P, PRA etc.) (High Temperature Applications)

SOLDERED STD W/A

SIZE	Rth$_{jsp}$ (°C/W)	PCB sCu	PCB MCu
		Rth$_{ja}$ (°C/W)	Rth$_{ja}$ (°C/W)
1206	20	110	60
2010	12	95	52
2512	11	95	51

SOLDERED ENLARGED W/A

SIZE	Rth$_{jsp}$ (°C/W)	PCB sCu	PCB MCu
		Rth$_{ja}$ (°C/W)	Rth$_{ja}$ (°C/W)
1206	5	95	45
2010	2	85	42
2512	1	85	41

GLUED STD W/A

SIZE	Rth$_{jsp}$ (°C/W)	PCB sCu	PCB MCu
		Rth$_{ja}$ (°C/W)	Rth$_{ja}$ (°C/W)
1206	33	123	73
2010	18	101	58
2512	16	100	56

WIRE BONDING ON BACK SIDE SOLDERED CHIP RESISTOR

SIZE	Rth$_{jsp}$ (°C/W)	PCB sCu	PCB MCu
		Rth$_{ja}$ (°C/W)	Rth$_{ja}$ (°C/W)
1206	5	95	45
2010	2	85	42
2512	1	85	41

WIRE BONDING ON BACK SIDE GLUED CHIP RESISTOR

SIZE	Rth$_{jsp}$ (°C/W)	PCB sCu	PCB MCu
		Rth$_{ja}$ (°C/W)	Rth$_{ja}$ (°C/W)
1206	10	100	50
2010	4	87	44
2512	2	86	42

Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chips Resistors and Arrays (P, PRA etc.) (High Temperature Applications)

NEW APPROACH FOR DERATING CURVES

First of all it is important to see what pieces of information are contained in the existing surface mount chip resistor derating curves.

- Pn stands for nominal power dissipation, it is the specified maximum power dissipation which can be applied to the component for ambient temperature lower than 70 °C

- The maximum operating temperature the component can withstand, most often 155 °C which is compulsory for military applications

- The way power dissipation shall be derated for ambient temperatures above 70 °C

All the derating curves are a representation of a basic thermal model:

- $T_c = T_a + Rth\ Pd$

- T_c = Temperature to be controlled

- T_a ambient temperature

Pd = maximum allowed power dissipation
Rth thermal resistance between point "c", at temperature T_c, and the ambient.
It can be written:
$Pd = (T_c - T_a)/Rth$
It gives the maximum allowed power dissipation, Pd, for a given ambient temperature, T_a, and a specified thermal path characterized by Rth.
This is the derating curve, a straight line with a slope equal to (- 1/Rth), arbitrarily truncated at 70 °C.

At this point it is important to notice that the Rth appearing on the published derating curves are higher than the Rth of actual assemblies.
This is due to the fact that component manufacturer engineers do not know the way users will mount their components therefore they are taking the Rth relevant to the worst assembly cases.
Like that they are not taking any risk customer wise but they are not optimizing their components use.
In new applications which are more and more demanding in terms of miniaturization this approach is not acceptable.
It is also important to have in mind that for ambient temperatures lower than 70 °C, Pd can be higher than Pn.
Last but not least, a thermal path with a Rth lower than the one coming from the derating curve will allow to get Pd at 70 °C higher than Pn.

When it comes to miniaturize an electronic assembly these remarks shall be considered.

ENLARGED TERMINATIONS FOR LARGEST CHIP SIZE

It seems common sense to use larger chips when it comes to dissipate more power. From the previous calculations and measurements it is obvious that it is not true. A great deal of attention should be paid to the thermal management of the longest chip resistor.

One way to optimize real estate is to use enlarged terminations together with high power dissipating PCB, MCu for example.

To summarize we can have a minimum of - 15 % reduction of Rth_{ja}.

SOLDERED ENLARGED W/A			
SIZE	Rth_{jsp} (°C/W)	PCB sCu Rth_{ja} (°C/W)	PCB MCu Rth_{ja} (°C/W)
1206	5	95	45
2010	2	85	42
2512	1	85	41

Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chips Resistors and Arrays (P, PRA etc.) (High Temperature Applications)

HIGH TEMPERATURE APPLICATION

Design engineers involved in the assembly of high temperature equipments know how to get high temperature withstanding solder joints.

For these applications the main concern is the junction temperature which is the controlling parameter for drifts.
Some orders of magnitude of drifts versus junction temperature, after 1000 h of high temperature storage.

For ohmic value range:
10 Ω to 1.5 MΩ for P1206. 10 Ω to 3 MΩ for P2010:

Vishay Sfernice Thin Film high temperature resistors T° junction (no load)	185 °C	200 °C	215 °C	230 °C
Typical drift at 4000 h	600 ppm	1000 ppm	3000 ppm	3500 ppm
Maximum drift at 4000 h	800 ppm	1200 ppm	3500 ppm	5000 ppm

Typical drift rate after 1000 h storage at high temperature is 1.5 ppm/h.

Load life drift (gold terminations 1000 h)	215 °C
	Typ. 3000 ppm

## EXAMPLE OF POWER CHOICE FOR HIGH TEMPERATURE APPLICATION ON CHIP RESISTOR

Derating curve, $Pd = (T_j - T_a)/Rth$, for a $T_j = 230$ °C and $Rth_{ja} = 40$ °C/W, 50 °C/W and 60 °C/W.
(Forecast drift > 3500 ppm after 1000 h)
These values are achievable through a convenient thermal management.

Example for a chip resistor P2010 high temperature mounted on PCB MCu:

Note

- $Pn = 1$ W for a standard P2010 at 70 °C
  For $Rth_{ja} = 40$°/W we can have the same drift performance = 2000 ppm < typical drift < 5000 ppm for the following configuration:

[1] At 230 °C at 0 W

[2] At 215 °C at 0.38 W = 0.38 x standard Pn

[3] At 200 °C at 0.75 W = 0.75 x standard Pn
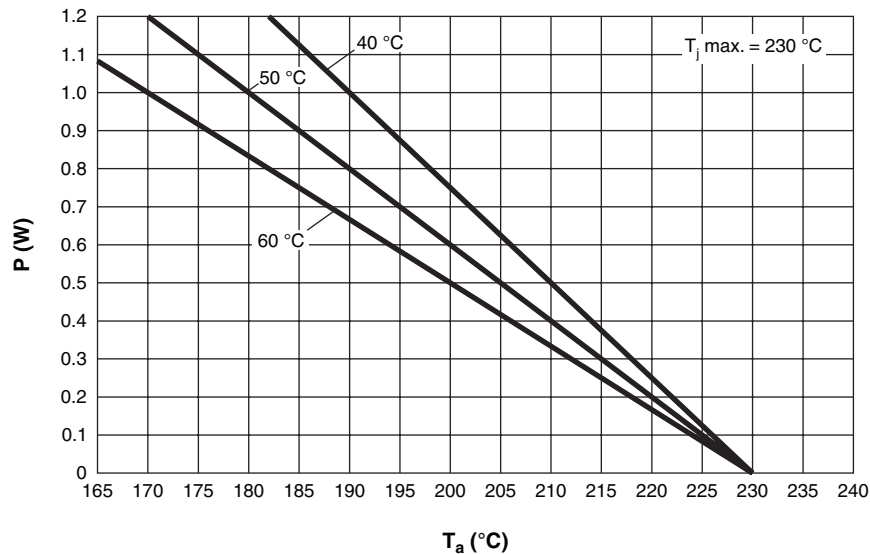
Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chips Resistors and Arrays (P, PRA etc.) (High Temperature Applications)

TERMINATIONS AND REPORTS

Possible high temperature terminations are N (tin/silver: 97/3), G (gold: Less than 1 µm) and L (lead/Ag/tin: 93.5/1.5/5).

Recommended process report:
G and L terminations: HMP process
N: Lead (Pb)-free process