Noise Assessment of Gallium Nitride Structures

CONTRACT 16013/02/NL

Final Short Summary Report

Consortium

THALES-TRT : Prime Contractor
IEMN
IMEC
CRHEA
LAAS
THALES AIRBORNE SYSTEMS
TNO

Redactor : Sylvain Delage, TRT / TIGER
Starting project date : April 1st, 2002
Planned duration : 24 months
Project Completion : December 3, 2004

Date : December 3, 2004
Numéro de page / Page number: 1 / 27
Document: Short Report ESA contract 16013-02-NL Revised Final Version
Ref : TRT-Fr/DCT/TIGER/SLD/04-0077

Summary

Abstract

This project was focused on low noise applications of AlGaN/GaN High Electron Mobility Transistors (HEMT). The Consortium, including 7 partners from 3 countries, was able to develop specific material and components, to carry out low frequency and high frequency noise measurements and modelling. Moreover it has realised dedicated :

- *X-Band robustness aggression tests showing capabilities to withstand from 7W/mm to 40W/mm depending of the device topology. The smaller the device size, the bigger the power density that can be handled.*
- *X-Band low noise amplifiers (LNA) : A one-stage with a noise figure of 1.25dB at 9.6GHz with 10dB gain and a 2-stages with a noise figure of 1.7dB with 20dB associated gain;*
- *X-Band oscillators : Frequency range between 8GHz to 10.6GHz with a moderate phase noise of –84dBc/Hz and –115dBc/Hz at 100kHz and 1MHz of 10GHz carrier respectively.*

Despite difficulties to produce the proper devices inducing planning delays, the Consortium finally was able to demonstrate that this new GaN-based components could be definitely used for low noise microwave applications. The robustness of the components could moreover simplified the architecture of the transmit-receive modules.

The document reviews the technical tasks in the same order as the contract was structured. A synthesis can be found at the end of each demonstrator workpackage.

1. Project Objectives

The aim of this project was to determine the performances of wide band gap AlGaN/GaN HEMT for low noise microwave applications. These components were well known 3 years ago for their advantages in power applications listed below :

- increased power levels compared to standard semiconductor technologies
- higher operation voltages leading to reduce losses and wider bandwidth by easier matching thanks to higher output impedances.
- improved EMP hardness
- higher temperature range
- chemically more inert
- The two latest advantages should lead to higher device reliability.

High power microwave transistors and amplifiers using nitride materials could be therefore used in many different Radar and communication systems.

In 2000 the use of such compound semiconductor devices for low noise applications was disclosed (noise in the 0.5dB range at 10GHz both demonstrated by Hughes Research laboratories and Marconi Caswell Limited[1]).

The impact of power device offering low noise capabilities is quite important. One could indeed expect to be able to simplify the transmit-receive chain by suppressing the input protection. The behaviour of power handling of GaN associated to excellent thermal effusivity should allow a reception amplifier to withstand electromagnetic aggression. Moreover, one has to remind the reader that GaN or SiC materials are much less sensitive to the creation of e-h current generation due to their wider band gap, which is important for space applications.

In this project we did want to evaluate both HEMT grown on sapphire (MOCVD IMEC material) and more advanced HEMT grown on resistive silicon substrate (MBE CRHEA material)[2]. These two centres had demonstrated material quality close to the worldwide state of the art in 2001. The process was based on the TIGER Thales-IEMN common laboratory expertise. The electrical characterisation was made either by LAAS (low frequency noise – LF) or by IEMN for the high frequency noise (HF). Finally TNO was in charge of the X-Band oscillator design and realisation, while Thales Airborne (TAS) Systems was in charge of the realisation of a detection amplifier and robustness tests.

The Figure 1 shows the programme structure as defined initially. The WP1400 was only a chip delivery work package. WP2000 was focused on the detection part, while WP3000 was dedicated to the oscillator work.

[1] ESA meeting, October 18th 2001, « Athena project » by Ingrid Moerman and Zahia Bougria (INTEC)
[2] ESA meeting, October 18th 2001, « Might project » by M.A. di Forte-Poisson and S.L. D[illegible]e (T[illegible])

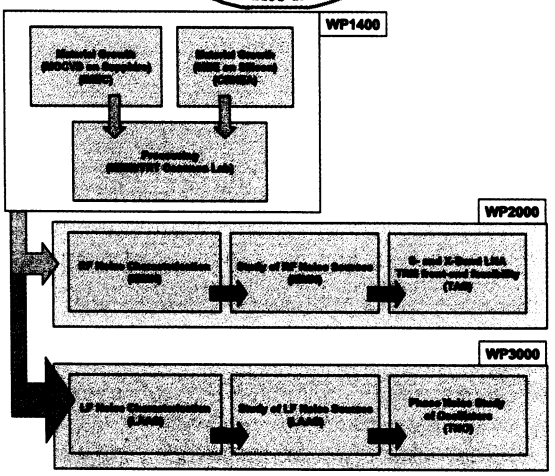


Figure 1. Programme flow

2. WP1400 Device delivery

The Consortium worked first on HEMT grown on sapphire and silicon substrates.

2.1 Material aspects

The project aimed to check the low noise performances of HEMT grown on sapphire and silicon substrates. The deliveries from IMEC and CRHEA were filling this requirement. Later on, various difficulties obliged the Consortium to re-orient towards the use of HEMT on silicon carbide substrates. TRT/TIGER MOCVD wafer was used for this purpose. In this part we review the three different sources of materials we used. This is carried out in the spirit of the project, meaning the review is based on the status at a given period, which can be the situation 3 years ago or last year.

2.1.1 GaN HEMT on sapphire substrates by MOCVD (IMEC)

A Thomas Swan MOCVD reactor fitted with a load lock and a glove box was used. It was largely described in the frame of ATHENA project. This new system was commissioned during October 1999 and since then has provided all IMEC material for processing by the partners.

The material was grown on C-plane sapphire substrates using ammonia (NH_3), trimethylgallium (TMGa), trimethylaluminium (TMAl) and silane (SiH_4) as precursors and dopant. Prior to the epilayer growth, a thin GaN nucleation layer (NL) was deposited at low temperatures (LT) in order to promote the growth of smooth and single-crystalline epilayers at high temperatures. It was found that the nucleation on sapphire could take place at T_g as low as ~410°C and that the growth rate increased up to a saturation value at ~ 480°C (the boundary between surface kinetic and mass transport limited regimes).

Dense two-dimensional electron gas (2DEG) are created at the triangular QW at the AlGaN-GaN interface. The 2DEG could be tailored through the growth of intentionally undoped AlGaN-GaN heterostructures with $6\%<x_{Al}<36\%$. The sheet carrier density (n_s) could be tuned from $4x10^{12}$ cm^{-2} to $1.7x10^{13}$ cm^{-2}. The 300K density n_s was found to follow an empirical linear law as depicted Figure 2 : $n_S = 4.9x10^{13} * X_{Al} - K$ (the constant K was for instance $3.5x10^{12}$ cm^{-2} for 28 %Al). This trend was fully consistent with theoretical predictions explaining the induction of the 2DEG by piezoelectric and spontaneous polarisations.

The Figure 3 shows IMEC data showing the 2D mobility versus the sheet carrier density. The samples processed in the frame of this project were stemming from this "vintage".

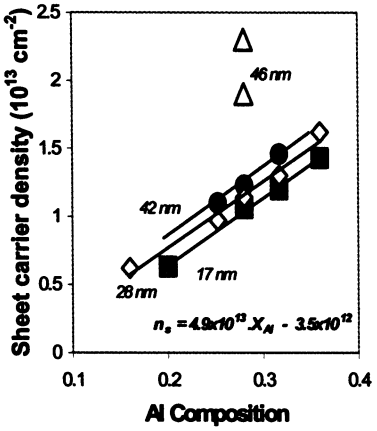


Figure 2. Sheet carrier density versus Al composition (IMEC)

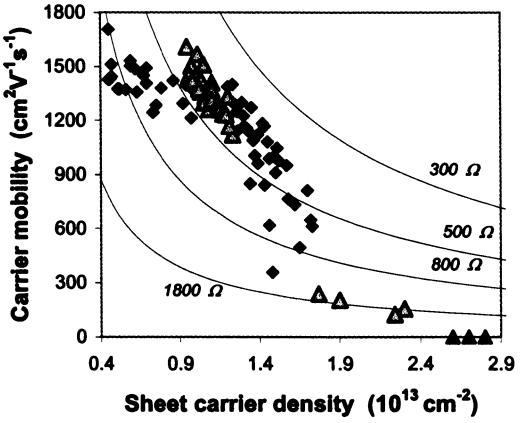


Figure 3. 2DEG mobility versus sheet carrier density. The triangles correspond to the 28%Al series.

2.1.2 GaN HEMT on silicon substrates by MBE (CRHEA)

CRHEA used for their growth of GaN on Si a Molecular Beam Epitaxy system Model Compact 21 from RIBER with a capability of 1x2" substrate. It was equipped with six cell ports and one NH_3 cracker cell. A turbo-molecular pumping unit with a speed of 1200l/s was connected to the system. In-situ growth mode and rating were available by RHEED and reflectivity. CRHEA was one of the first team to work on GaN on silicon substrate for microwave applications. This approach is important for catching low cost market by processing large surfaces up to 100mm diameter. High resistivity silicon substrates were already available and offering a thermal conductivity 3 times better than sapphire. This approach could also be mixed with substrate removal and wafer-bonding. Due to the hexagonal surface required for GaN crystal, it was however required up to now to use <111> oriented Si substrates, which is not a standard orientation.

In order to grow on silicon <111>, a specific scheme was introduced in the GaN buffer to handle a lattice mismatch of –17% and a thermal mismatch of 139%. AlN layers were introduced in the GaN buffer to limit the stress (Figure 5). The defect density was in the mid 10^9 cm^{-2}, which was above densities observed on sapphire and silicon carbide.

The Table 1 shows the sheet carrier density and Hall mobility at room temperature obtained on silicon as a function of the aluminium concentration of the $Al_xGa_{1-x}N$/GaN heterojunction at the date of wafers delivery.

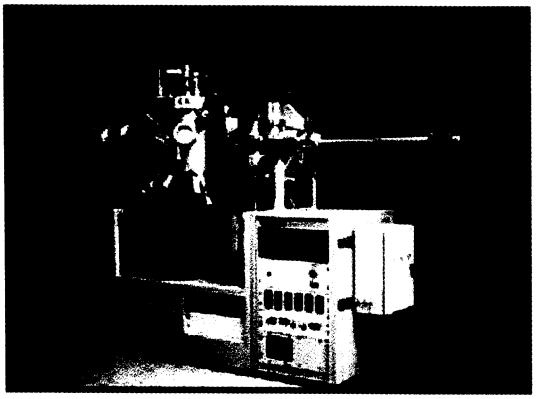


Figure 4. CRHEA MBE system for GaN growth

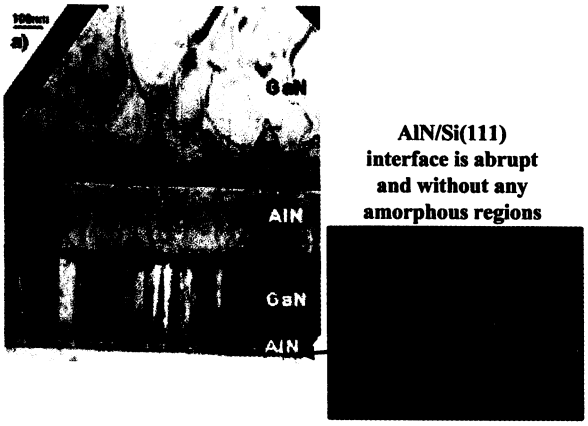


Figure 5. Transmission Electron Microscopy of GaN buffer including 2 AlN layers from CRHEA

	Sheet carrier density Ns (x 10^{12} cm^{-2})	Hall mobility (cm^2/V.s)
x=16%	4.0-5.0	1550-1620
x=20%	5.7-5.8	1400-1450
x=25%	8.3-8.5	1590-1630
x=30%	8.0-9.8	1200- 820
x=32%	1.14*	1240*

(* obtained with a HEMT grown by Picogiga)

Table 1. Sheet carrier density and Hall mobility obtained on Si by CRHEA using MBE versus Al content.

2.1.3 GaN HEMT on silicon carbide by MOCVD (TIGER)

Due to processing and material-based difficulties, the Consortium decided to use HEMT grown on silicon carbide substrates. Non intentionally doped and silicon (Si) doped GaN, GaAlN bulk material and GaAlN/GaN HEMT heterostructures with Al content varying from 22% to 29% were grown at low pressure (50 mb), in an Aixtron RF reactor on sapphire and silicon carbide substrates, using triethylgallium (TEG), trimethylgallium (TMG), Trimethylaluminium (TMAl) and ammonia (NH_3) as groupIII and groupV precursors respectively. The growth procedure on silicon carbide included two temperature steps, but at high temperature (990°C/1150°C). The growth parameters of the nucleation layer (Composition, thickness, growth temperature) and the silicon carbide surface preparation were found to have a clear impact on the material quality of the GaAlN/GaN HEMT structures. The material quality of the epilayers was assessed by various characterization techniques such as Hall and C-V measurements, High Resolution X-Ray Diffraction (HRXRD), low temperature photoluminescence, Transmission Electron Microscopy (TEM), and Secondary Ion Mass Spectroscopy (SIMS). Reflectivity was used in complement to photoluminescence owing to its sensitivity to intrinsic properties of non-intentionally doped (nid) GaN.

The GaAlN/GaN HEMT structures under study consisted of GaN or GaAlN nucleation layers, followed by a 1 µm thick insulating GaN buffer layer, then a 27 nm Si doped or undoped GaAlN layer with 22% Al content, and finally a 3nm thick undoped GaN cap layer. TEM analysis revealed that GaN/SiC interfaces grown showed sharp interface with steps originating from the substrate misorientation (cf. Figure 6), while more ill-defined at higher growth temperatures. Mapping of the sheet resistance($R_\square$ ~ 410Ω) and pinch-off voltage (Vp~-6V) using C-V (Figure 7) and Eddy current probe measurements performed on such GaAlN based nucleation layer HEMT structures reveal a good homogeneity of these electrical characteristics on 2" wafers. A very good crystalline quality of the GaAlN/GaN epilayers with a RMS close to 0.3 nm has been checked by AFM.

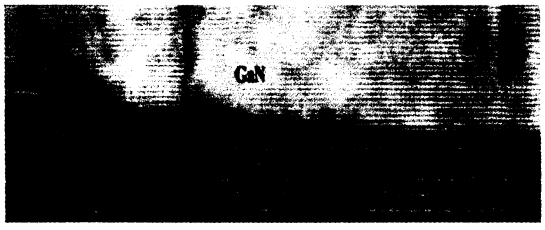


Figure 6. TEM cross section of a GaN/SiC interface (low growth temperature GaN nucleation layer).

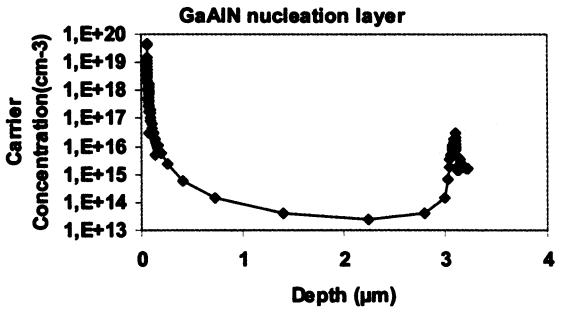


Figure 7. Typical capacitance-Voltage depth profiles of GaAlN/GaN HEMT wafers.

2.2 Processing issues

The kick-off of the project was very closed to the TIGER Thales-IEMN common laboratory creation. This clearly was both an opportunity and a difficulty since the active device processing from both centres was merged and localised in Lille (IEMN). In the mean time the last steps of the process were developed as planned in Orsay (TRT). In 2004 this 2-sites operation is now well running but in 2002 TIGER was heavily charged with many different technical problems.

In March 2003 TIGER issued a document synthesizing its processing status. The results are now in fact one year old and very important progresses have been obtained by TIGER for the last year.

2.2.1 Ohmic Contacts

At this time TIGER compared the ohmic contact quality realised on both sites. The Figure 8 shows the access and specific contact resistance of Ti/Al metal as a function of the place where the steps were carried out. Due to the IEMN equipment specificity, it was decided to use the Ti/Al/Ni/Au recipe developed by IEMN. The access resistances were and are in the 0.2Ωmm range, but with a morphology that should be improved.

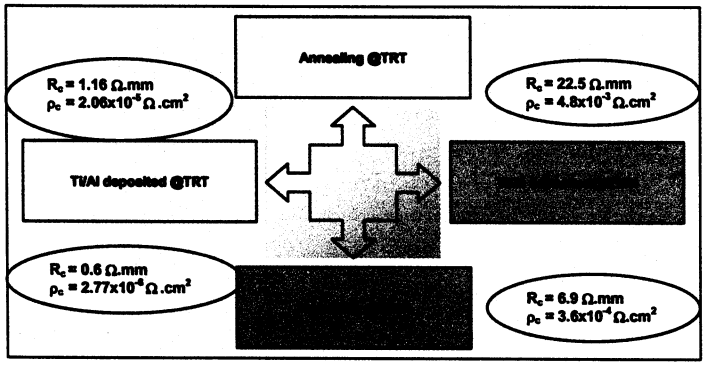


Figure 8. Comparison of Ti/Al ohmic contact quality realised at TRT and IEMN

2.2.2 Schottky contacts :

Different metallisations (Ti, Ni, Ir, Pt) were tested by TIGER to improve the Schottky barrier quality during the first year of TIGER. The Table 2 shows the ideality factor and the built-in voltage we obtained with these metallisations. The values were pretty poor and we had selected Pt/Au or Pt/Ti/Pt/Au contacts, which were the best available. The quality of the Schottky barriers is clearly a mixed between material and processing aspects.

	η	V_b
Ti	9.48	0.358
Ni	3.81	0.450
Ir	2.62	0.523
Pt	3.50	0.496

Table 2. Ideality factor and built-in voltage

Recent wafers, including the wafer AEC1036 used for the final demonstrators on SiC, were using molybdenum-based contacts. This gave rise to a very impressive step towards high quality gate contact. The Figure 9 shows the reversed (up to 100V) and forward (up to 2V) I-V characteristics of a 1µm long Mo/Au gate deposited on a passivated AlGaN/GaN HEMT grown on SiC. The Figure 10 shows the forward characteristics of Mo/Au Schottky diodes as measured on different wafers grown on SiC. Some green curves shows some leakage currents below 0.5V is attributed to surface leakage. The current status on the Mo/Au gates is now a Schottky barrier height of 1 +/- 0.1eV with an ideality factor of 1.7 +/- 0.2. This result is a very important breakthrough compared to the values we first obtained (Table 2).

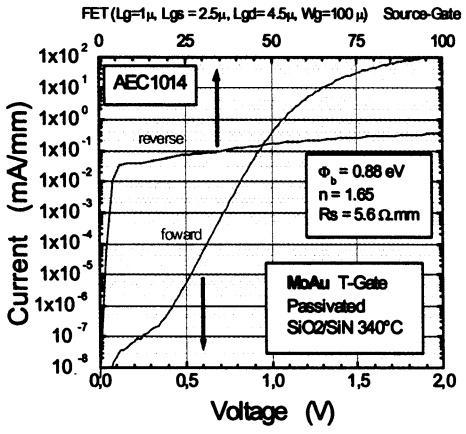


Figure 9. Reversed and forward I-V characteristics of a 1µm x 100µm Mo/Au gate contact.

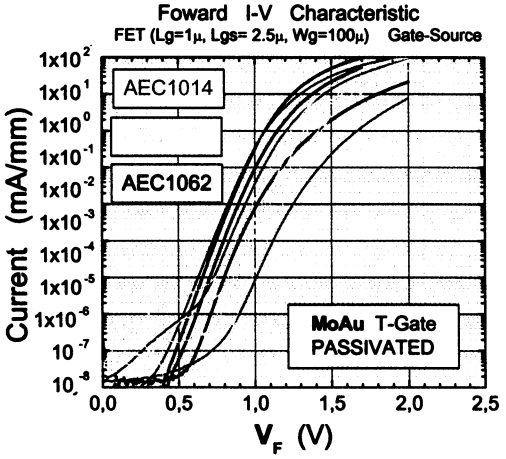


Figure 10. Forward I-V characteristics of Mo/Au gate as measured on 3 different AlGaN/GaN HEMT wafers grown on SiC.

The gate contacts are now using mushroom shape to diminish both resistance and parasitic capacitance. This was not the case for early delivery in this project. The Figure 11 shows a cross-section by focused ion beam of our first 0.15 µm mushroom shaped gate on GaN. The delaminating foils are in fact due to sample preparation for focused ion beam preparation.

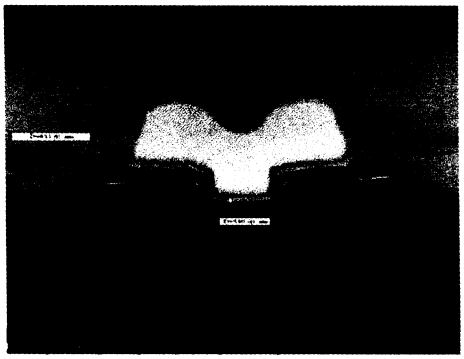


Figure 11. 0.15µm mushroom gate

2.2.3 Device current leakages

Uncontrolled leakage current were a great concern for TIGER research activities. The situation was quite complicated due to the various possible sources of leakage currents.

The Table 3 shows the 5 main sources of leakage currents. Two of them do not induce gate leakage. Our main problems at the beginning of the project was stemming from the very intricate situation. Even if that seems quite trivial when written down, one has to emphasize that, in the middle of turmoil, all the different phenomena seemed quite similar.

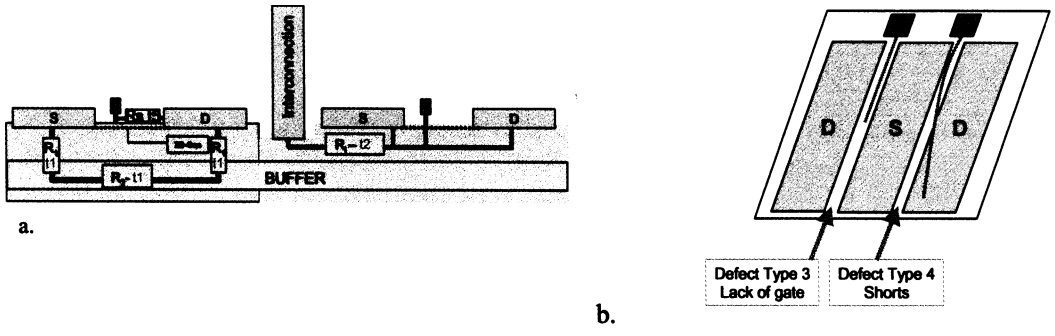
Source of Leakage Current	Defect Category	Origin	Gate Leakage Current	Drain Leakage Current
Leaky buffer	1	Material quality		X
Bad device isolation	2	Processing scheme	X	X
Localised lack of gate metallisation	3	Gate adhesion and/or lithography control		X
Gate-Drain or Source short circuit	4	Gate adhesion	X	X
Device surface leakage	5	Passivation	X	X

Table 3. Leakage types and their effects on the transistor I-V characteristics

The Figure 12 shows the place of the equivalent resistors in the component for the five sources of leakage. Inside the resistors, the type of the leakage is displayed (ti).

The Figure 13 shows the Ids-Vds characteristics we obtained very often up to the end of 2003. This was obtained for most of our wafers. For small transistors the leakage currents were very often in the 10mA/mm to 50mA/mm. In this example, the component can be pinched and one can observed that there is a parallel resistive path to the electrodes. This is typical from the defect 2, which was our main difficulty.

The Figure 14 shows the Ids-Vds of a component obtained using a GaN/SiC wafer from an external supplier. Despite very high power performance, one can observe that above 20V an important leakage current takes place. We believe that some kinds of parasitic conduction path is present in the buffer (defect 1). The RF performances remains satisfactory thanks to an important decrease of the leakage current as the temperature increases.



a.

b.

Figure 12. Schematics of the leakage origins. (a.: t1, t2, and t5 ; b.: t3 and t4)

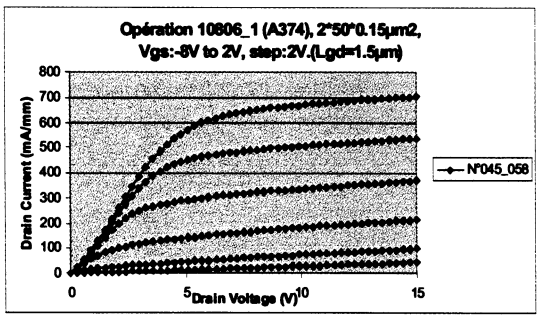


Figure 13. Ids-Vds of A374 GaN/Si wafer from CHREA (defect type 2)

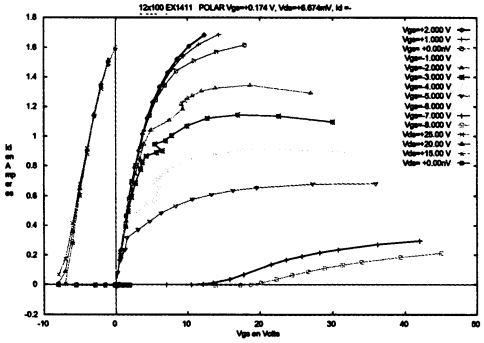


Figure 14. Ids-Vds of a GaN on SiC device showing a defect type 1

The Figure 15 shows the Ids-Vds curve of a component using a GaN on SiC substrate. A soft failure at pinch-off is observed associated to a drain leakage of about 10mA/mm. This failure is observed despite an inter-device leakage below 10µA at 50V based on our simple measurement procedure. In this case the current originated from the surface of the component **(defect type 5)**.

The defect 3 and 4 are more straightforward. A short circuit is quite an easily monitored defect. The Figure 16 shows the photography of a broken gate. This type of physical defect can induce a short circuit or leave a part of the component without any gate control.

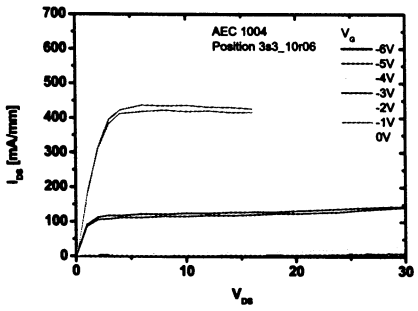


Figure 15. Ids-Vds of a GaN/SiC HEMT - The pinch-off is not perfect despite a high inter-device isolation (defect type 5)

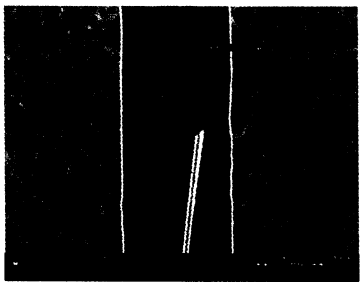


Figure 16. Scanning electron microscopy of a broken gate

From the comparison of different HEMT grown on sapphire, silicon and silicon carbide, it appeared that generally the component obtained on silicon were about 10 times more leaky than the other ones. It has to be stressed that there is unfortunately no general rules. For instance TIGER was able, like some other laboratories, to demonstrate high performance HEMT on silicon. The origin of the higher leakage current on silicon is believed to be of type 1 defect. Indeed at one hand the Figure 17 below shows that the losses on high resistivity silicon substrates are very similar to the ones measured on silicon. At the second hand the RF losses measured on GaN grown on sapphire and silicon using similar device isolation process can exhibit very different loss levels (Figure 18). The Figure 19 shows the Ids-Vds characteristics of one of the best passivated GaN/Si HEMT we got using a Picogiga Int. wafer. The intrinsic transconductance g_m is higher than 350mS/mm for a 0.17µm gate length. It can be clearly seen a not negligible leakage current. The small signal performances are quite good (cf. Figure 20) with f_{max} above 100GHz. The noise frequency is however 0.94 dB at 10GHz, which is to our knowledge a world record using silicon substrate.

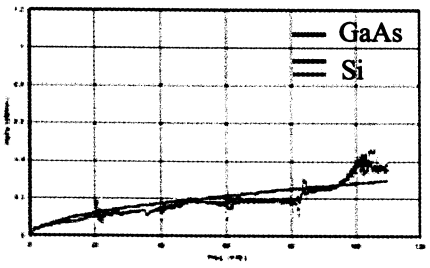


Figure 17. RF losses of coplanar on high resistivity silicon (color lines) and SI GaAs (Black)

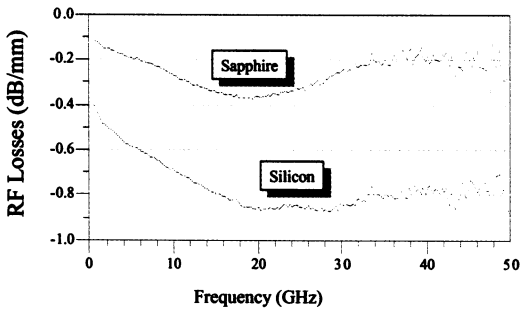


Figure 18. Losses in dB/mm versus the frequency of CPW lines realized both on wafers n°2 (Sapphire red curve) and wafer n°3 (Silicon, blue curve).

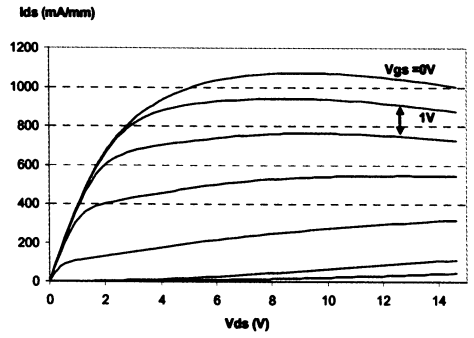


Figure 19. DC (I-V) characteristics to a 2x50µmx0.17µm AlGaN/GaN HEMT (gate to drain spacing of 2.5µm)

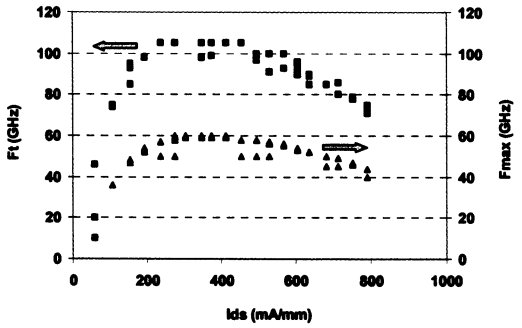


Figure 20. Unity current gain cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}) against drain current for 0.17 x 100 µm2 Vds = 10V and Ids= 235mA/mm.

2.2.4 Sapphire sawing

Effort was carried out to saw component grown on sapphire substrate – The IMEC structures were grown on such substrate. The sawing of sapphire appeared very difficult due to very brittle material. Sapphire appeared much more difficult to saw compared to classical amorphous alumina or even silicon carbide.
Retained conditions corresponding to a 200µm thick blade were those which guarantied the best ratio of dices regardless of the quality of the edge and loss of material. In addition the biggest splinters were on the backside but there was little breakage of the wafer. If the initial trials lead to about 70% chips losses during the sawing even for large size (4x4 mm²), the use of large blades with optimised speeds gave rise to yield close to 100%. The minimum chip size was found to be 1x1mm² but this is the minimum value and could not be use as a standard due to the lack of adherence of the chip on the sticking film during sawing. A reasonable chip size is therefore 2x1 mm².

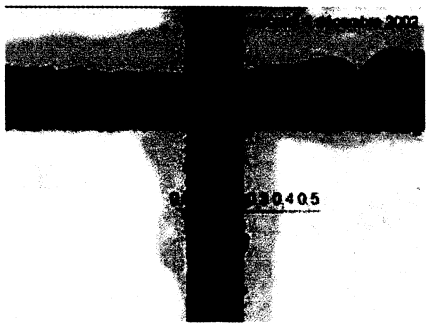


Figure 21. Optimised conditions of GaN HEMT on sapphire using thick blade = 200µm

The sawing of sapphire was therefore not satisfactory if one wanted to realise microwave amplifiers above S-Band. The poor size control requires to use long bonding wire leading to reduce power gain through parasitic inductance. Moreover the lower electrical performances were not a great incentive for designers. This situation pushed us not to use the sapphire substrate for the demonstrator.

2.2.5 Electrical performances of AEC1036 HEMT on SiC

A very important work was carried out in the frame of this project on device manufacturing and characterisation. Technical notes and additional documents describing the studies of the Consortium in electrical characterisation (DC, pulsed, low and high frequency noise, Small signal, etc...) were already presented. We describe here only the devices we finally used for the Low Noise amplifiers and the X-Band oscillator. The devices we used were grown on silicon carbide and were benefiting of the best material and processing schemes TIGER developed at the beginning of 2003. Unfortunately we could not use the devices grown on sapphire (precise sawing difficulties) and on silicon (higher leakage current and low manufacturing yield).

Our passivated components from TIGER wafer AEC1036 on SiC were exhibiting the following performances :

- Very good device isolation (> 1 MΩ) with no losses in the access lines
- Access resistances R_s # 0.9 Ω.mm and R_D = 1.6 Ω.mm – no variation of the access elements versus the frequency
- Good equivalent device scheme determination
- Good Schottky contact – low reverse leakage current
- Good yield (60 %)
- Drop of the I_{DS} current under pulsed measurement showing gate lag and drain lag effect but a satisfying behaviour is observed.[3]
- F_t # 33 GHz ; F_{max} # 100 GHz

The Figure 22 shows the drain and gate current of the TIGER wafer AEC1036 after SiO_2/Si_3N_4 passivation. The gate leakage current remains below 30µA/mm at 30V, which confirms the excellent control of the device manufacturing.

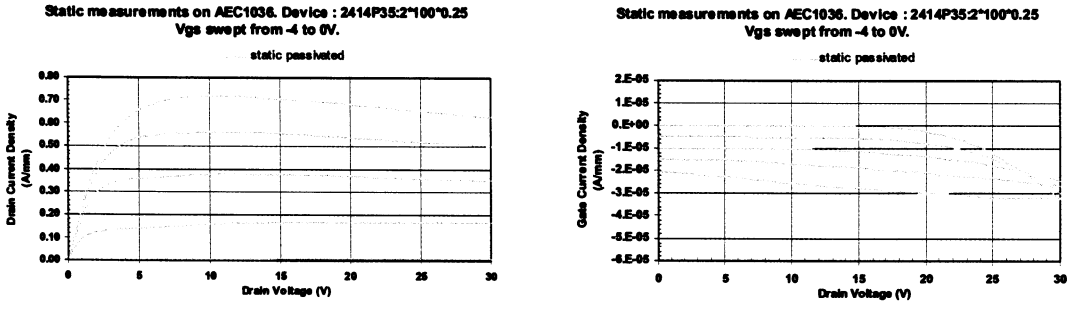


Figure 22. DC electrical performances of a 0.25µm x2x100 µm device from GaN/SiC AEC1036

[3] No precise criterion for lag was up to now defined. A collapse of the Ids-Vds curve smaller than 25% at V_{ds}=25V between pulsed conditions from a quiescent point of (V_{gs} = 0 – V_{ds} = 0V) to (V_{gs} = $V_{pinch-off}$ – V_{ds} = 25V) is perceived as good.

The lag behaviour is a very important feature to estimate the capabilities of components for microwave power capabilities. The Figure 23 shows the pulsed output characteristics of passivated devices at three different idling points (dashed blue: Vgs=0V, Vds = 0V – red line: Vgs=-4V, Vds=0V – green line: Vgs=-4V, Vds=15V). We observed lag effects on this sample. However it is in line with results from other partners in Europe.

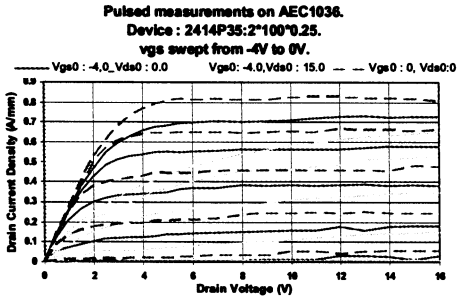


Figure 23. AEC1026 Ids-Vds curves for gate pulse of 600ns, drain pulse : 550ns every 10µs

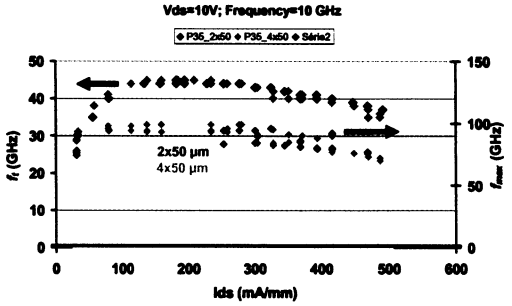


Figure 24. f_t and f_{max} as a function of drain current (AEC1036)

The Table 4 shows the small signal performance of the wafer AEC1036. f_{max} is as high as 110GHz which is an excellent result. The Figure 24 shows f_t and f_{max} as a function of the drain current. The flat response of the 2 figures of merit is quite impressive. The Figure 25 shows the 4 S-parameters as measured and modelled. A very good agreement is observed in the full frequency range (up to 50GHz) and very neat frequency response is observed.

Nom	Topologie (µm²)	Gm_max _dc (mS/mm)	Ft (GHz)	Fmax (GHz)	Rg (Ω) Rm (Ω.mm)	Rs (Ω.mm)	Rd (Ω.mm)
2413P35	2x50x0.15	239	45	110	2.1 252	0.82	1.54
1612P35	4x50x0.15	240	41	110	1 240	0.82	1.58
0823P50	2x50x0.15	232	41	100	2.4 288	0.77	1.45

Table 4. Small signal performance of AEC1036 GaN/SiC component

Figure 25. Measured and modelled S-parameters of 2x50µm AEC1036 devices : left : S_{11} and S_{22}, right : S_{12} and S_{21}.

The Figure 26 shows the microwave noise performances of components measured on the wafer AEC1036. 4x50µm device shows at 10GHz noise as low as 0.8dB.

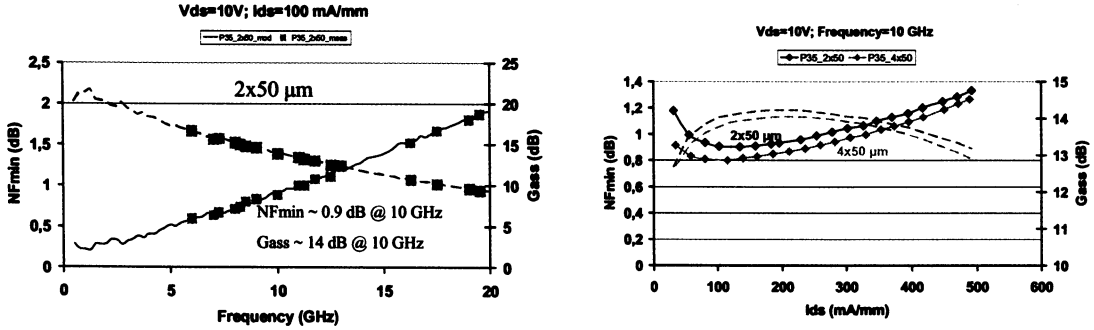


Figure 26. Microwave noise performance as a function of frequency (left) and at 10GHz as a function of the drain current (right)

It has to be stressed that the Consortium reaches most of the targets defined in the project proposal :

- For a 2 gates device (0.5µm – 150µm each) (realised 0.15 and 0.25µm devices)
- Transconductance g_m ~160mS/mm (extrinsic g_m obtained ~290 mS/mm)
- Breakdown voltage > 80V (obtained typically >90V)
- Idss > 0.5A/mm obtained 0.8A/mm
- Gain at 10GHz ~14dB (obtained even at low RF noise condition !)
- ESA target was a RF noise below 1dB at 12GHz. This is obtained only if GaN on SiC epitaxies are used. Best results using silicon substrate was 1.1dB using TIGER process.

3. WP2000 - : Assessment of high-frequency noise figure of components on GaN material

The previous parts show some of the work on RF noise characterisation carried out by IEMN. The technical notes 1 and 2 described the technique used and the raw performances and models developed. The WP2300 was focused on the GaN robustness against electrical aggression and the realisation of low noise amplifier. It was decided in agreement with ESA at mid-term of the project that TAS will focus on the toughest demonstrator at X-Band.

3.1 WP2200 - High frequency noise performance of GaN devices, comparison with other GaN HEMTs.

In the frame of the workpackage 2100 and 2200, IEMN did carried an analysis of the potential of the GaN HEMT for low RF noise applications. This work was carried out at mid-project and are based on data that are now a little bit pessimistic.

We represent at Figure 27 and Figure 28 the best published results in term of noise performance of AlGaN/GaN HEMTs realized on Sapphire and SiC substrates. The Figure 27 corresponds to the minimum noise equivalent temperature at 12 GHz as function of the gate length square. An important figure of merit to design low noise amplifier is represented at Figure 28 by plotting the available associated gain versus the minimum noise figure. It has to be stressed that TIGER obtained using HEMT grown on silicon substrate by Picogiga about 1dB at 10GHz confirming these predictions written in TN2. The Figure 29 shows this latest results[4].

This benchmarking work, in which the Consortium was able to contribute as manufacturing state of the art components for noise applications, is quite important for the future of GaN technology. Indeed it appears that these new materials are offering noise performances very close to classical GaAs pHEMT ones.

[4] "RF Noise performance of AlGaN/GaN HEMTs on Silicon Substrate", V. Hoël, A. Minko, B. Grimbert, E. Morvan, S. Lepilliet, G. Dambrine and J.C. De Jaeger, H. Lahreche, L. Wedzikowski, R.Langer, P.Bove, submitted to Electronics Letters

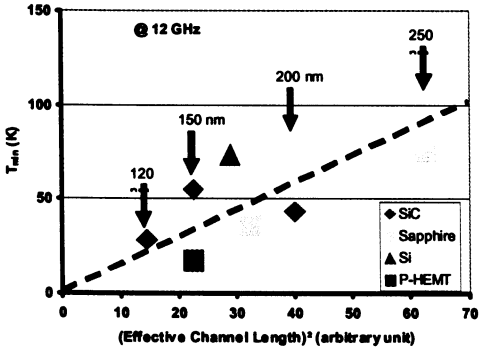


Figure 27. State of the art of T_{min} versus L_g^2 at 12GHz for different GaN HEMTs. The blue triangle corresponds to the estimated T_{min} of GaN HEMT on silicon.

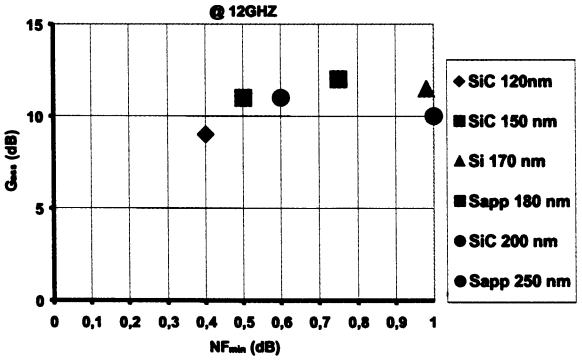


Figure 28. State of the art of G_{ass} versus NF_{min} at 12GHz for different GaN devices. The blue triangle corresponded to the estimated Gass / NFmin of GaN HEMT on Silicon.

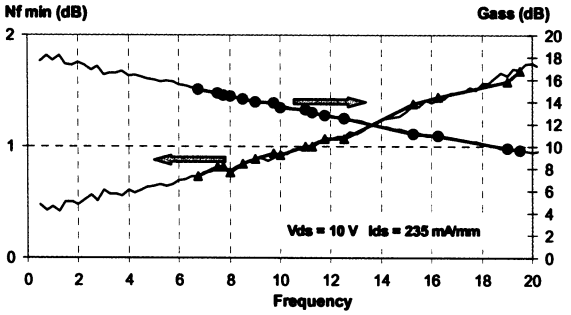


Figure 29. Noise figure and associated gain at 10 GHz versus drain-current I_{DS} of a 2x0.17µmx50µm AlGaN/GaN HEMT grown on hi gh resistivity silicon substrate.

3.2 WP2300 - TRM RF low noise front-end feasibility and perspective

3.2.1 Robustness tests

The Figure 30 shows the block diagram of the aggression test bench that was developed by TAS for the project. The input of the components to be stressed was matched at 50Ω to ensure that all the power emitted by the travelling wave tube (TOP in French) will impinge the component. The Figure 30 shows a photograph of the test set-up. The Figure 32 shows the aggression conditions, which were imposed. Power level of the nominal input signal was fixed at –10 dBm during 30 seconds for minimum noise configuration. A 5 seconds step stress signal was increased regularly from 1 dB by 1 dB step until the device broke down. The Figure 33 shows the evolution of S_{21} after each step stress between 9.2GHz and 11GHz. The component withstand power level up to 34dBm. The Figure 34 shows the effect of the aggression on a 2-gates component. The device was grown on silicon. In all cases the gate melted and sometimes the semiconductor blow out. Increase of the gate cross-section might lead to improve robustness.

The Table 1 synthesises the aggression, which were carried out. 23 components were mounted and stressed by TAS (about 50% more than contractually). The power levels reached up to 40W/mm, and these values decreased as the component size increased. That seems to indicate that a thermal limitation does exist. TAS tried on one sample short aggression pulses but the 4x75µm on SiC component died at 38dBm like the ones stresses for 5". The devices probably died due to both bias and thermal breakdown. It is important to note that the DC bias conditions (3rd raw) didn't display a straightforward relationship with the robustness. To our point of view the GaN HEMT devices present a robustness about 10-20 times higher than the GaAs ones. As a summary :

- Power aggression robustness increases as gate development increases.
- Power aggression robustness is lower at gain compression.
- Time recovery is getting longer as input power increases
- Vgs increases as input power increases, whereas Ids decreases at the same time.

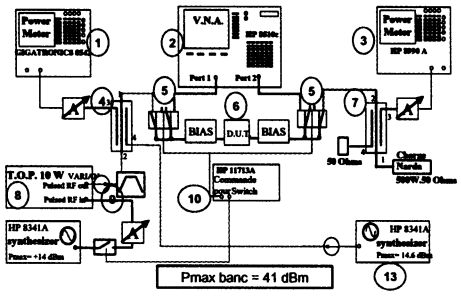


Figure 30. Block diagram of aggression test bench

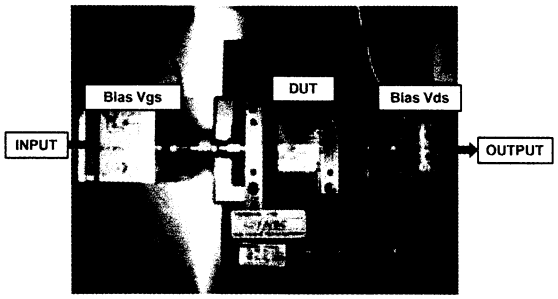


Figure 31. Test bench bias photograph.

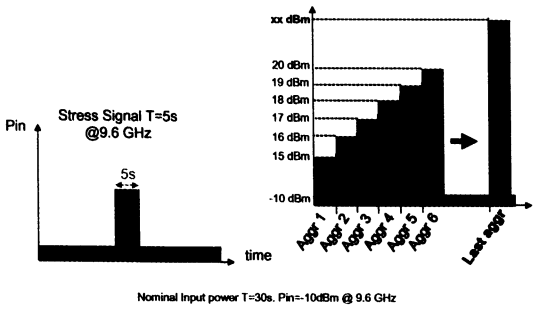


Figure 32. Input signal during aggression tests

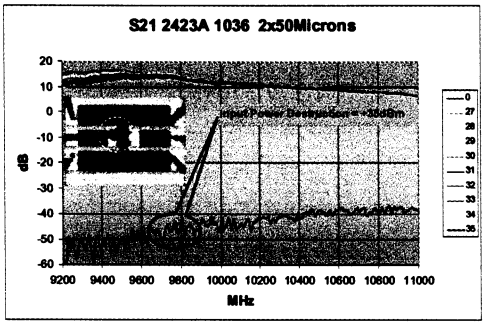


Figure 33. S_{21} parameter of a 2x50µm HEMT grown on SiC (AEC1036 #2423A), at Vg=-3V, Vd=10V during aggression step stress

Figure 34. 46086 Si A379 before and after aggression

Gate development	Layer	Polarization	Mean Power Destruction	W/mm
2x50	A379	Minimum Noise	32,2	17
	1036	Minimum Noise	36	40
	1036	Compression 1dB	33	20
	1036	OFF	35	32
2x100	1036	Minimum Noise	32	8
	1036	Compression 1dB	34	13
	1036	OFF	36	20
2x150	379	Minimum Noise	36	13
	812	Minimum Noise	36,5	15
4x75	1036	Minimum Noise	37	17
		Compression 1dB	33	7
		OFF	35	11
2x250	A379	Minimum Noise	38,5	14

Table 5. Synthesis of the aggression tests (379 : Si, 1036 : SiC, 812 : Sapphire)

3.2.2 Low Noise Amplifier

The Table 6 shows the performances that was targeted for the X-Band LNA to be designed and realised by TAS. 1 stage and a 2 stages LNA were simulated and realized using 4x50µm GaN SiC dices. Simulations were based on data and models from IEMN. Minimum Noise bias points were determined using those data. For the HEMT on SiC, the X-Band minimum noise was reached at Vds= +10V and Id= 28mA for a single dice. A preliminary design was done using ADS software.

	X Band LNA
Center Frequency	9.65 GHz
Frequency Bandwidth	500 MHz
LNA Gain	20 dB
LNA Noise Figure	1.2 dB
LNA Isolation during transmission	50 dB
Power Robustness	12W

Table 6. Targeted performances of X-Band LNA

The Figure 35 shows the photograph of the 1-stage amplifier. The Figure 36 shows the performances of this amplifier from 6GHz to 14GHz. At 9.6GHz the power gain was 10dB and the noise figure is about 1.25dB. It is important to point out that at 7GHz the noise was below 1dB.

The Figure 37 shows the photograph of a 2-stages amplifier. The Figure 38 shows the noise figure of this 2-stages amplifier in the frequency band between 9.4GHz – 9.9GHz. The noise figure is equal to 1.7dB in the defined bandwidth. S_{21} is very close to 20dB in the bandwidth (Figure 39).

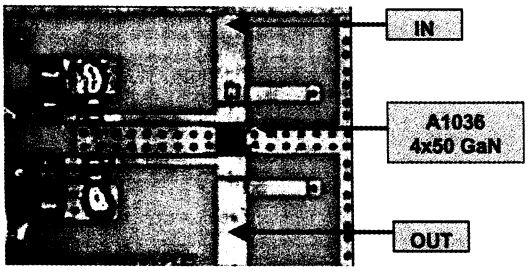


Figure 35. 1-stage X-Band GaN-LNA

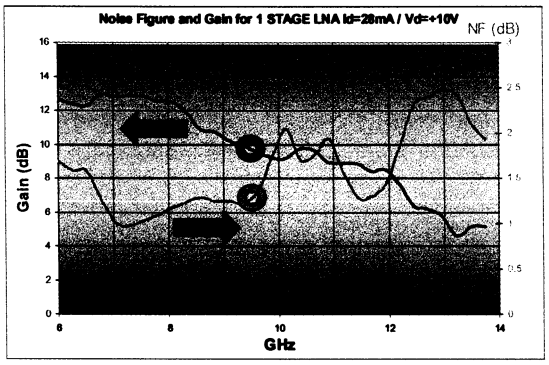


Figure 36. 1-stage X-Band GaN-LNA Gain and Noise Figure Measurements (Vds = 10V, Ids = 28mA)

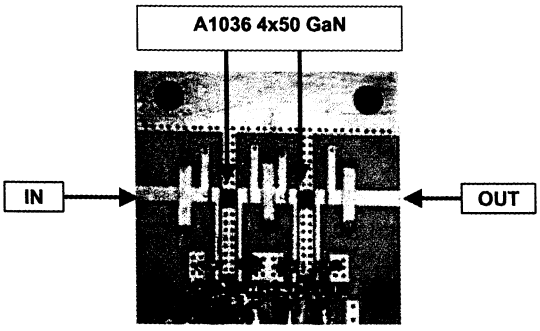


Figure 37. 2-stages X-Band GaN-LNA

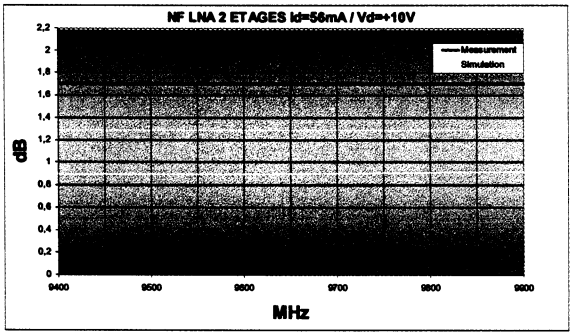


Figure 38. 2-stages X-Band GaN-LNA Noise Figure Measurements

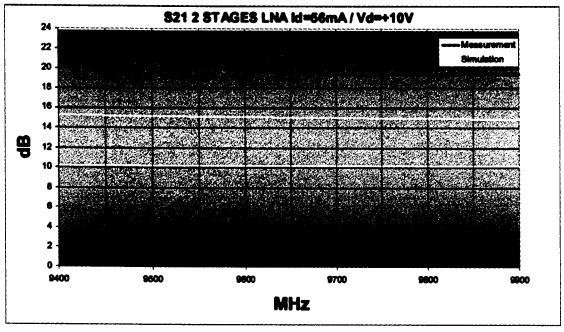


Figure 39. S_{21} measured on 2-stages X-Band GaN-LNA (Vds = 10V, Ids = 56mA)

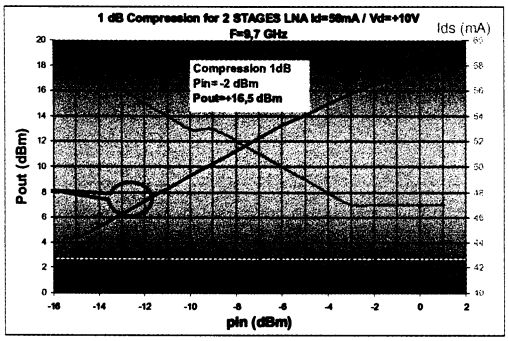


Figure 40. 1dB compression measured at 9.7GHz (Vds = 10V, Ids = 56mA) of the 2-stages X-Band GaN-LNA

3.3 Conclusion of TRM RF low noise front-end feasibility and perspective workpackage

Aggression measurements on GaN device underline a good power robustness.

During high power aggression, GaN device parameters vary:

- Power aggression robustness is lower during gain compression (2 or 3dB).
- Vgs increases as input power increases, whereas Ids decreases at the same time. At destruction input power, Vgs reaches up to –18V.

Power robustness is more important as gate development increases and time recovery is getting longer as input power increases.

X Band GaN LNA preliminary design and prototypes show encouraging noise performances.

In T/R modules, the isolation between transmit and receive paths is carried out by important mass and size switches, isolators or PIN diodes. Generally, the receive low noise amplifier has to be protected against the power leakage during transmit phase and high power pulses coming from the antenna by means of a limiter the insertion of which increases the module noise figure. GaN-based components are known to have very high breakdown voltages (at least one order magnitude higher than similar GaAs components). The objective of this work was therefore to study the feasibility of TRM without any limiter, and with simplified transmit/receive duplexer by using the electrical properties of GaN components (ON/OFF impedance, high breakdown voltages,...), the objective being to suppress any switch or circulator by controlling the TRM only by HPA/LNA bias switching. To establish the feasibility of this TRM architecture, it has been necessary to perform a complete set of overdrive, load mismatch, isolation and ON/OFF input/output measurements on GaN amplifier.

For example, if we have a 10 Watts HPA output power, and if the return loss of the radiating element is about –7dB, we need a LNA which can support 2 Watts without any degradation.

From our work, it seems to be possible for space applications to remove the limiter circuit. This will be true if no invasive external aggression are stressing the receive chain. In case of external aggression that will depend on the value of the input power and also if it is CW or in pulsed mode.

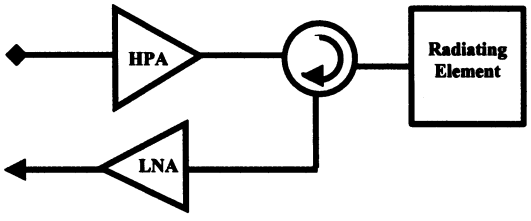


Figure 41. Schematic of a transmit-received module.

4. WP3000 : Assessment of low frequency noise of components on GaN material

4.1 WP3100-3200 : Low frequency noise characterisation

LAAS is involved in this project on the low frequency noise characterisation (TN5 and TN6). They worked mainly on the first components, which were delivered and including quite a high leakage current. They have been able to make a comparison between these early devices and mature GaAs components (c.f. Figure 42). GaN technology is still noisier compared to GaAs, but that should be improved as the material and technology improved.

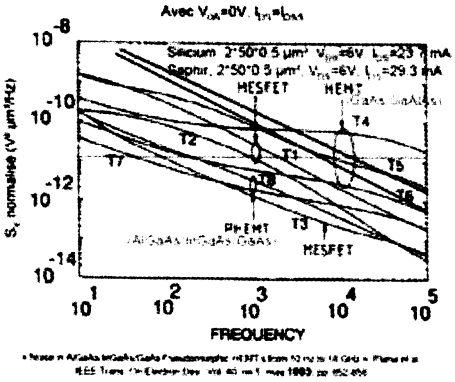


Figure 42. Low frequency comparison (GaAs pHEMT, GaAs MESFET and GaN HEMT grown on Si and Al_2O_3)

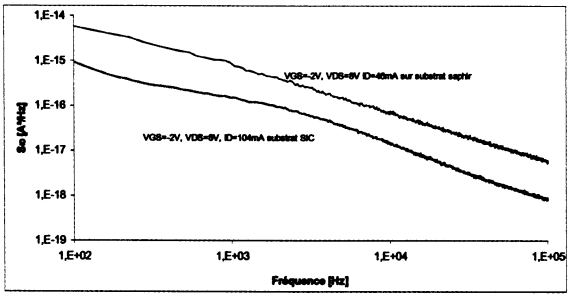


Figure 43. S_{ID} comparison of 2x50x0.15µm HEMT grown on sapphire (Blue curve) and SiC (Black curve)

Recently, LAAS did characterise the electrical and LFN characteristics of our latest generation of components, which used TIGER MOCVD HEMT structures grown on silicon carbide and the improved processing schemes. These devices exhibit all the best properties a LFN scientist and circuit designer could expect. The transconductance g_m is above 230mS/mm. The series resistance R_{on} is equal to 2.5Ωmm. The DC I_{dss} reaches 1A/mm. The pinch-off voltage is close to –5.8V. The standard deviation is below 10%. Moreover the leakage currents are below 0.5µA, i.e. 5µA/mm. This leakage current density is at least 3 orders of magnitude better than the best result we obtained with GaN/Si in the period 2001-2003.

- The Figure 43 shows the same spectrum obtained by LAAS on one 2x50x0.15µm SiC device from AEC 1024 and one similar but grown on sapphire. The same bias points are used but much higher drain current were achieved by the HEMT structure using the SiC substrate. One can see that once again the SiC-based HEMT is one order of magnitude better than the sapphire one.

4.2 WP3300 : Phase noise performances of oscillators using components on GaN material

TNO was in charge of designing and realising a X-Band voltage-controlled oscillator (VCO) using GaN HEMT as active device. The oscillator work is fully described in TN7.

The voltage tuning was done using a MA46H200-1056 hyperabrupt GaAs tuning varactor from M/A-com. The Figure 44 shows the board fully equipped with the active and passive elements. The board material used is RO4003 from Rogers, 20 mil substrate thickness, doubled sided Copper with 0.5 mm plated via's and bondable (2 µm) Gold plating finish. All components are mounted using a manual surface-mount pick-and-place workstation and soldered in a standard infra-red reflow oven. 25 micron Gold bond wires are used to connect the gate, source and drain of the transistor to the tracks. A 6 dB Pi-type attenuator is used to create some isolation to the output connector, avoiding excessive pulling effects caused by the connector and cable mismatch. The RF connector (on the right) used is a surface-mount SMP-type connector. Drain and tuning voltage are connected with wires soldered to the pads on the board.

The Figure 45 shows the evolution of the oscillation frequency and the output power as a function of the varactor bias. The tuning is pretty high for oscillation were measured from 8.1GHz to 10.6GHz. The output power reached about 12.5dBm over this frequency band. This actual output power of the oscillator is 6dB higher for an attenuator was included on the board.

The phase noise has been measured at offset frequencies of 100 kHz and 1 MHz. The average measured values are -84 dBc/Hz @ 100 kHz and -114 dBc/Hz @ 1 MHz offset. The Figure 46 shows the phase noise versus carrier frequency. Only small variations are visible. The small peak occurring around 8300 MHz is probably caused by the changes that occur in the oscillator when the tuning voltage passing the detected RF voltage by the varactor diode (at around 1 Volt.).

The Figure 47 shows as a function of Vdrain the phase-noise level. At bias voltages around +11 Volts, the phase-noise has a minimum of approximately -117 dBc/Hz at 1 MHz offset frequency. With this value, the oscillator compares favourably with existing and published VCO designs using GaAs MESFETs.

The Table 7 shows a summary of the different parameters that were measured by TNO. This oscillator presents right now the advantage of high power and very wide bandwidth.

4.3 Conclusion of low frequency noise workpackage

The Figure 48 shows the phase noise performances of free-running oscillators using different types of transistors. The data which are used were collected in the mid-90s when TRT was involved in GaAs/GaInP HBT oscillators. This figure shows that bipolar transistors in general are much better than field effect transistor for the free-surface has a much lower impact on the current flow. Our result using GaN is surprisingly quite close to the status of 1995, despite the very different maturity of GaAs and GaN HEMT. It has to be also added that recent circuit design development are now able to derive better noise performances than the ones shown in 1995. They need however an excellent noise source description and circuit design than we could use at this very early stage.

As a conclusion it seems that AlGaN/GaN HEMT oscillator could fairly compared to oscillator using GaAs pHEMT. They will have the advantages of robustness and maybe higher bandwidth.

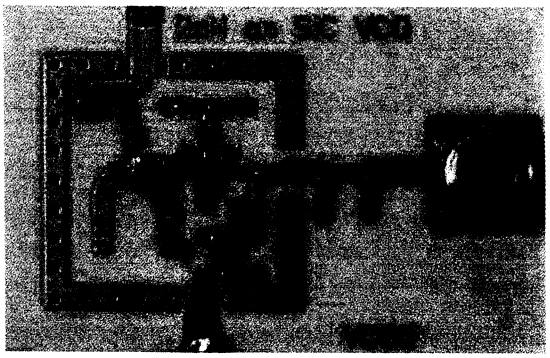


Figure 44. Photograph of X-Band oscillator

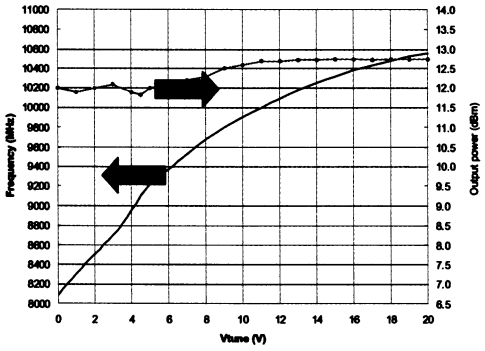


Figure 45. Measured oscillation frequency and output power of the X-Band VCO versus V_{tune} (Vds = 15V – Ids = 37mA)

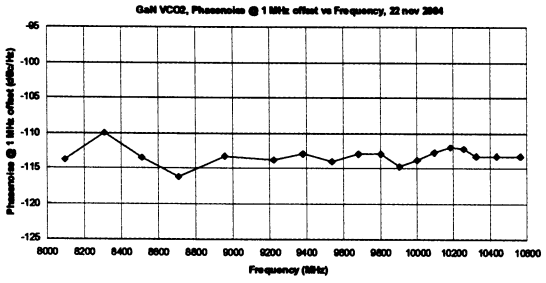


Figure 46. Measured phase noise at 1MHz of carrier of the X-Band VCO versus carrier frequency

(Vds = 15V – Ids = 37mA – Vtune = 0V to 20V)

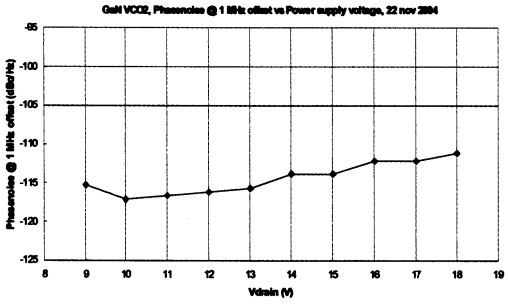


Figure 47. Measured phase noise at 1MHz of carrier of the X-Band VCO versus V_{drain}. Vtune was fixed at 7V.

specification	symbol	min	typ	max	units
Frequency Tuning Range			8.2 - 10.5		GHz
Tuning Voltage @ minimum frequency			0.5		V
Tuning Voltage @ maximum frequency			18.0		V
Tuning Voltage Range		0		22	V
Average Tuning Sensitivity			130		MHz/V
Tuning Sensitivity Ratio			4.5 : 1		
Tuning Linear Modulation Bandwidth		500			MHz
Tuning Port Input Capacitance			10		pF
Output Power Level			19		dBm
Second Harmonic Output Level			-15		dBc
Third and Higher Harmonics Output Level			-25		dBc
Power Supply Voltage			+15		V
Power Supply Current			37		mA
Frequency Pushing			20		MHz/V
Phase-Noise Level @ 100 kHz offset			-84		dBc/Hz
Phase-Noise Level @ 1 MHz offset			-114		dBc/Hz

Table 7. Overview of X-Band GaN-VCO performances

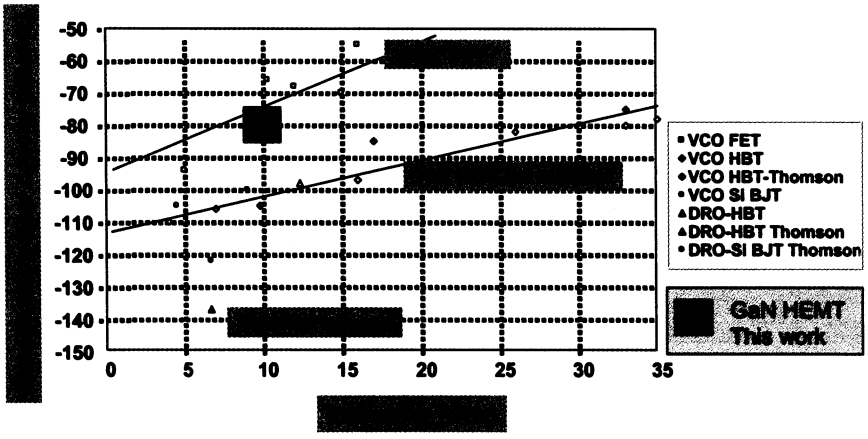


Figure 48. Comparison of free-running oscillators using different types of transistors

This work was possible thanks to the dedication of the staff members of the different research and development centres and the programme leader wants herein to acknowledge the quality of their studies !

TNO report

Technical Note 7: Design and analysis of an X-band VCO using a GaN active device

TNO Physics and Electronics Laboratory

Oude Waalsdorperweg 63
PO Box 96864
2509 JG The Hague
The Netherlands

Phone +31 70 374 00 00
Fax +31 70 328 09 61

Date
December 2004

Author(s)
A.P.M. Maas

Contract no	16013/02/NL/CK
Sponsor	
Affiliation	
Project officer	
Affiliation	
Classification	
Title	
Managementuittreksel	
Abstract	
Report text	
Appendices	
Classified by	
Classification date	-
Copy no	
No of copies	-
No of pages	22 (incl appendices & RDP, excl distribution list)
No of appendices	-

The TNO Physics and Electronics Laboratory is part of TNO Defence Research which further consists of:

TNO Prins Maurits Laboratory
TNO Human Factors Research Institute

Netherlands Organisation for Applied Scientific Research (TNO)

Contents

Abbreviations

AM	Amplitude Modulation
dBc	dB referenced to the carrier-frequency signal-level
dBm	dB referenced to 1 milliWatt
FM	Frequency Modulation
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
MESFET	Metal Semiconductor Field Effect Transistor
MMIC	Monolithic Microwave Integrated Circuit
PCB	Printed Circuit Board
PM	Phase Modulation
RF	Radio Frequency
SiC	Silicon Carbide
SiGe	Silicon Germanium
TNO	Netherlands Organisation for Applied Scientific Research
TNO-FEL	TNO Physics and Electronics Laboratory
VCO	Voltage Controlled Oscillator

1. Voltage Controlled Oscillators

1.1 Specification of a VCO

Several parameters are used to identify an quantify the non-ideal behaviour of a VCO. Depending on the application, the values of some or all of these parameters can be of crucial importance for determining the usability of the circuit.

In table 1, an example is given of a relatively complete VCO specification.

Table 1 example of a VCO specification

parameter	symbol	min	typ	max	units
Frequency Tuning Range					GHz
Tuning Voltage @ minimum frequency					V
Tuning Voltage @ maximum frequency					V
Tuning Voltage Range					V
Average Tuning Sensitivity					MHz/V
Tuning Sensitivity Ratio					
Tuning Linear Modulation Bandwidth					MHz
Tuning Port Input Capacitance					pF
Frequency Settling to 1 MHz					nsec
Output Power Level					dBm
Second Harmonic Output Level					dBc
Third and Higher Harmonics Output Level					dBc
Power Supply Voltage					V
Power Supply Current					mA
Spurious Output Level					dBc
Frequency Pushing					MHz/V
Frequency Pulling into a -14 dB RL load					MHzpp
Phase-Noise Level @ 10 kHz offset					dBc/Hz
Phase-Noise Level @ 100 kHz offset					dBc/Hz
Phase-Noise Level @ 1 MHz offset					dBc/Hz
Phase-Noise Level @ 10 MHz offset					dBc/Hz
VCO Output Noise Floor (>100 MHz offset)					dBc/Hz
Operating Temperature Range					°C
Dimensions					mm
Weight					g

1.2 Definition of oscillator noise

The output signal of any physical oscillator circuit will have noise superimposed on it. This noise can be represented as a relatively small vector rotating more or less independently of the main vector representing the output signal itself. This noise-vector can be split up in two orthogonal vectors, one representing the amplitudevariation and one representing the phasevariation of the signal. This is commonly referred to as amplitude noise and phase noise.
As oscillators are mostly used for timing purposes, phasenoise is ofen used when specifying an oscillator performance.

A frequency independent parameter for the phasenoise is the so-called oscillator number, N_0:
N_0 can be defined as the point of the £(ω_m) curve (dBc/Hz) where $\omega_m=\omega_0$. It gives a carrier frequency independent value for the $(1/f)^2$ part of the phasenoise (does not say anything on 1/f noise or noisefloor, or on the oscillator output power level).

$$N_0 = 20\log\left(\frac{\omega_0}{\omega_m}\right) - L(\omega_m)$$

A formula to be able to make a linear prediction of the phase noise level for a certain oscillator has been introduced by Leeson. Leeson's equation predicts the SSB phasenoise of an oscillator. Below it is shown in an expanded version, including 1/f noise and signal levels:

$$L(\omega_m) = \frac{1}{2}\left[1+\frac{\omega_0^2}{4\omega_m^2}\left(\frac{P_{in}}{\omega_0 W_e}+\frac{1}{Q_{unl}}+\frac{P_{sig}}{\omega_0 W_e}\right)^2\right]\left(1+\frac{\omega_c}{\omega_m}\right)\frac{FkT_0}{P_{sav}}$$

ω_0 = center frequency (rad/s)
ω_m = modulation frequency (rad/s)
ω_c = 1/f corner-frequency (rad/s)
P_{in} = amplifier input power (W)
W_e = energy stored in capacitor/inductor = $(C \times U^2)/2$ (Ws)
Q_{unl} = unloaded quality factor of resonator
P_{sig} = output signal power (W)
P_{sav} = average signal power (W)
F = large-signal noise factor of the active device
k = Boltzmann's constant (J/K)
T_0 = operating temperature (K)

Looking at Leeson's equation, to achieve low noise, choose:
- signal power high
- unloaded Q high
- in-circuit noise figure low
- 1/f corner frequency low

1.3 Noise sources in an oscillator

At each node inside the oscillator circuit, noise will be present. For each node (or branch) there are 2 mechanisms which result in phase or amplitude noise on the output signal:

- additive, this will result in broadband white noise.
- modulation (AM or FM), or upconversion, this will result in sidebands, of which the FM part rolls of with 20 dB/decade versus the offset frequency.

Table 2 noise sources inside the VCO

component	description	mechanism
active element	low frequency noise	modulation
active element	high frequency noise figure	additive
tuning device	equivalent noise resistance	modulation
Resistor	low frequency noise	modulation
Resistor	high frequency noise	additive

Table 3 components or circuit parameters that influence the output noise of VCO

component	description	mechanism
power supply noise	pushing	modulation
power supply noise	isolation	additive
resonator coupling	insertion loss, loaded Q	additive
resonator Q	filtering	additive
active element	in-circuit linear signal gain	additive
active element	rf level / bias dependent parameters	modulation
tuning device	modulation sensitivity	modulation
circuit design	local feedback	modulation
signal level	signal-to-noise ratio	additive

1.4 Transistor technology related noise

The technology dependent noise sources for the active element are:

- 1/f-noise
- in-circuit equivalent noise-figure (Leeson)

The technology dependent noise conversion of the active element:

- bias dependent gain (amplitude and phase) defines to a great amount the upconversion (modulation) of low-frequency noise from both the transistor itself as well as from circuitresistors and powersupplies.

2. Design considerations

2.1 VCO design consideration

A reference VCO design could be used to evaluate the transistor technology. Looking at tables 2 and 3, it can be seen that this will only be possible when the transistor noise sources are the dominant sources when looking at the oscillator phase noise.
In a very wide-band voltage controlled oscillator the equivalent noise resistance of the tuning device, together with the high tuning sensitivity, is often the dominant noise source. Therefore these types of oscillators, although very popular and useful for several applications, are not very well suited for testing transistor technology. However, the noise caused by the tuning device can be characterised by replacing it with a (fixed) capacitor, resonator or inductor with a known or much lower noise level.

Apart from this, the phasenoise due to resistors and the noise from tuning voltage and power supplies should be minimised.
Using a low Q resonator will give rise to higher phasenoise which will eventually mask the noise from all modulation mechanisms.
Generally spoken, a very low phase noise voltage controlled oscillator will not make the evaluation of technologies concerning phase noise easier. To avoid noise from other sources than the transistor from influencing the measurement, a noisy fixed frequency oscillator can be much more useful.

2.2 Transistor performance evaluation

Two basic methods can be used:

1 To evaluate the transistor performance by replacing it with other types in an identical VCO design, and comparing the phase noise performance. This can be thought of as the "50 Ohms noise figure" of a transistor in stead of the minimum noise figure.

- Basic transistor parameters should be equivalent (g_m, C_{gs}, C_{gd}, R_{ds}, etc.) Parasitics should be comparable or negligable.
- The assumption is made that no second order dependencies are present

2 To evaluate the transistor performance by optimising the circuit topology, circuit parameters or bias condition to achieve the minimum amount of phase-noise, using the same resonator. Use bias dependent s-parameters to determine optimum bias condition for low noise-up conversion factor.

- More difficult due to the level of uncertainty in realising the actual minimum noise condition
- Gives a better view on the potential of the transistor technology

2.3 Literature survey

A literature survey has been carried out, investigating the performance of 6 - 14 GHz VCO designs of the past 10 years.

In the table showing the results, a column is added where the phase noise has been normalised for a frequency of 10 GHz, in order to make the comparison between the different VCOs more easy.

Table 4 comparison table 5 to 15 GHz VCO publications with measured performance

ref	Freq. (GHz)	tuning range (MHz)	output power (dBm)	phase-noise (dBc/Hz) 100kHz	circuit type	resonator	active device material / technology	phase-noise normal. 10 GHz	active device type
5	9.0	270	6	-109	hybrid	microstrip	Si	-108.1	bipolar
38	8.9	140	-14	-104	MMIC	off - chip	GaAs	-103.0	HBT
15 *	8.25	900	5	-102	hybrid	microstrip	Si BFP420	-100.3	bipolar
38	8.9	770	-14	-100	MMIC	off - chip	GaAs	-99.0	HBT
2 **	11.8	1100	1	-92	MMIC	on - chip	SiGe	-93.4	BiCMOS
14	11.5	550	11.5	-91	MMIC	on - chip	GaAs	-92.2	MESFET
39	10	1000	15	-90	hybrid			-90.0	FET
7	9.6	1500	13	-91	MMIC	on - chip	GaAs	-90.6	HBT
4 *	9.2	0	9	-90	hybrid		GaAs	-89.3	uPG110
26	9.6	400		-89	hybrid		Si	-88.6	bipolar
26	9.6	400		-89	hybrid		SiGe	-88.6	HBT
72	8.4	150	24	-90	hybrid	patch	GaAs	-88.5	MESFET
24 *	8.2	60	3	-90	hybrid		InAlAs,InGaAs/InP	-88.3	HITFET
1	6.0	600	18-27	-92	hybrid		AlGaN/GaN	-87.6	HEMT
2	11.3	500	-6	-85	MMIC	on - chip	SiGe	-86.1	BiCMOS
73	14.0	2000	11	-75	MMIC	on - chip	GaInP/GaAs	-77.9	HBT
71	11.2	1300	12	-75	MMIC	on - chip	GaAs	-76.0	MESFET
57	9.8	500	19	-65	MMIC	on - chip	AlGaAs/GaAs	-64.8	HBT
70	7.5	1300	10	-63	hybrid		GaAs	-60.5	HJ-FET
61 *	10.2	1800	12	-60	MMIC	on - chip	GaAs	-60.2	HEMT
50	10.4	2000			MMIC				MESFET
47		1300			hybrid				?
45	9.35	300	14		hybrid	microstrip	GaAs		FET

** : only simulated data

* : phase noise level at 100 kHz estimated from higher offset frequency data

3. VCO design

3.1 Introduction

An X-band oscillator is to be designed using Gan on SiC transistor samples from Thales. The samples that are actually used have a gatelength of 0.15 μm and a total gatewidth of 2 x 50 μm.

3.2 Transistor characterisation

A 2x50 μm GaN transistorsample has been characterised on a wafer probe station. The DC curves have been measured, and the S-parameters from 2 to 18 GHz have been measured for several bias conditions.

In figure 1 on the next page, the measured drain current versus gate and drain voltage are shown. The dissipated power has been limited to 700 mW to avoid overheating of the sample.

From the measured s-parameters, the current gain versus frequency has been calculated to find the transition frequency of the device. The result is shown in figure 2.

In table 5 the measured values of the main transistor parameters are given.

Table 5 summary of the measured GaN transistor parameters

parameter	value	conditions	unit
I_{dss}	94	V_{ds} = 6V, V_{gs} = 0V	mA
V_{po}	-5.5	V_{ds} = 12V, I_{ds} = 0.01 * I_{dss}	V
g_m	20	V_{ds} = 12V, I_{ds} = 0.50 * I_{dss}	mS
f_T	22	V_{ds} = 12V, I_{ds} = 0.50 * I_{dss}	GHz
$V_{dg,\ breakdown}$	> 42	V_{gs} = -7V	V

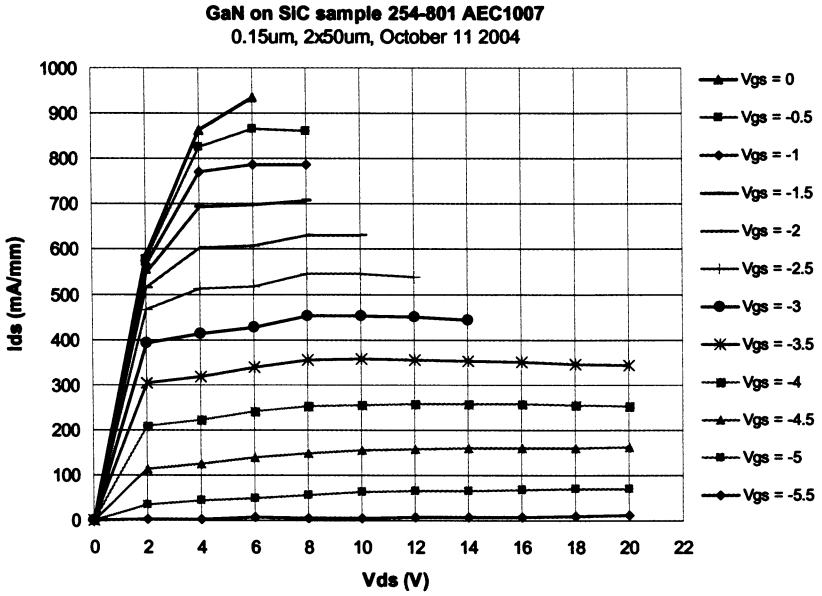


Figure 1 *measured DC I-V curves of the GaN transistor*

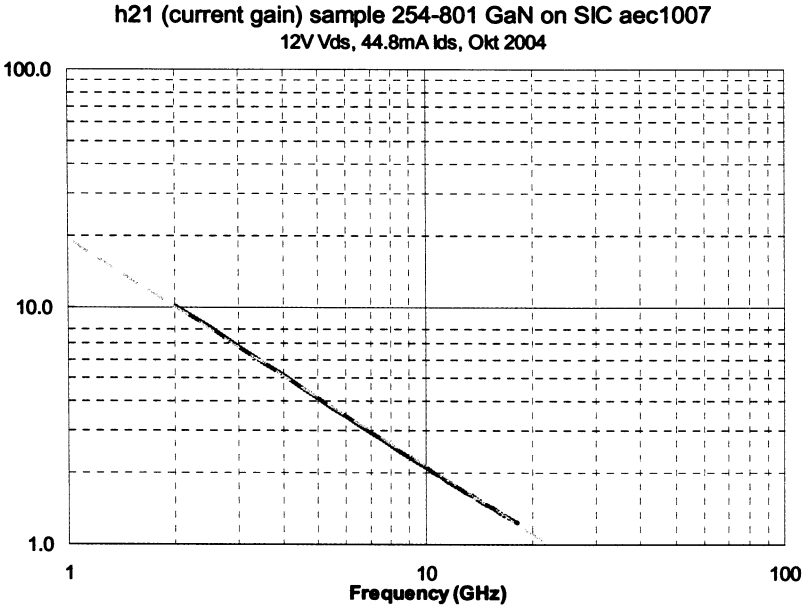


Figure 2 *measured current gain versus frequency, showing a f_T of > 21 GHz*

3.3 Basic VCO design

3.3.1 Oscillator topology

The VCO design is based on a negative impedance approach. The transistor is embedded in a network with source series feedback, creating a negative input impedance at the gate. At the input of this network, a microstrip resonator is coupled to define the frequency and conditions for oscillation. Then the output network is designed for optimum output power efficiency to the 50 Ohms load.

3.3.2 Frequency domain analysis

The Agilent ADS2003c design environment is used for the design. The measured transistor s-parameters are modified in to 6 s-parameter files to model the gaincompression of the device. One original (small-signal) file and then files in which the real and imaginary pasrt of S21 has been decreased in 1dB in steps down to -6 dB. Using the linear simulator and s-parameter models, a first-order simulation of the VCO performance can be made.

In the Smith chart, the intersection of the locus of the reflection coefficient of the resonator vs frequency with the locus of (1/[input reflection of negative impendance]) versus frequency and versus gain-compression can be made visible. In figure 3, the red curve shows the reflection coefficient of the resonator for increasing frequency (direction of arrow) while the green curve equals 1 divided by the input reflection of the active device for increasing gain compression, at a frequency equal to the frequency of the resonator reflection curve at the point where both curves intersect.

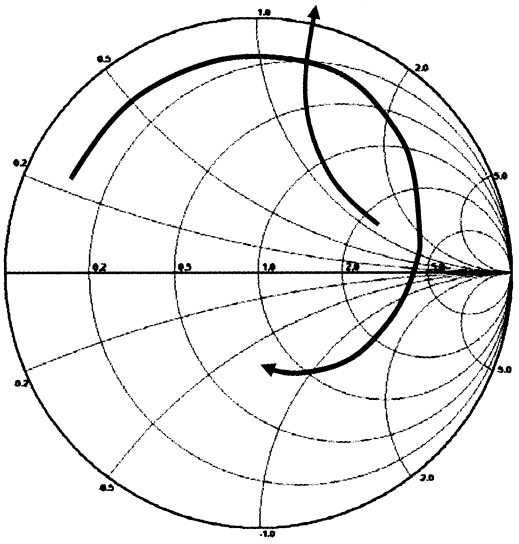


Figure 3 linear analysis of optimum oscillation condition

Optimum conditions for oscillation exist when the 'resonator reflection versus frequency curve' and the 'input reflection vs gain-compression curve' are orthogonal when they intersect, because there will be a minimum amount of AM to PM conversion. The amount of compression of the active device for stable oscillation condition is then easily read from the graph.

3.3.3 Transient analysis

Within the flexible environment of PSPICE, a lumped-element transistor model has been made for both the FET and the varactor, and transient analysis is carried out to look at both the output power and actual frequency range of the VCO. The varactor proposed for the VCO is a MA46H200-1056 hyperabrupt GaAs tuning varactor from M/A-com.
The varactor has the characteristics shown in table 6.

Table 6 Varactor parameters

parameter	value	conditions	unit
C_{tot}	1.2	V_R = 2V	pF
C_{tot}	0.6	V_R = 4V	pF
C_{tot}	0.2	V_R = 20V	pF
Q	> 3000	@ 50 MHz	pF
$V_{R,max}$	> 22	I_d = 10 µA	V
L_{par}	0.45	Package inductance	nH

All originally in ADS2003c designed microstrip lines are modelled by LCR low-pass filterstructures valid up to at least 20 GHz. In order to avoid unwanted resonances other than from the resonator itself, 0402 lumped element components are used for most biasing/decoupling parts of the VCO. The FET is self-biased by a source resistor, and is set at roughly 45 % Idss (40 mA) and a Vds of 12 V. With these values, a reasonable power dissipation of around 400 mW is achieved, which should be low enough to avoid escessive channel temperatures.
The basic schematic is shown in figure 4.

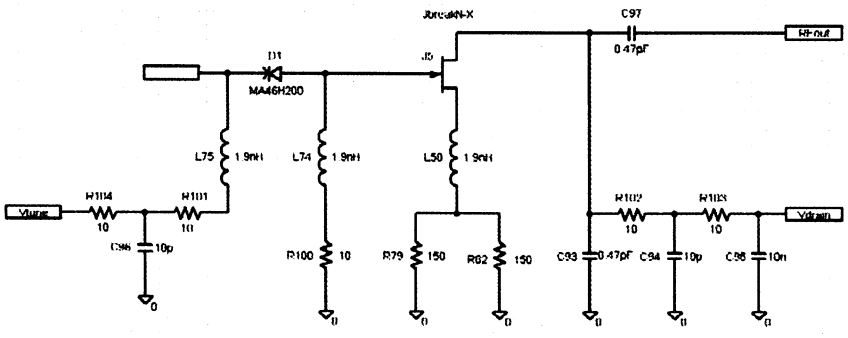


Figure 4 basic VCO schematic with only lumped elements (SMD parts)

The complete schematic includes all transmission lines and LCR models for all 0402 resistors, capacitors and inductors. The inductor used (1.9 nH) is from the CoilCraft 0402CS series.

The predicted PSPICE performance of the VCO is shown in figure 5.

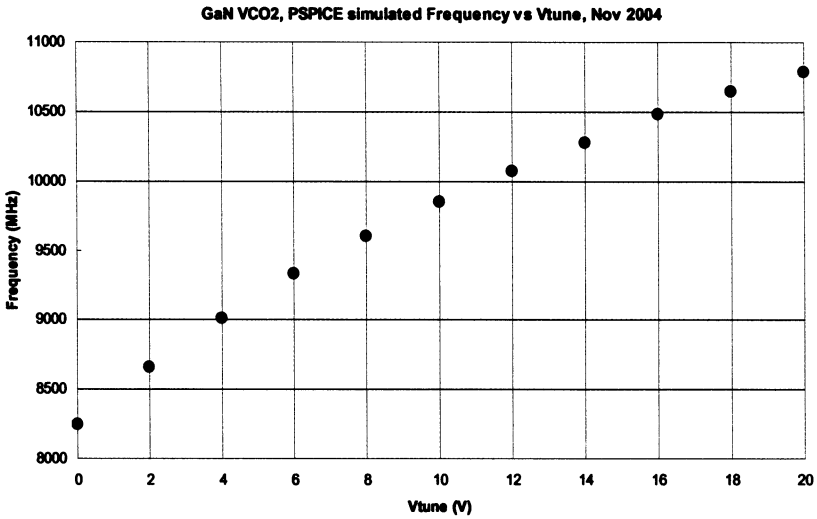


Figure 5 PSPICE - predicted tuning characteristic of the VCO

The simulated output powerlevel is around +18 dBm average into a 50 Ohms load and shows an output level that slightly increases with frequency.

3.4 VCO layout & manufacturing

The physical layout of the VCO has been designed using Protel PCB software. The final layout is shown in figure 6.

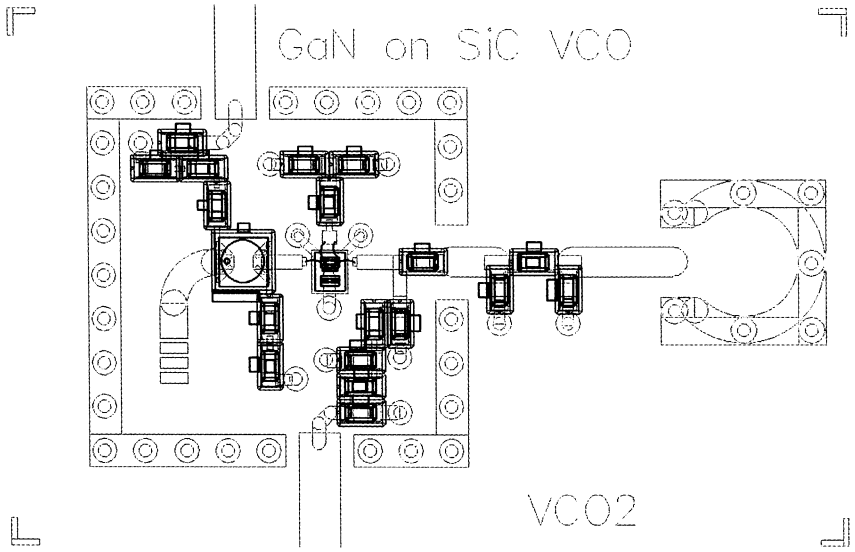


Figure 6 Layout of the VCO showing components and traces

The boardmaterial used is RO4003 from Rogers, 20 mil substrate thickness, doubled sided Copper with 0.5 mm plated via's and bondable (2 µm) Gold plating finish. All components are mounted using a manual surface-mount pick-and-place workstation and soldered in a standard infra-red reflow oven. 25 micron Gold bondwires are used to connect the gate, source and drain of the transistor to the tracks.

A 6 dB Pi-type attenuator is used to create some isolation to the output connector, avoiding excessive pulling effects caused by the connector and cable mismatch. The RF connector (on the right) used is a surface-mount SMP-type connector. Drain and tuning voltage are connected with wires soldered to the pads on the board.

In figure 7, a picture is shown of the completed VCO.

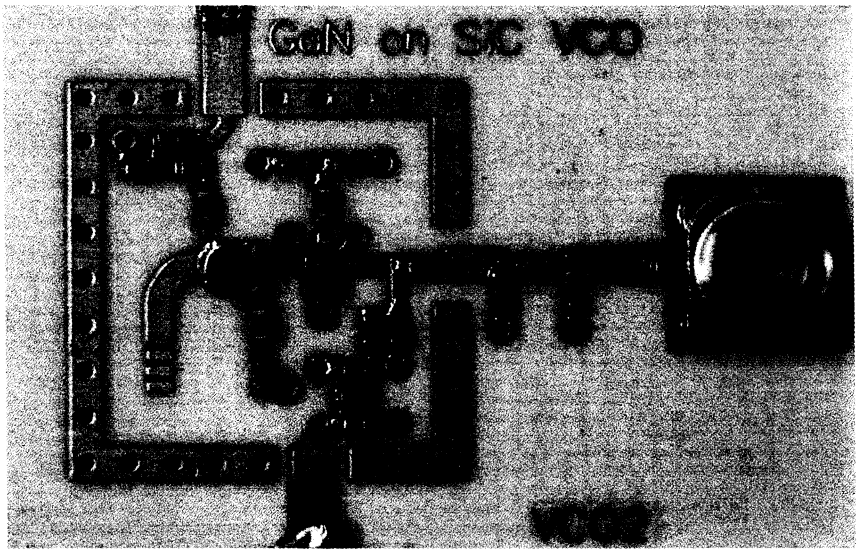


Figure 7 Photograph of the completed VCO

The board size is approximately 20 x 30 mm, while the actual VCO (including ground strip for attaching a lid) uses a total PCB area of less than 14 x 14 mm.

4. VCO measurement results

The first measurement of the finished VCO showed consistent oscillator behaviour. No problem of non-oscillation, spurious or other non-idealities were observed. For most measurements, the VCO was biased at +15 Volts on Vdrain. The nominal measured supply current is 37 mA.

The measured frequency and output power versus tuning voltage of the PCB is shown in figure 8.

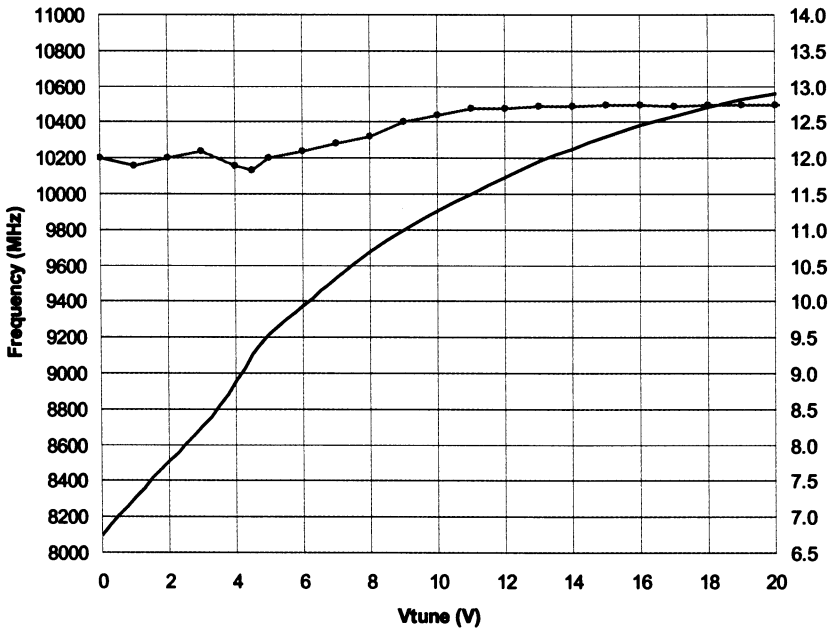


Figure 8 measured frequency and output power of the VCO versus Vtune

The output power of the VCO itself will be at least 6 dB higher because of the 6 dB attenuator on the test PCB. The VCO delivers a calculated average RF output power of 80 mW (+19 dBm).

The phasenoise has been measured at offset frequencies of 100 kHz and 1 MHz. The average measured values are -84 dBc/Hz @ 100 kHz and -114 dBc/Hz @ 1 MHz offset.

In figure 9, the phasenoise versus carrier frequency is plotted. Only small variations are visible. The small peak occurring around 8300 MHz is probably caused by the changes that occur in the oscillator when the increasing tuning voltage passes the DC voltage caused by detection of the RF signal at the varactor

diode, at approximately 1 Volt tuning voltage. For the same reason, the tuning voltage range from 0 to 1 Volts is often excluded from the specified tuning voltage range for a VCO with a tuning voltage range up to 20 Volts.

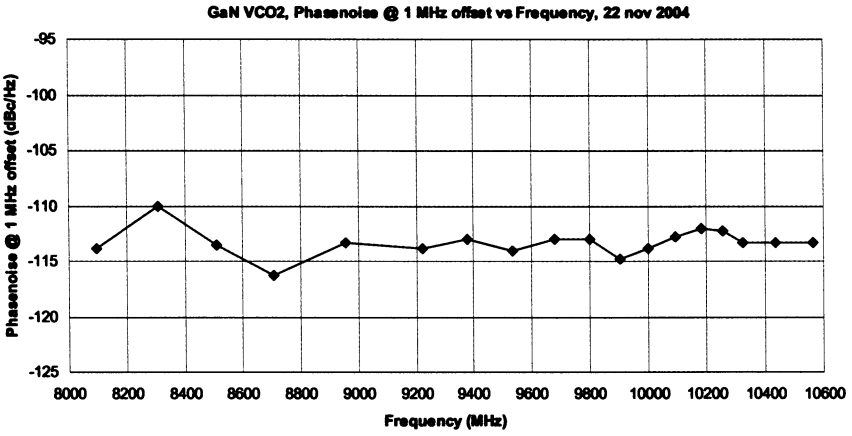


Figure 9 measured phase noise of the VCO versus carrier frequency

The phase-noise level as a function of drain-voltage at a tuning voltage of +7 Volts, is shown in figure 10.
At a bias voltage of +11 Volts and a frequency of 9.5 GHz, the phase-noise reaches a minimum value of approximately -117 dBc/Hz at 1 MHz offset frequency. With this phase-noise, the oscillator compares favourably with existing and published VCO designs using GaAs MESFETs.

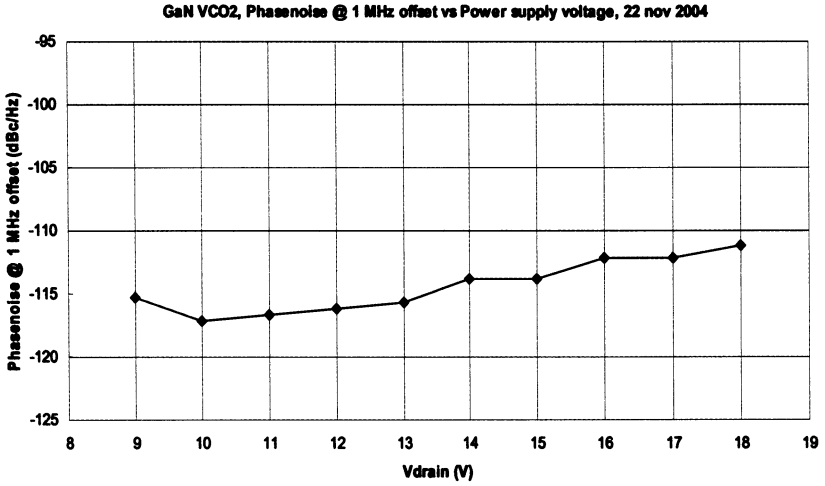


Figure 10 measured phase noise of the VCO versus Vdrain

The pushing of the VCO is measured and plotted in figure 11. The average pushing factor on Vdrain is approximately 20 MHz/V at a tuning voltage of 10 Volts.

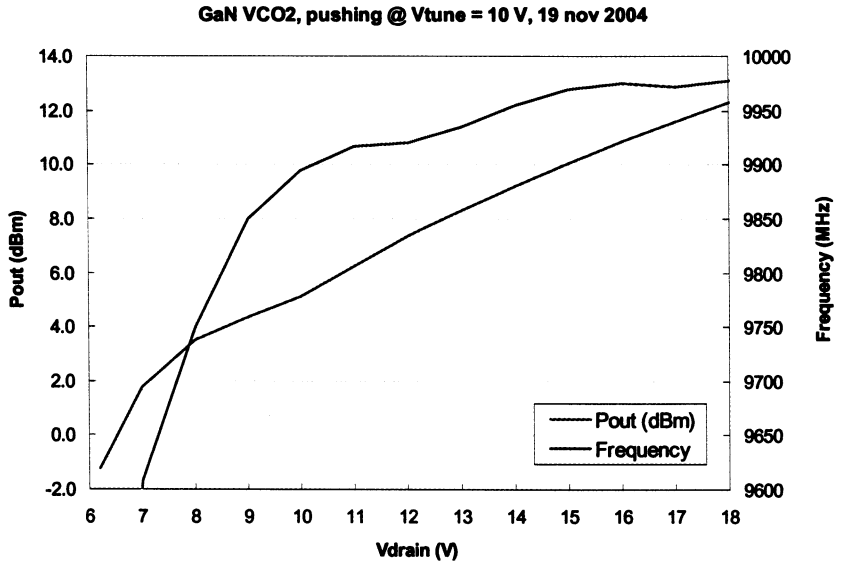


Figure 11 measured Vdrain frequency and power pushing of the VCO

A summary of all measured parameters of the VCO is presented in table 7.

Table 7 overview of measured VCO performance

specification	symbol	min	typ	max	units
Frequency Tuning Range			8.2 - 10.5		GHz
Tuning Voltage @ minimum frequency			0.5		V
Tuning Voltage @ maximum frequency			18.0		V
Tuning Voltage Range		0		22	V
Average Tuning Sensitivity			130		MHz/V
Tuning Sensitivity Ratio			4.5 : 1		
Tuning Linear Modulation Bandwidth		500			MHz
Tuning Port Input Capacitance			10		pF
Output Power Level			19		dBm
Second Harmonic Output Level			-15		dBc
Third and Higher Harmonics Output Level			-25		dBc
Power Supply Voltage			+15		V
Power Supply Current			37		mA
Frequency Pushing			20		MHz/V
Phase-Noise Level @ 100 kHz offset			-84		dBc/Hz
Phase-Noise Level @ 1 MHz offset			-114		dBc/Hz

5. Conclusion

An X-band VCO has been designed and realised using a GaN on SiC transistor sample. The VCO shows a good output power level (+19 dBm) and flatness (±0.5 dB) over a typical tuning range from 8.10 to 10.55 GHz. The bias voltage is +15 Volts and the VCO draws 37 mA of current. The tuning voltage can be varied from 0 to +20 Volts.

At a bias voltage of +12 Volts, the phase noise level at 1 MHz offset frequency is at its lowest value and has been measured to be -117 dBc/Hz at 1 MHz offset frequency, and -87 dBc/Hz at 100 kHz offset frequency.

In comparison with published results for hybrid VCOs at X-band, as shown in table 8, the circuit compares nicely with other VCOs produced using GaN transistors. The phase-noise level is roughly equivalent to the values that have been reported for GaN, SiGe and GaAs based VCOs.

Table 8 overview of measured hybrid X-band VCO performances

ref	Freq. (GHz)	tuning range (MHz)	output power (dBm)	phase-noise (dBc/Hz) 100kHz	circuit type	resonator	active device material / technology	phase-noise normal. 10 GHz	active device type
5	9.0	270	6	-109	hybrid	microstrip	Si	-108.1	bipolar
15 *	8.25	900	5	-102	hybrid	microstrip	Si BFP420	-100.3	bipolar
39	10	1000	15	-90	hybrid			-90.0	FET
4 *	9.2	0	9	-90	hybrid		GaAs	-89.3	uPG110
26	9.6	400		-89	hybrid		Si	-88.6	bipolar
26	9.6	400		-89	hybrid		SiGe	-88.6	HBT
24 *	8.2	60	3	-90	hybrid		InAlAs,InGaAs/InP	-88.3	HITFET
1	6.0	600	18-27	-92	hybrid		AlGaN/GaN	-87.6	HEMT
this work	***9.5***	***2400***	***19***	***-87***	***hybrid***	***microstrip***	***GaN on SiC***	***-86.6***	***HEMT***
70	7.5	1300	10	-63	hybrid		GaAs	-60.5	HJ-FET

6. References

3
Title : Low-phase noise AlGaN/GaN FET-based voltage controlled oscillators (VCOs).
Author(s) : Shealy, J.B.; Smart, J.A.; Shealy, J.R. (RF Nitro Commun. Inc., Charlotte, NC, USA)
Source : IEEE Microwave and Wireless Components Letters (June 2001) vol.11, no.6, p.244-5. 10 refs. Doc. No.: S1531-1309(01)05214-X

2
Title : X band BiCMOS SiGe 0.35 mu m voltage controlled oscillator in parallel and reflection topology and external phase noise improvement solution.
Author(s) : Wong, W.; Cibiel, G.; Tartarin, J.-G.; Tournier, E.; Plana, R.; Llopis, O. (LAAS, CNRS, Toulouse, France)
Source : 2003 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. Digest of Papers (Cat. No.03CH37410) Editor(s): Quach, T. Piscataway, NJ, USA: IEEE, 2003. p.281-4 of xlii+727 pp. 6 refs.

4
Title : A novel microwave oscillator using double-sided MIC.
Author(s) : Kawahata, K.I.; Miyayoshi, N.; Aikawa, M. (Dept. of Electr. & Electron. Eng., Saga Univ., Japan)
Source : 2002 IEEE MTT-S International Microwave Symposium Digest (Cat. No.02CH37278) Piscataway, NJ, USA: IEEE, 2002. p.699-702 vol.2 of 3 vol.(lxxxii+xxiii+xxv+2272) pp. 7 refs. Conference: Seattle, WA, USA, 2-7 June 2002 Price: CCCC 0-7803-7239-5/02/$10.00 ISBN: 0-7803-7239-5

5
Title : A low phase noise silicon 9 GHz VCO and an 18 GHz push-push oscillator.
Author(s) : Dussopt, L.; Guillois, D.; Rebeiz, G.M. (Radiat. Lab., Michigan Univ., Ann Arbor, MI, USA)
Source : 2002 IEEE MTT-S International Microwave Symposium Digest (Cat. No.02CH37278) Piscataway, NJ, USA: IEEE, 2002. p.695-8 vol.2 of 3 vol.(lxxxii+xxiii+xxv+2272) pp. 10 refs. Conference: Seattle, WA, USA, 2-7 June 2002 Price: CCCC 0-7803-7239-5/02/$10.00 ISBN: 0-7803-7239-5

7
Title : Low phase noise, fully integrated monolithic VCO in X band based on HBT technology.
Author(s) : Ouarch, Z. (UMS, Orsay, France); Arlot, F.; Borgarino, M.; Prigent, M.; Bary, L.; Camiade, M.
Source : 2001 IEEE MTT-S International Microwave Sympsoium Digest (Cat. No.01CH37157) Editor(s): Sigmon, B. Piscataway, NJ, USA: IEEE, 2001. p.1415-18 vol.3 of 3 vol.(lxiii+xxiv+xxiii+2262) pp. 5 refs. Conference: Phoenix, AZ, USA, 20-25 May 2001 Price: CCCC 0 7803 6538 0/2001/$10.00 ISBN: 0-7803-6538-0

8
Title : A very low phase noise SiGe VCO at X-band frequencies.
Author(s) : Dussopt, L.; Rebeiz, G.M. (Dept. of Electr. Eng. & Comput. Sci., Michigan Univ., Ann Arbor, MI, USA)
Source : 2001 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems. Digest of Papers (IEEE Cat. No.01EX496) Editor(s): Ponchak, G.E. Piscataway, NJ, USA: IEEE, 2001. p.219-21 of x+236 pp. 8 refs. Conference: Ann Arbor, MI, USA, 12-14 Sept 2001 Sponsor(s): IEEE Microwave Theroy and Techniques Soc.; NASA Glenn Res. Center; Army Res. Office Price: CCCC 0 7803 7129 1/2001/$10.00 ISBN: 0-7803-7129-1

14
Title : A low phase noise X-band MMIC GaAs MESFET VCO.
Author(s) : Lee, C.-H.; Han, S.; Matinpour, B.; Laskar, J. (Sch. of Electr. Eng. & Comput. Eng., Georgia Inst. of Technol., Atlanta, GA, USA)
Source : IEEE Microwave and Guided Wave Letters (Aug. 2000) vol.10, no.8, p.325-7. 11 refs. Doc. No.: S1051-8207(00)07045-8 Published by: IEEE Price: CCCC 1051-8207/2000/$10.00 CODEN: IMGLE3 ISSN: 1051-8207 SICI: 1051-8207(200008)10:8L.325:PNBM;1-R

15
Title : An X-band microstrip VCO with 900 MHz tuning range.
Author(s) : Ozdemir, M.K.; Huang, T.-H.D.; Arvas, E. (Syracuse Univ., NY, USA)
Source : ANTEM 2000. Symposium on Antenna Technology and Applied Electromagnetics. Conference Proceedings Winnipeg, Man., Canada: Univ. Manitoba, 2000. p.109-12 of 544 pp. 8 refs. Conference: Winnipeg, Man., Canada, 30 July-2 Aug 2000 Sponsor(s): Canadian Space Agency; Commun. Res. Centre; Defence Res. Establishment Ottawa; InfoMagnetics Technol. Corp ISBN: 0-9692563-7-X

16
Title : GaAs MESFET-based MMIC VCO with low phase noise performance.
Author(s) : Lee, C.-H.; Han, S.; Matinpour, B.; Laskar, J. (Pettit Microelectron. Res. Center, Georgia Inst. of Technol., Atlanta, GA, USA)
Source : GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuits Symposium. 22nd Annual Technical Digest 2000. (Cat. No.00CH37084) Piscataway, NJ, USA: IEEE, 2000. p.95-8 of ix+266 pp. 9 refs. Conference: Seattle, WA, USA, 5-8 Nov 2000 Sponsor(s): IEEE Electron Devices Soc.; IEEE Microwave Theory & Tech. Soc.; IEEE Solid-State Circuits Soc Price: CCCC 0 7803 5968 2/2000/$10.00 ISBN: 0-7803-5968-2

24
Title : X-band heterostructure interband tunneling FET (HITFET) VCOs.
Author(s) : Nair, V.; El-Zein, N.; Lewis, J.; Deshpande, M.; Kramer, G.; Kyler, M.; Maracas, G.; Goronkin, H. (Phoenix Corp. Res. Labs., Motorola Inc., Tempe, AZ, USA)
Source : GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. 20th Annual. Technical Digest 1998 (Cat. No.98CH36260) New York, NY, USA: IEEE, 1998. p.191-4 of xv+262 pp. 8 refs. Conference: Atlanta, GA, USA, 1-4 Nov 1998 Sponsor(s): IEEE Eletron Devices Soc.; IEEE Microwave Theory & Tech. Soc.; IEEE Solid-State Circuits Soc

Price: CCCC 0 7803 5049 9/98/$10.00 ISBN: 0-7803-5049-9

26
Title : Low cost voltage controlled oscillators for X-band mobile communication purposes realized with Si HBTs and SiGe HBTs.
Author(s) : Guttich, U. (Daimler-Benz AG, Ulm, Germany)
Source : 1998 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems. Digest of Papers (Cat. No.98EX271) Editor(s): Kayali, S. Piscataway, NJ, USA: IEEE, 1998. p.124-5 of viii+219 pp. 3 refs. Conference: Ann Arbor, MI, USA, 17-18 Sept 1998 Sponsor(s): IEEE Microwave Theory & Tech. Soc.; NASA Lewis Res. Center; Jet Propulsion Lab.; Army Res. Office Price: CCCC 0 7803 5288 2/98/$10.00 ISBN: 0-7803-5288-2

28
Title in English : APPLICATION OF THE OPEN LOOP METHOD FOR THE DESIGN OF DIELECTRIC RESONATOR OSCILLATOR AND VOLTAGE CONTROL OSCILLATOR IN X
BAND, WITH VERY LOW PHASE NOISE
Title in French : APPLICATION DE LA METHODE D'ANALYSE EN BOUCLE OUVERTE A LA CONCEPTION D'OSCILLATEURS A RESONATEUR DIELECTRIQUE ET
CONTROLE EN TENSION EN BANDE X, A TRES FAIBLE BRUIT DE PHASE
Author(s) : LAPORTE Eric; PRIGENT Michel (dir.)
Corporate Source : Universite de Limoges, Limoges, France (tutelle)
Source : (1997-09), 84 refs. 177 p. Dissertation Information: Universite de Limoges. Limoges. FRA, Th. doct., 97LIMO0015

33
Title in English : Voltage controlled X band low noise monolithic oscillator using HBT technology
Title in French : Oscillateur monolithique faible bruit en bande X controlle en tension en technologie TBH JNM 97 : 10emes journees nationales microondes : Saint Malo, 21-23 mai 1997
Author(s) : ROUX P.; LAPORTE C.; CACHIER G.; FLORIOT D.; DELAGE S.
Corporate Source : THOMSON CSF COMMUNICATIONS- 160 Bd de VALMY, 92704 Colombes, France; THOMSON CSF- LCR- Domaine de Corbeville, 91404 Orsay, France Institut national des sciences appliquees de Rennes, Rennes, France (patr.)

38
Title : A quenchable GaAs HBT X-band VCO for switched band synthesizer architectures.
Author(s) : Kobayashi, K.W.; Smith, D.M.; Kau, C.P.; Oki, A.K.; Sharma, A.K.; Allen, B.R.; Streit, D.C. (Electron. & Technol. Div., TRW Inc., Redondo Beach, CA, USA)
Source : IEEE 1996 Microwave and Millimeter-Wave Monolithic Circuits Symposium (Cat. No.96CH3594-9) Editor(s): Bahl, I.J. New York, NY, USA: IEEE, 1996. p.107-10 of xvi+232 pp. 20 refs. Conference: San Francisco, CA, USA, 16-18 June 1996 Sponsor(s): IEEE Microwave Theory & Tech. Soc.; IEEE Electron. Devices Soc Price: CCCC 0 7803 3360 8/96/$5.00 ISBN: 0-7803-3360-8

39
Title : Design of state of art low noise VCO using MMIC negative

resistance modules.
Author(s) : Laporte, E. (IRCOM-UA, CNRS, Brive, France); Maurin, P.; Nallatamby, J.C.; Reffet, D.; Prigent, M.; Obregon, J.
Source : GAAS 96. European Gallium Arsenide and Related III-V Compounds Applications Symposium and Associated CAD Workshop Paris, France: Conservatoire Natl. Arts et Metiers, 1996. p.1-4 of 396 pp. 7 refs. Conference: Paris, France, 5-7 June 1996 Sponsor(s): IEEE; MTT Soc.l ED Soc.; French Chapter of MTT-EDS; SEE

42
Title : MMIC oscillator design.
Author(s) : Dearn, A.W. (GEC-Marconi Mater. Technol. Ltd., Towcester, UK)
Source : IEE Colloquium on MMIC's (Monolithic Microwave Integrated Circuits) (Digest No.1995/221) London, UK: IEE, 1995. p.8/1-6 of 44 pp. 4 refs. Conference: London, UK, 28 Nov 1995 Sponsor(s): IEE

44
Title : A 1 watt X-band power combining array using coupled VCOs.
Author(s) : Liao, P.; York, R.A. (Dept. of Electr. Eng., California Univ., Santa Barbara, CA, USA)
Source : 1994 IEEE MTT-S International Microwave Symposium Digest (Cat. No.94CH3389-4) Editor(s): Kuno, H.J.; Wen, C.P. New York, NY, USA: IEEE, 1994. p.1235-8 vol.2 of 3 vol. (xxxiii+xlvii+1788+xxviii+xviii+xli) pp. 11 refs. Conference: San Diego, CA, USA, 23-27 May 1994 Price: CCCC CH3389-4/94/0000-1235$01.00
ISBN: 0-7803-1778-5

45
Title : Design of X-band VCO for marine radar product.
Author(s) : Harcun, I.; Davis, B.; McGrath, B. (Canadian Centre for Marine Commun., St.John's, Nfld., Canada)
Source : 1994 Canadian Conference on Electrical and Computer Engineering. Conference Proceedings (Cat. No.94TH8023) Editor(s): Baird, C.R.; El-Hawary, M.E. New York, NY, USA: IEEE, 1994. p.449-52 vol.2 of 2 vol. 834 pp. 3 refs. Conference: Halifax, NS, Canada, 25-28 Sept 1994 Sponsor(s): Canadian Soc. Electr. & Comput. Eng.; IEEE Canada ISBN: 0-7803-2416-1

47
Title : A varactor-tuned patch oscillator for active arrays.
Author(s) : Liao, P.; York, R.A. (Dept. of Electr. Eng., California Univ., Santa Barbara, CA, USA)
Source : IEEE Microwave and Guided Wave Letters (Oct. 1994) vol.4, no.10, p.335-7. 20 refs. Price: CCCC 1051-8207/94/$04.00 CODEN: IMGLE3
ISSN: 1051-8207

50
Title : Modelling and design of X-band MMIC varactor-tuned VCOs.
Author(s) : Karacaoglu, U.; Lucyszyn, S.; Robertson, I.D. (Dept. of Electron. & Electr. Eng., King's Coll., London, UK)
Source : IEE Colloquium on 'Modelling, Design and Application of MMIC's' (Digest No.1994/092) London, UK: IEE, 1994. p.13/1-5 of 90 pp. 3 refs. Conference: London, UK, 17 June 1994 Sponsor(s): IEE

57
Title : X-band HBT VCO with high-efficiency CB buffer amplifier.
Author(s) : Wang, N.-L.; Ho, W.-J. (Rockwell Int. Sci. Center, Thousand Oaks, CA, USA)
Source : IEEE Journal of Solid-State Circuits (Oct. 1992) vol.27, no.10, p.1439-43. 8 refs. Price: CCCC 0018-9200/92/$03.00 CODEN: IJSCBC ISSN: 0018-9200

60
Title : Piecewise linear modeling of solid-state varactor-tuned microwave oscillators.
Author(s) : Behagi, A. (Penn State Univ., Middletown, PA, USA); Turner, S.
Source : Proceedings of the 1992 IEEE Frequency Control Symposium (Cat. No.92CH3083-3) New York, NY, USA: IEEE, 1992. p.415-19 of xiii+871 pp. 5 refs. Conference: Hershey, PA, USA, 27-29 May 1992 Sponsor(s): IEEE Price: CCCC 0 7803 0476 4/92/$3.00 ISBN: 0-7803-0476-4

61
Title : X-band MMIC voltage-controlled oscillator using HEMTS.
Author(s) : Allamando, E.A. (Dept. Hyperfrequences et Semicond., Inst. d'Electron. et de Microelectronique du Nord, Villeneuve d'Ascq, France)
Source : Microwave and Optical Technology Letters (July 1992) vol.5, no.8, p.395-8. 4 refs. Price: CCCC 0895-2477/92/$4.00 CODEN: MOTLEO ISSN: 0895-2477

66
Title : A GaAs monolithic X band VCO.
Author(s) : Bollaert, S.; Vindevoghel, J.; Constant, E. (Centre Hyperfrequences et Semicond., Univ. des Sci. et Tech. de Lille 1, Villeneuve d'Ascq, France)
Source : Conference Proceedings. 21st European Microwave Conference, Microwave '91 Tunbridge Wells, UK: Microwave Exhibitions & Publishers, 1991. p.1487-91 of 2 vol. (xxv+v+1579) pp. 3 refs. Conference: Stuttgart, Germany, 9-12 Sept 1991 ISBN: 0-946821-37-2