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Development of GaN X-Band Power HFET´s

***Abstract*—This document summarises results from "Wide Bandgap Semiconductors for X-Band TT&C SSPA" project (ESTEC contract. no. 17489/03/NL/CH). It aimed at the development and fabrication of GaN HFET X-band RF power transistors with 3 different device sizes, followed by package assembly, characterisation, life tests and irradiation assessment.**

This project enabled partners Tesat-Spacecom (prime), Backnang, Germany, and Ferdinand-Braun-Institut für Höchstfrequenztechnik (FBH), Berlin, Germany, to improve GaN technology and to perform space application related tests for the first time.

***Index Terms*—GaN microwave field-effect transistor (FET) for SSPA, RF life test, DC life test, satellite applications, radiation effects, heavy ions**

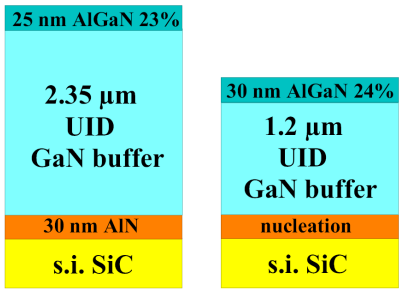
I. Introduction

Gallium-Nitride (GaN) is considered as an enabling key future technology for space applications. The wide bandgap, the high electron velocity and the high thermal conductivity make GaN an ideal material for operation at high power levels and at high frequencies. A high degree of radiation hardness is expected from GaN, due to its wide bandgap.

This document summarises the work undertaken on the ESA funded Wide bandgap semiconductors for X-band TT+C SSPA project and covers the period from October 2003 to May 2009. The aim of the project was to develop a family of discrete packaged GaN power transistors suitable for realising a 30W SSPA and undertake DC, RF and radiation lifetesting. This abstract document summarises the results obtained from the final processing run based on wafers supplied from two different epitaxy suppliers.

II. Epitaxial Design

Two wafers (one from each supplier) with different epitaxial design, GES04-05 and GES04-06, were selected for final device assembly based on on-wafer measurement results (DC characteristics and RF power sweep). Both wafers were grown on a SiC substrate. The epi structure of wafer GES04-05 consists of a 30 nm AlN layer, a 2.35 µm GaN buffer layer and a 25 nm $Al_{0.23}Ga_{0.77}N$ layer (see Fig. 1). The epi structure of wafer GES04-06 consists of a AlN nucleation layer, a 1.2 µm GaN buffer layer and a 30 nm $Al_{0.24}Ga_{0.76}N$ layer. Devices with gate widths of 4x125 µm (i.e. 4 gate fingers 125 µm wide), 12x125 µm and 2x12x125 µm (two 12x125 mm cells integrated on a single chip) and a gate length of 0.35 µm have been processed. Transistors with gate widths of 12x125 µm and 2x12x125 µm have on-chip internal gate pre-matching to 30 Ohm to ease use in a packaged environment. To improve electrical properties and to simplify the assembly process source via technology has also been introduced successfully during the course of the project. Prior to assembly, all devices were measured on-wafer at FBH. After device selection (note: an important selection criteria was to ensure good device pinch-off, therefore only devices with Id < 2.5 mA/mm in the pinch-off region were used) the wafers were diced and transistor chips were assembled by Tesat.



GES04-05 GES04-06

Fig. 1: Epitaxial structures.

III. Device Assembly and Characterisation

100 chips from wafer GES04-05 and 60 chips from wafer GES04-06 were assembled into A1510 RF packages from Kyocera, as shown in Fig. 2.

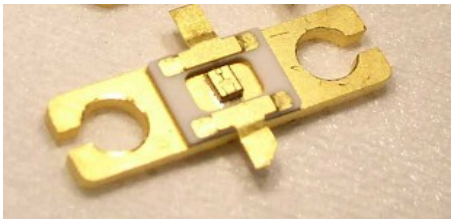


Fig. 2: 12x125 µm transistor chip assembled in A1510 package.

After AuSn solder attachment, X-ray inspection, wire bonding and pre-cap inspection (performed by ESA), devices were electrically characterised. Burn-in was performed on

This work was supported in part by the European Space Agency under ESTEC contract. no. 17489/03/NL/CH.

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selected devices for 168 hours at 20 V drain-source voltage and drain current of 0.25 A/mm. Neither failures nor significant degradation occurred. The estimated channel temperature for the device with gate width 4x125 µm during the burn-in was 250°C. The estimated channel temperature for the device with the gate width 12x125 µm and 2x12x125µm was 200 °C.

Fig. 3 shows the three different chip types and measured RF performance of packaged devices. The 4x125, 12x125 and 2x12x125µm chip size is 1.3 x 2 mm, 1.3 x 2 mm and 2.6 x 2 mm, respectively. P_{out} is the output power for 3 dB of compression.

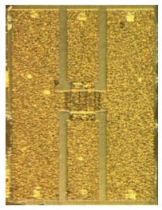
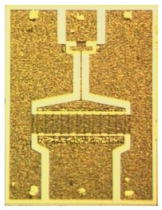
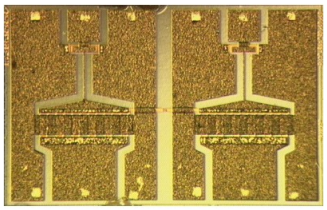
4 x 125 µm	12 x 125 µm	2 x 12 x 125 µm
		
P_{out} = 1.2 W	P_{out} = 5 W	P_{out} = 10 W
PAE = 47 %	PAE = 45 %	PAE = 35 %
G = 13 dB	G = 12.8 dB	G = 13.3 dB

Fig. 3: Chip photographs and RF performance of packaged devices.

IV. Thermal Properties

To extract lifetime parameters on the packaged devices the knowledge of the thermal resistance is a matter of substantial importance. The thermal properties of power cells attached to a CuMo base plate using AuSn solder had previously been simulated at FBH. The SiC substrate acts as a very effective heat spreader. Raman measurements show [1], that the thermal boundary resistance of the nucleation layer also has a significant influence on the temperature distribution in the device. Finite element simulation calibrated to Raman measurements and taking into account nucleation layer resulted in an average predicted thermal resistance of 15 K/W for devices with a gate width of 12x125 µm.

V. DC Life Test

The DC life test was performed on six 4x125 µm devices from wafer GES04-06. The life test duration was 1000 hours with DC and RF measurements at 0, 48, 168, 500 and 1000 hours. The drain-source voltage was 20 V and the drain current was 150 mA. The ambient oven temperature was 127.5 °C, which resulted in a junction temperature of T_j = 273°C. The maximum transconductance of the devices decreased insignificantly up to 4 % from the start value. RF output power decreased by a maximum of 1 dB. Compared to RF life test, DC life test degradation is higher probably due to higher channel temperature (273 °C compared to 200 °C).

VI. RF Life Test

A test board with SMA connectors was manufactured, comprising a packaged 12x125 µm device and a substrate providing matching to 50 Ohm as illustrated in Fig. 4. Optimum transistor impedances had been determined by load pull measurements at package level. The biasing is implemented on the matching substrate.

Four 12x125 µm devices from wafer GES04-05 had been selected for RF life test. The drain-source voltage was 26 V and the drain current was 250 mA. The devices were operated at 8 GHz at more than 2 dB of gain compression. The ambient oven temperature of 125 °C resulted in a junction temperature of T_j = 200°C (assuming a thermal resistance of 15K/W). DC and RF measurements have been performed at 0, 48, 168, 500, 700, 1000, 1050 and 2000 hours at room temperature.

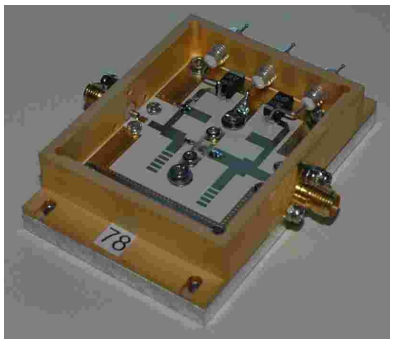


Fig. 4: Device under test prepared for the RF life test and heavy ion irradiation tests.

The RF output power drift is extracted from the intermediate measurements, as shown in Fig. 5. The observed 0.2 dB drift of the output power is far away from the 1 dB drift limit.

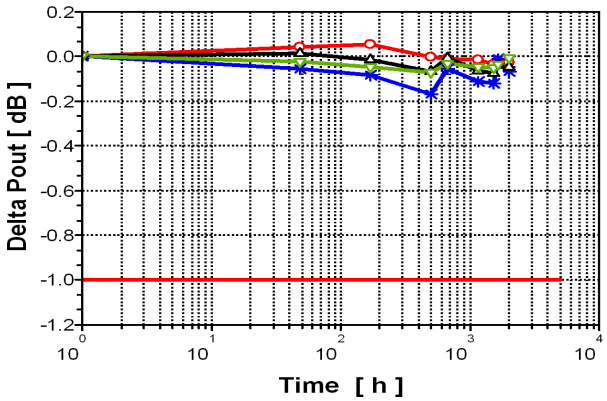


Fig. 5: RF output power drift extracted from the intermediate measurements during 2000 hours RF life test.

VII. Heavy Ion Irradiation Test

Besides displacement damage and ionisation irradiation effects, heavy ion impact on GaN transistors is of particular

interest for space application. To the authors' knowledge heavy ion irrradiation effects on RF GaN transistors both under DC and RF operation have been investigated for the first time during the course of this project. The heavy ion test was performed on four 12x125 µm devices mounted in the test board shown in Fig 4. The Heavy ion tests were performed at the Heavy Ion test Facility (HIF) of the Université Catholique de Louvain (UCL) in Louvain-la-Neuve, Belgium.

A schematic of the measurement set-up used to perform heavy ion irradiation tests is given in Fig. 6. The DUT assembled into the test board as shown in Fig. 4 is mounted on a water cooled plate in the vacuum chamber as marked with a dashed box (2) in Fig. 6. The ion beam enters the vacuum chamber with an adjustable angle. Sensors installed inside and outside of the vacuum chamber control and monitor the beam parameters (flux and homogeneity).

Unit 5 in Fig. 6 monitors the DUT temperature at the base plate. During all tests the temperature did not exceed 30 °C.

Feed through connections at the front side of the chamber allow the insertion and extraction of the generated and amplified RF signal into and out of the chamber, respectively. The RF input and output signal are monitored during the RF test campaign in unit (1) and (4). The RF output is additionally monitored by an oscilloscope. During static tests, single event transients occurring at the drain of the DUT can be monitored via this oscilloscope and events can be counted (unit (4)). The drain and gate voltages are supplied by a Source Measure Unit (SMU). During the test campaign, the drain and gate currents are monitored. An oscilloscope detects current peaks on bias lines and an event counter uses the oscilloscope trigger signal to count the number of peaks (events) during a test (unit(3)).

It was observed that transients caused by ion hits can be detected with much more confidence at the RF output than at the bias ports. Therefore, the following test results description concentrates on events measured at the RF output.

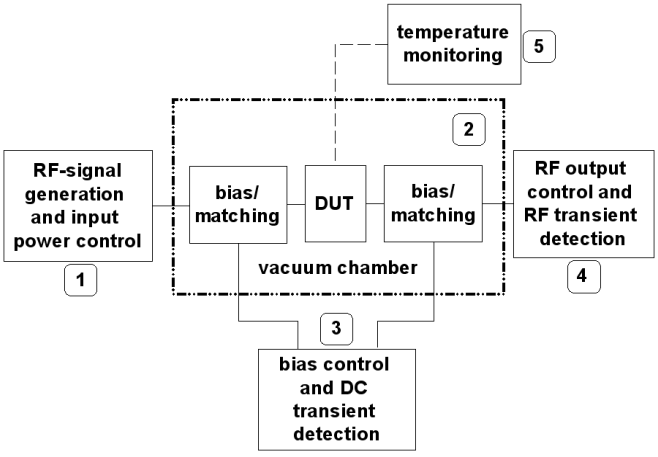


Fig. 6: Schematic of heavy ion test setup.

All devices were tested up to a linear energy transfer (LET) of 69 MeV/mg/cm² with a flux of about 5500 ions/(cm²s) up to a fluence of 10^6 ions/cm². The test sequence included static tests at several bias points and RF tests at different RF levels with and without QPSK modulation. All devices were tested up to a drain-source voltage of 30 V at pinch-off conditions within the static test campaign and up to 26 V drain-source voltage under RF operation with a QPSK modulated signal at 8 GHz within the RF test campaign. Detailed test conditions are shown in table I.

The number of events detected in static test campaigns of irradiated devices varies from 18 to 46 with a mean value of 32. With a fluence of 10^6 ions/cm² the device sensitive area (cross section) results in $3.2 \cdot 10^{-5}$ and $4.6 \cdot 10^{-5}$ cm² for the mean and maximum number of the detected events, respectively.

Neither single event burn-out nor significant degradation occurred during static and dynamic tests up to a LET of 69.1 MeV/mg/cm² and a fluence of 10^6 ions/cm². The static tests have been performed at a maximum drain voltage of 40 V in the pinch-off region. The maximum output power within the tests under RF excitation was 36.1 dBm at 8 GHz (CW and QPSK) at a drain-source voltage of 30 V.

TABLE I
HEAVY ION TEST CONDITIONS

SN	LET (GaN) [MeV /cm²/mg]	static drain-source voltage [V]	drain-source voltage at RF operation [V]	Pout,max [dBm]
76	4.76/52.93/69.1	15/20/ 25/30	26	35.4
162	52.93/69.1	15/30	26	35.5
165	52.93/69.1	15/30	30	36.2
156	69.1	15/30/ 40	26	35.2
78	n/a	15/30	26	34.8

SN78: reference device, identical measurement sequence, but not irradiated
SN132 control device, not shown here

VIII. CONCLUSION

GaN X-band power HFETs fabricated on a SiC substrate with 3 different RF output power levels/gate widths (1 W, 5 W, 10 W nominal RF output power, i.e. 4x125 µm, 12x125 µm and 2x12x125 µm gate width) have been developed and fabricated. 5 W and 10 W devices incorporated integrated pre-matching on-chip to simplify matching in a packaged environment. Source via-hole technology has also been successfully implemented and was found to simplify chip assembly and increase the maximum available gain by 0.3 to 0.5 dB for the largest power cells compared with using source bond wires.

More than 160 devices from 2 selected wafers of the final wafer batch have been assembled into RF packages with an

assembly yield of > 97%. Selected devices have shown the required RF performance and robustness to long-term DC and RF stress tests, as well as to heavy ion irradiation under RF operation.

6 devices with gate width 4x125 µm from wafer GES04-06 have been subjected to a 1000 h DC-life test at Uds = 20 V, Ids = 150 mA, i.e. 6 W/mm dissipated power and $T_{ambient}$ = 127.5 °C. This results in a calculated channel temperature of over 273 °C. For an assumed activation energy of 1 eV (worst-case) this corresponds to a MTTF of 180 years at 150 °C channel temperature and 60% confidence level.

2000 hours RF life test on four 12x125 µm devices at Uds = 26 V, 8 GHz, compression level > 2dB and estimated channel temperatures of 200 °C resulted in maximum output power drift of 0.2 dB. For an assumed activation energy of 1 eV this corresponds to a MTTF of 12.5 years at 150 °C channel temperature and at 60% confidence level.

Heavy ion irradiation test on GaN X-band transistors under RF excitation has been successfully performed. Neither single event burn-out nor significant degradation occurred up to a LET of 69.1 MeV/mg/cm² and a fluence of 10^6 ions/cm²

- in static tests up to 40 V drain voltage and
- in tests under RF excitation up to 36.1 dBm output power at 8 GHz (CW and QPSK) at a drain-source bias up to 30 V.

For the first time, the radiation hardness of GaN transistors under heavy ion irradiation and under RF excitation has been verified.

With ongoing projects such as GREAT^2 it is expected that the reliability and activation energy of GaN HEMTs will improve over time giving much more useful values for MTTF. The work undertaken on this activity will therefore form an important foundation for performing successful DC, RF and radiation tests on GaN devices in the future.

Acknowledgment

Special thanks to Andrew Barnes from ESA/ESTEC for the technical guidance of the project “Wide bandgap components for X-Band TT+C SSPA demonstrator”.

The authors would like to thank Fredrik Sturesson and his team from ESA/ESTEC to give the opportunity to perform a pre test at the Californium Assessment for Single Event Effects (CASE) facility at ESTEC in Noordwijk, The Netherlands.

References

[1] A. Sarua, “Thermal Boundary Resistance Between GaN and Substrate in AlGaN/GaN Electronic Devices,” *IEEE Trans. on Electron Devices*, vol. 54, pp. 3152-3158, Dec. 2007.