Microwave Frequency Capability of Wide Bandgap Semiconductors

M. van Heijningen[1] and R. Quay[2]

5 November 2008, version for public release

[1]TNO Defence, Security and Safety, Oude Waalsdorperweg 63, 2597 AK, The Hague, The Netherlands, email: Marc.vanHeijningen@tno.nl , tel +31 70 374 0422, fax +31 70 374 0653.

[2]Fraunhofer Institute of Applied Solid-State Physics, Tullastr. 72, D-79108 Freiburg, Germany. email: ruediger.quay@iaf.fraunhofer.de

***Abstract* — This paper presents the results of the ESA/ESTEC contract 17473/03/NL/CH “Microwave Frequency Capability of Wide Bandgap Semiconductors”, carried out by TNO Defence, Security and Safety and Fraunhofer Institute of Applied Solid-State Physics. The work performed from November 2003 to September 2008 has focused on the development of Gallium-Nitride (GaN) technology, devices and Monolithic Microwave Integrated Circuits (MMICs) for Ka-band (30 GHz) and V/W-band (50-75 GHz / 75-110 GHz). This project has been the first in Europe to target the development of GaN technology and MMICs for frequencies at and above 30 GHz. This paper will present the major results obtained in this project and recommendations for future developments.**

I. INTRODUCTION

The wide bandgap semiconductor Gallium-Nitride (GaN) offers many benefits with respect to the mainstream Gallium-Arsenide (GaAs) technology, such as: higher power density, higher operating temperature, radiation hardness, high efficiency and higher breakdown. These benefits make this technology very suitable for the design of Monolithic Microwave Integrated Circuits (MMICs) for space applications, especially for High Power Amplifiers (HPAs). The technology benefits can be translated into system advantages such as: smaller circuits due to the higher power density, or more power using the same device size, no need to lower the internal bus voltage for the amplifier bias which results in lower-weight and more efficient systems. It is also foreseen that in the near future power amplifiers currently using traveling wave tubes can be replaced by Solid-State Power Amplifiers (SSPA), using GaN MMICs. Apart from space applications, GaN technology also offers many benefits for other application areas such as automotive, communication and defence. The first commercial devices for W-CDMA and WiMAX communication systems are already available, from US and Japanese suppliers. Europe is currently catching up with this development: from the defence side there is mainly interest and development up to 20 GHz applications. But GaN also has the potential for much higher frequency operation, for power amplifiers, low-noise amplifiers, doublers, triplers, etc., at least up to 100 GHz and maybe even higher.

This paper will discuss the objectives of this project, the results obtained in two project phases and present conclusions and recommendations. In phase 1 of this work two processing runs have been completed, to evaluate the improvements to the technology. In phase 2 a third processing iteration has been performed, focusing specifically on efficiency improvements at Ka-band. In total 12 2-inch and 6 3-inch wafers have been processed.

II. PROJECT OBJECTIVES

Prior to the start of this program, GaN HPA’s were already demonstrated up to 20 GHz but the technology had not yet been demonstrated at 30 GHz and higher frequencies. Therefore this program was launched to develop the technology and demonstrate the performance of GaN MMICs and devices operating at frequencies >= 30 GHz. The original ESA specifications are given in the following two tables. For demonstration a Ka-band HPA has been chosen.

Table 1 : Ka-band HPA specifications

Relevant parameter	ESA Call for tender
Frequency Band	29.5 to 30 GHz
Min. Output power at 30 GHz	37 dBm
QPSK Modulation	Yes
Min. total gain of HPA	27dB
Min. gain per device	7 dB
Linearity (for 35% filtered QPSK modulated signal, at maximal output power)	Spectral re-growth of 20dBc maximum
Minimum PAE	40%

From the beginning on it has already been noted that the PAE value would be difficult to obtain at HPA level.

Table 2 : W-band HPA specifications

Relevant parameter	ESA Call for tender
Frequency	94 GHz
Minimum gain per device	5 dB

In addition to the W-band targets, demonstration of intermediate results at 60 GHz was proposed by the project team, with a projected gain of 7 dB per device.

III. Phase 1

A. Technology and MMIC design

The development work has started from an existing base-line technology. The performance of this technology is illustrated in Fig. 1, showing a power density of 4 W/mm at 30 GHz for a discrete transistor.

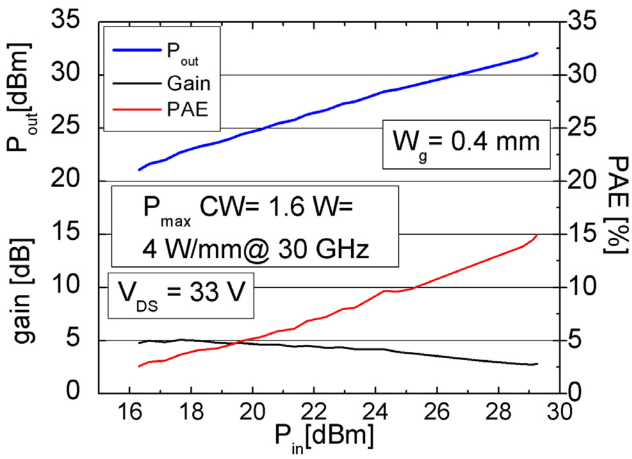

Fig. 1 : Measured performance of an 8x50 μm FET at 30 GHz.

The main focus of the technology improvement has been on increasing reproducibility, efficiency, high frequency performance and decreasing dispersion. The means to achieve these improvements are the epi-layer configuration (e.g. layer thicknesses, gate-to-channel separation, doping levels), gate module engineering (e.g. gate recess), contact spacing, gate pitch and gate length scaling (reduction from 150 nm to 100 nm). Information from amongst others published literature has been used to set-up a number of design experiments to evaluate different technology process options.

Since the power performance of the baseline technology was already good, more effort has been put in increasing the reproducibility, yield and dispersion. These figures have all improved during the course of the project, which results in a stable technology that is well understood and that can again be used as basis for further developments.

The specified power amplifier demonstrator has been divided into a 3-stage driver MMIC and 2-stage HPA MMIC design. Starting point for the design was the availability of large-signal transistor models and a full Agilent ADS coplanar waveguide passives design kit with auto layout, both created by IAF. In between the iterations significant effort has been devoted towards analyzing the measurement results and matching these results with new simulations in order to improve the next design. Much use of 2.5D and 3D EM simulators has been made, e.g. to simulate the passive networks at high frequencies. The resulting layouts for a driver and HPA version are shown in Fig. 2 and Fig. 3.

Devices from the first iteration processing exhibited problems with leakage (pinch-off) and dispersion. These problems were solved in the second processing iteration by optimizing the epitaxial layers.

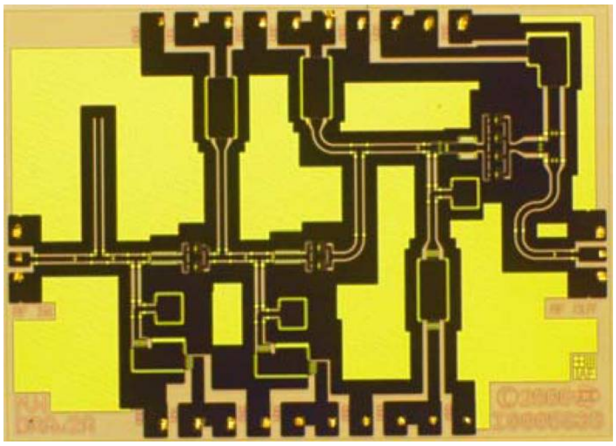

Fig. 2 : Photograph of the 3-stage driver amplifier MMIC with a size of 2.75 x 2.00 mm^2.

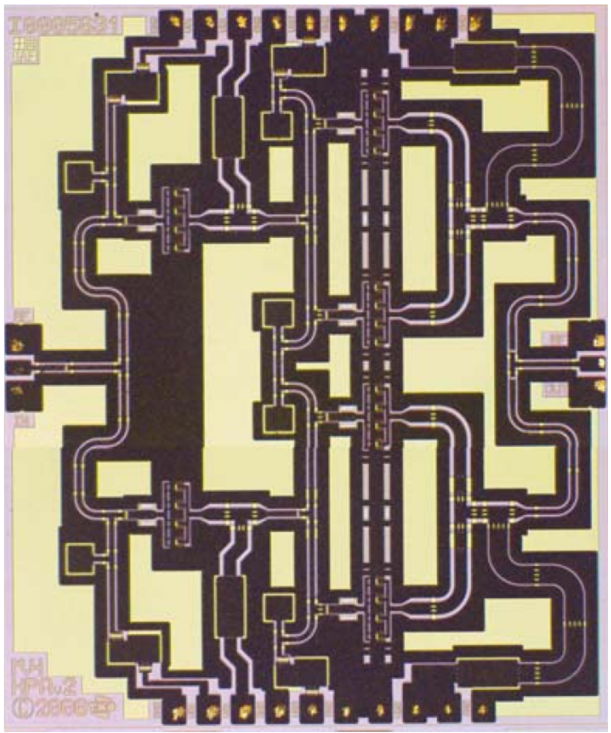

Fig. 3 : Photograph of the power amplifier MMIC with a size of 2.75 x 3.25 mm^2.

B. MMIC measurement results

The S-parameter measurement results of all functional driver and HPA MMICs from one of the processed wafers from iteration 2 are shown in Fig. 4 and Fig. 5. As can be seen, the uniformity over the wafer is already very good for this second processing iteration. The yield is also good, with on average 17 out of 21 functional samples. The maximum gain of the driver MMIC is around 15 dB and 10 dB for the HPA. Both designs have shifted down in frequency with respect to the original design. Fig. 6 shows the pulsed power measurements on the HPA from processing iteration 2. A maximum output power of 35 dBm has been measured at 30 V drain bias and 28 GHz, corresponding to a MMIC-level power density of 1.7 W/mm.

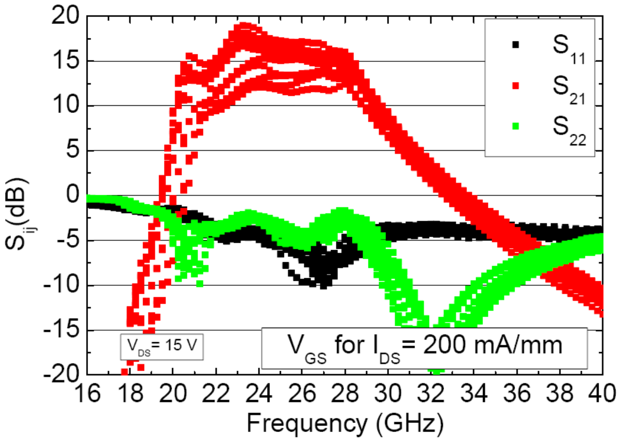

Fig. 4 : S-parameter measurements of driver amplifier DRA2b from processing iteration 2.

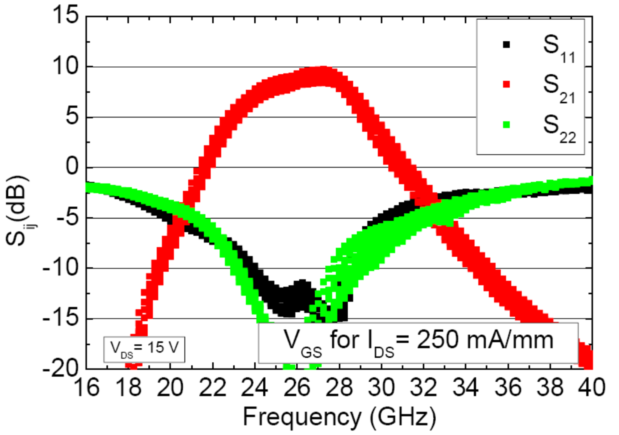

Fig. 5 : S-parameter measurements of HPAv2 from processing iteration 2.

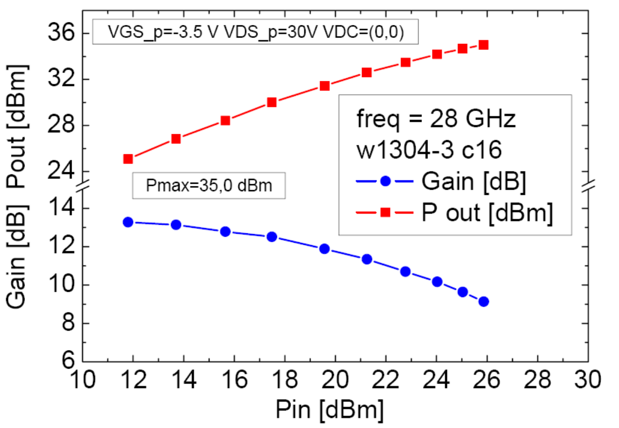

Fig. 6 : Pulsed power measurement of HPAv2 from processing iteration 2.

To verify the linearity target requirement of 20 dBc spectral re-growth, 2-tone measurements have been performed. During the design simulation it was already determined that an OIP3 of 38 dBm would be enough to obtain 24 dBc spectral re-growth. The measurement in Fig. 7 shows an OIP3 value of more than 42 dBm, which shows that the linearity requirements can be easily met.

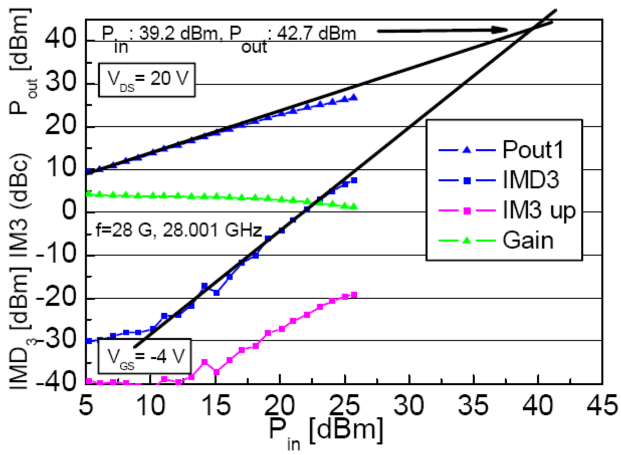

Fig. 7 : IM3 measurement of HPAv2 from processing iteration 2.

C. SSPA module measurement results

Both driver and power amplifier MMIC's from the second processing iteration have been mounted in modules. Because of the high power dissipation, the mounting and module design requires special attention. Fig. 8 shows a closed and open module. The selected demonstrator for this project is an HPA which consists of the cascaded driver and power amplifier module.

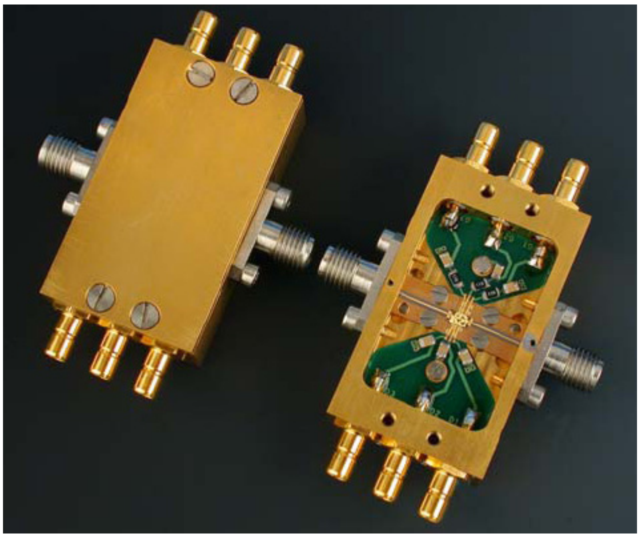

Fig. 8 : Line-up of a driver and power amplifier module.

Fig. 9 shows the small signal measurement for two of these cascaded driver and power amplifier chains. A total gain of 22 dB around 25 GHz has been measured. Large signal measurements could not be performed due to the high dissipation and thermal loading and PCB biasing that prevents the use of pulsed measurements. Mounting of the MMICs from the third iteration, with increased efficiency, will automatically lead to better performance, but this was not included in the second phase of the project.

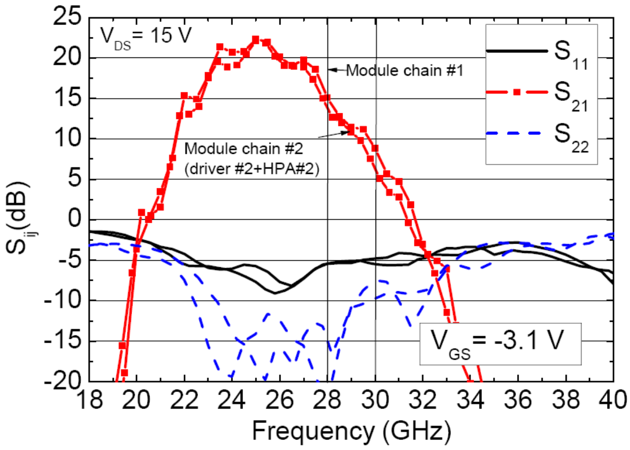

Fig. 9 : Measurement of two driver-amplifier module chains.

C. V/W-band device measurement results

To obtain higher operating frequency, gate length scaling from 150 nm to 100 nm was also investigated. The following three figures show the major results obtained with the 100 nm devices: ft/fmax of 55/124 GHz, 6.5 dB gain at V-band (59 GHz) and 3.2 dB at W-band (101 GHz) for pre-matched devices (MMICs). The performance improvement obtained by the gate-length scaling is however not yet optimal and further performance improvements are possible.

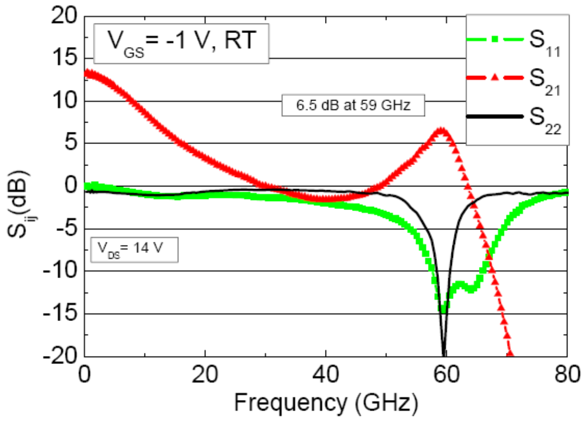

Fig. 10 : Measured performance of a pre-matched cascode 4x45 µm FET optimized for V-band.

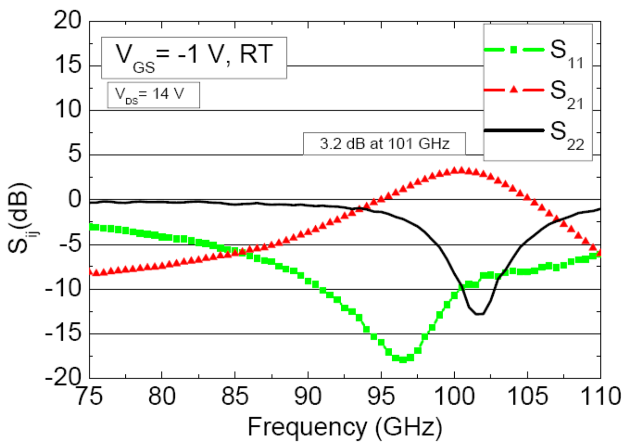

Fig. 11 : Measured performance of a pre-matched cascode 4x45 µm FET optimized for W-band.

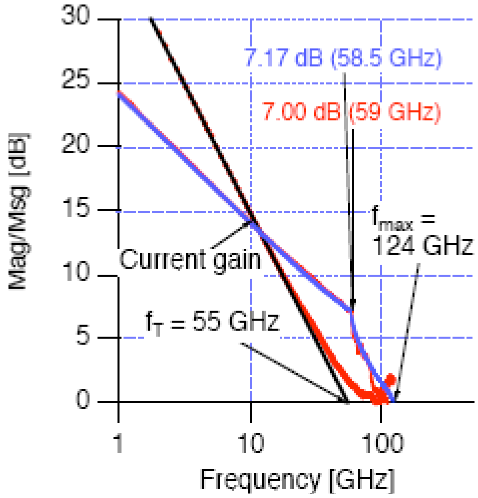

Fig. 12: Measured and modeled performance of a 4x45 µm FET with 100 nm gate length at Vds=7V.

IV. Phase 2

In phase 2 of the project an extra processing iteration has been performed, using the latest technology improvements developed in parallel to this project. In this iteration, 3 technology variants have been processed, with and without AlN interlayer and with varying nitride thickness. The major goal here was to improve the efficiency while maintaining the already good yield and uniformity. New targets for the final process iteration were defined, based on the results obtained in phase 1. These new targets were aimed at demonstrating discrete transistor operation at 30 GHz with at least 7 dB gain, 4 W/mm power density and 30% power added efficiency, at a supply voltage of at least 20 V.

The following three figures show the obtained CW and pulsed efficiency versus power density results from iteration 3, measured on a 150 nm gate length 4x50 µm device. At Ka-band PAE values of 47% have been achieved in pulsed operation (10% duty cycle) and power densities up to 4.6 W/mm. The typical associated linear gain is 10 dB at 27 GHz in efficient bias operation.

The device measurement results from phase 2 show that the new targets can be met in pulsed operation for a 4x50um device

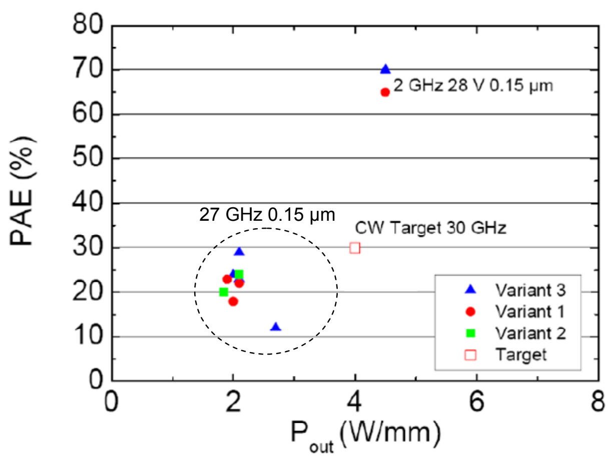

Fig. 13: Measured CW PAE versus power density for processing iteration 3 at 2 GHz and 27 GHz.

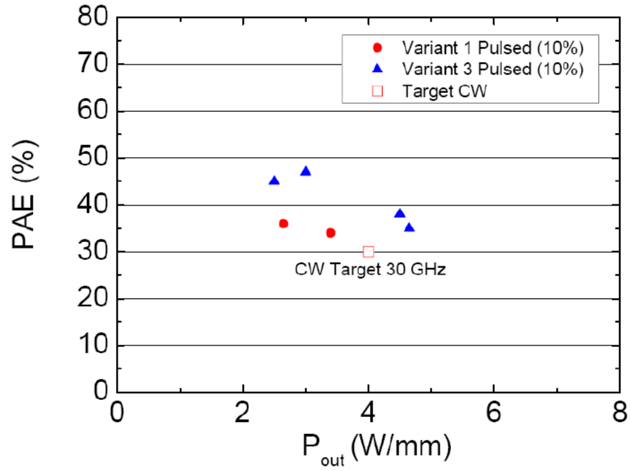

Fig. 14: Measured pulsed PAE versus power density for processing iteration 3 at 27 GHz.

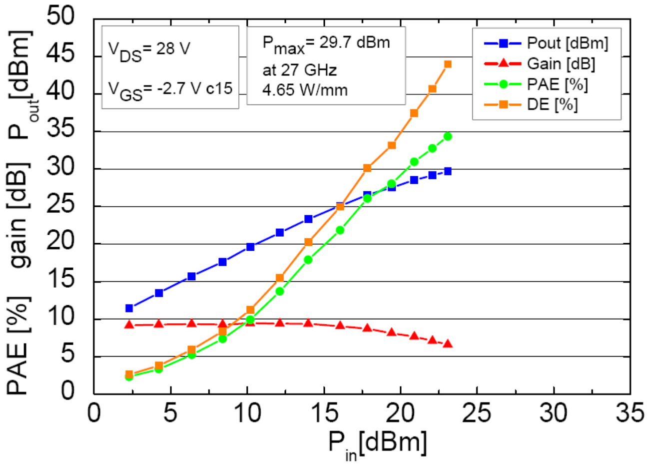

Fig. 15: Pulsed power measurements on a 4x50um pre-matched device at 27 GHz (technology variant 3).

The measured small-signal CW S-parameters for a driver MMIC and HPA MMIC version from the third iteration processing (technology variant 1) are shown in Fig. 16 and Fig. 17. As can be seen there is very little spread on the samples over the wafer and the number of functional samples (i.e. the yield) is also very high. This applies to all three technology variants. The gain of the driver is around 18 dB and 10 dB for the HPA. For both designs the center frequency has shifted downwards from the target value of 30 GHz.

In pulsed operation the driver MMIC delivers an output power of 28.6 dBm at 27 GHz and Vds=25V. Fig. 18 shows the measured CW large signal performance of the power amplifier MMIC (iteration 3, variant 1). The maximum measured output power is 33.2 dBm at 26 GHz. Technology variant 3 shows a slightly lower output power (32.7 dBm) but higher efficiency (10 %) Pulsed power measurements on iteration 2 HPA samples have shown a maximum output power of 35 dBm, as shown in Fig. 6.

Because of the introduction of the new process technology variants, these MMIC designs are not optimized for these new technologies. This results in relatively poor PAE performance at MMIC level, however the discrete transistor targets are achieved in pulsed operation, showing good promise for the technology with optimized layouts, improved matching and better thermal management.

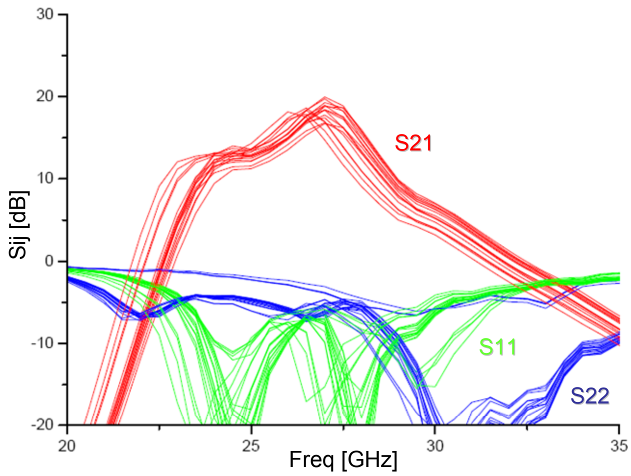

Fig. 16 : Measured S-parameters of all driver MMICs from the third iteration (variant 1, Vds=15V, Ids=200mA/mm).

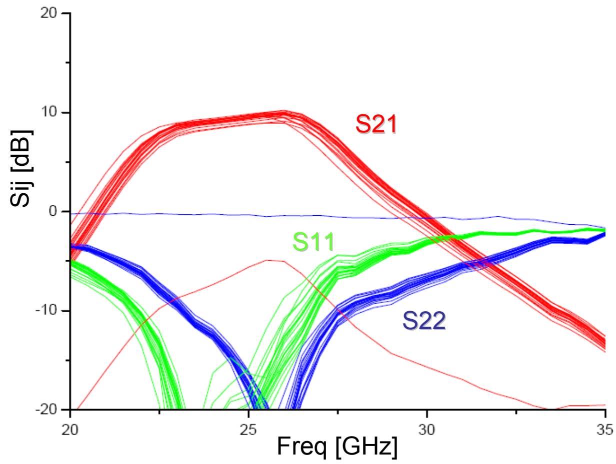

Fig. 17 : Measured S-parameters of all HPAs from the third iteration (variant 1, Vds=15V, Ids=200mA/mm).

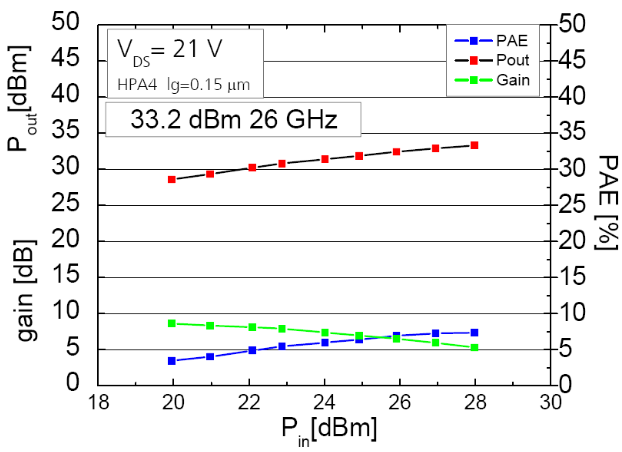

Fig. 18 : Measured CW large signal performance of the third iteration HPA.

V. Conclusions and Outlook

Great potential is expected for millimeter-wave applications of GaN technology. GaN MMICs at millimeter-wave frequencies will enable compact and high-power SSPA's as well as robust receiver components. This project has been the first activity in Europe and a major driver for the development of GaN devices and MMICs beyond 20 GHz and up to 100 GHz.

Using the FhG-IAF AlGaN/GaN on SiC technology, a large number of coplanar Ka-band amplifier MMICs and V/W-band devices have been designed, fabricated, tested and analyzed. The results show very promising performance. The 2-stage power amplifier MMIC shows an output power of 35 dBm at 28 GHz under pulsed conditions. For pre-matched devices (MMICs) 6.5 dB gain at V-band (59 GHz) and 3.2 dB at W-band (101 GHz) have been demonstrated. Results from the third iteration have shown increased efficiency performance, with pulsed PAE values of 47% at 27 GHz.

The major achievement is that these results have been obtained for stable and uniform processes with high yield. The realized technology improvements include:

- optimized epitaxial structure (Si doping, Al content, AlN interlayer)
- nitride-assisted gate
- optimized source-drain spacing
- processing on 3 inch SiC wafers
- 150nm and 100nm gate length
- Si doped GaN cap

Further process improvements are still possible and are also worked on, especially focusing on increasing the efficient operation of the devices and specific improvements for operation at 100 GHz. The introduction of microstrip technology and libraries for GaN designs up to 110 GHz will further increase the power amplifier MMIC performance, by providing decreased matching losses and increased design freedom.

The MMIC results have been made possible thanks to the continues process improvements and modelling activities of FhG-IAF and the power amplifier design experience of TNO and the good cooperation between these two project partners. With increasing design experience in GaN processes, optimum devices, improved modelling accuracy based on stable and reproducible processes even higher performance figures are near.

In conclusion, it has been shown that GaN technology, especially for power amplifier designs, can offer lower cost and higher performance systems for applications over a wide frequency range.

V. Acknowledgement

The project partners TNO and Fraunhofer IAF acknowledge the support of the ESA/ESTEC Technology Research Program (TRP) for funding this work and especially the professional guidance of Andrew Barnes.

The results of this project have also been made possible thanks to the continues technology improvement at Fraunhofer IAF and the processing of many wafers in parallel to this project.

V. Publications and Presentations

- F. van Vliet, "Microwave Capability of Wide Bandgap Semiconductors: Ka-band MMIC design", ESA round table on Wide Band Gap Technologies for microwave application, 17-18 Mar 2005.
- F. van Vliet, M. van Heijningen, F. van Raay and R. Quay, "GaN microwaves for space", Proc. of the European Microwave Association, Vol. 1, Sep. 2005, pp.212-218.
- M. van Heijningen, F.E. van Vliet, R. Quay, F. van Raay, R. Kiefer, S. Müller, D. Krausse, M. Seelmann-Eggebert, M. Mikulla and M. Schlechtweg, "Ka-Band AlGaN/GaN HEMT High Power and Driver Amplifier MMICs", Proc. GAAS 2005, Paris, pp. 237-240.
- R. Quay, "AlGaN/GaN HEMT MMICs and Hybrid PAs for High Bandwidth and High Frequency High Power Applications", contribution to short course at CSICS 2005.
- M. van Heijningen, "Ka-Band AlGaN/GaN HEMT Power Amplifier MMIC Design and Realisation", MOD – Space Agency Workshop on GaN Technologies, 14-15 Nov 2005.
- R. Quay, "Advanced High-Speed GaN HFET Devices for Broadband Communication MMICs", contribution to workshop at IMS 2006.
- M. van Heijningen, F.E. van Vliet, R. Quay, F. van Raay and M. Seelmann-Eggebert, "Design and Analysis of a 34 dBm Ka-Band GaN High Power Amplifier MMIC", Proc. EuMIC 2006, Manchester, pp. 75-78.
- M. Schlechtweg, "Microwave/mm-wave AlGaN/GaN HEMT circuits and applications", contribution to short course at CSICS 2006.
- W. Pletschen, R. Kiefer, B. Raynor, S. Müller, F. Benkhelifa, R. Quay, M. Mikulla, M. Schlechtweg, G. Weimann, "Recessed gate processing for GaN/AlGaN-HEMTs", MRS Fall Meeting 2006, Boston, USA.
- R. Quay, "GaN/AlGaN HEMT Amplifiers and Modules from 0.9 GHz-100 GHz for Space Applications", DGA/ESA Workshop, 3rd Space Agency – MOD Round Table Workshop on GaN Microwave Component Technologies, 2-3 Apr 2007.
- R. Quay, F. van Raay, A. Tessmann, R. Kiefer, M. Dammann, M. Mikulla, M. Schlechtweg, G. Weimann, "GaN HEMT: Trends in civil and military circuit applications", 31st Workshop on Compound Semiconductor Devices and Integrated Circuits WOCSDICE, May 20-23, 2007.