Linearity Assessment of GaN Technology

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***Abstract* - This document summarises results from the "Linearity assessment of GaN Technology" project (ESTEC contract. no. 20456/07/NL/IA). This project aimed at finding intrinsic transistor fabrication techniques and using device/circuit level implementation techniques to improve the linearity and power added efficiency of GaN HEMT for space application. Results of literature review, physical device simulation study, on-wafer linearity assessment, assessment of packaged transistor power bars and high power amplifier realisation will be described.**

***Index Terms* - GaN high electron mobility transistor (HEMT), FET, MMIC process, linearity, HPA, satellite applications**

I. INTRODUCTION

The wide bandgap semiconductor Gallium-Nitride (GaN) is considered as key future technology for space applications, especially microwave solid state power amplifiers (SSPAs). The wide bandgap, the high electron velocity and the high thermal conductivity of the SiC substrate make GaN-on-SiC an ideal material for operation at high power levels and at high frequencies. A high degree of radiation hardness is expected from GaN, due to its wide bandgap.

Linearity and efficiency are key parameters of solid-state amplifiers. Although solid-state amplifiers with GaN high electron mobility transistors (HEMT) already show a good linearity performance e.g. when compared to traveling waveguide tubes, output power needs to be backed-off from the point of highest efficiency when highest linearity performance is required.

This study aims at investigating linearity performance and improving both linearity and efficiency behaviour of GaN power HEMTs.

This abstract summarises the results obtained in the frame of the ESA TRP project "Linearity assessment of GaN Technology".

II. SOLUTION STRATEGY FOR HIGH EFFICIENCY AND LINEARITY

In order to obtain a solution strategy for high efficiency and linearity a literature overview and a simulation study has been performed prior to epitaxial design, device layout and fabrication.

Literature Overview

Key issue for linearity is to achieve a high trans-conductance value combined with an abrupt transition from the sub-threshold region into a broad flat region of the transconductance versus the gate-source voltage.

High transconductance values can be achieved by increasing the donor concentration in the 2 DEG or increasing the velocity in the channel, and finally to increase the channel depth or introduce multiple channels.

Also important in this context is the role of access resistance, especially the source resistance, due to its feedback character on device performance. Decrease of the source access resistance can be achieved either by dedicated layer structure or by local implantation.

To summarise the solution strategy for linearization of the device from literature can be subdivided into geometrical, layout / cross-sectional and epitaxial aspects:

1) Layout / Cross-sectional aspects

a) Implementation of as short gate length as possible. This will provide higher gain and smaller capacitances, especially smaller gate-drain capacitance.

b) Implementation of a field-plate, which will provide an equalized electric field distribution in the region between the gate and the drain leading to higher breakdown voltages. Decision of field-plate connection has to be made upon the achievable cut-off frequency and gain, because a source-connected field plate will increase the (linear) gate-drain and gate-source capacitances.

c) Implementation of a T-gate for very short gate-length to decrease gate resistance.

d) Floating field-plate or a field-plate connected to the source are both possible.

2) Geometrical aspects

a) Implementation of an effective heat-sink. This is important to avoid temperature gradients, which lead to degraded linear operation.

b) Gate recess is NOT necessary

c) Fabrication of recessed ohmic contact in order to decrease the access source and drain resistances

d) Gate finger width should be around 150 – 300 µm depending on frequency (higher width at lower frequencies).

e) Implementation of a tailored air-bridge design for the source contact of a multi-finger device in order to achieve a favourable feedback source inductance

3) Epitaxial aspects

a) Implementation of a suitable surface cap layer structure. The cap layer structure will improve the trapping and dispersion effects.

b) Highly doped channel (delta doping > 5×10^{12} cm^{-2}).

c) Implementation of double-channel or complementary channel structures.

Linearity assessment using physical/electrical simulation tools

Based on the literature overview a set of parameters was suggested for verification by device simulation. Silvaco Atlas 2D device simulator was used. Calibration on test 0.4 µm gate length AlGaN/GaN HEMT demonstrated to give sufficiently accurate information about the third order derivatives of the transfer characteristics.

The parameter set included variations of epitaxial structures, reduced gate length, source-gate distance variation and transistors with source-connected field plates. A sensitivity analysis has been carried out into the effect on the intrinsic device linearity of GaN/AlGaN HEMTs. The primary observations are:

- Reducing the barrier thickness does not seem to significantly change linearity, but increases the electric field
- Composite channels and AlN exclusion layers result in an improvement in linearity
- Reducing the Al percentage in the barrier layer reduces electric fields (and hence increases operating voltage) but at the expense of degraded linearity
- A GaN cap allows a reduction in electric fields and hence an improvement in operating voltage without a significant penalty in linearity.
- Recess gates seem to have little benefit for linearity
- Reducing the source-gate spacing results in a significant degradation in linearity
- Reducing the gate length degrades linearity
- Field plates and gamma gates can reduce electric fields without significantly changing the linearity.

III. EPITAXIAL DESIGN AND DEVICE FABRICATION

For device processing embedded gate technology with 0.25 µm gate length was used.

Baseline epitaxial structures from FBH (E4) and QinetiQ (E1), as well as structures with AlN spacer (E2 and E9), Iron (Fe) (E1, E2, E6, E7, E8) and Carbon(C) (E5) doping in the buffer, and AlGaN back-barrier (E3) were used for the fabrication of transistors. All epitaxial structures had a GaN cap as it was proven to be beneficial by previous experience. Both versions n-type (E3-6, E9) and UID (E1-2, E7-8) GaN caps have been included in this study.

Three main processes were completed for the purpose of the project. These are Process 1, Process 2 and trial for the fabrication of X-band MMICs. In addition, two process trials were necessary for technology optimization purposes. The Process 1 was used primarily for the initial on-wafer assessment of linearity, while Process 2 produced power bars for power amplifier demonstrator design.

For the verification of device layout impact on linearity, transistors with reduced 0.5 µm gate-source distance as compared to standard 1.5 µm gate-source distance were fabricated.

5×8×125 µm width and 5×8×250 µm width power bars were fabricated as a result of final Process 2 in the project. The other variations of the power bars in Process 2 included source connected field plates and reduced 4.0 µm (as opposed to standard 5.5 µm) source-drain distance.

IV. RESULTS AND DISCUSSION

Results of on-wafer linearity assessment based on comparison of the transconductance profiles and analysis of the two-tone intermodulation distortion (IMD), assessment of packaged transistor power bars and high power amplifier realisation will be discussed here.

Epitaxial layers and linearity

AlGaN back-barrier

The transconductance profiles for the wafers with AlGaN back-barrier (E3) were found to be the most linear in Process 1 and Process 2. Figure 1 shows cross-comparison of transfer and transconductance characteristics from Process 2, where wafer GLI04-04 has structure E3.

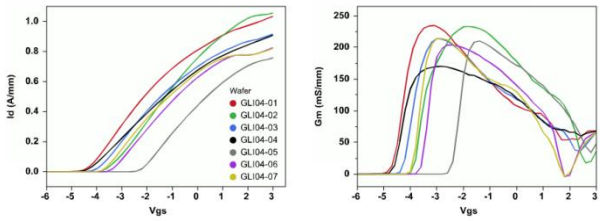

Figure 1: Transfer characteristics and derived transconductance profiles for transistors from Process 2

As can be seen from Figure 1 the linearization of transconductance is due to a relatively low value of maximum transconductance and one of the most negative pinch-off voltages in the ensemble of compared transistors. A cross-comparison of epitaxial structures in terms of the C/I3 ratio confirmed improved linearity for transistors fabricated on E3 structure.

It is suggested that the better confinement of electrons at the AlGaN/GaN interface due to the AlGaN back-barrier keeps the pinch-off voltage in the range of -4.5 V and in combination with the increased source resistance leads to a reduction of maximum transconductance and to the broader dynamic range of the transfer characteristic [1] [2].

It is important to note that the linearity of transistors on layers E3 was improved not in expense of microwave performance. Power bars 5×8×125 and 5×8×250 fabricated on wafer with structure E3 were found to have the best load-pull results at -25 dB 3rd order intermodulation distortion ratio (IMD3) and were used for L-band amplifier demonstrator.

GaN cap layer

Simulation showed that a reduced barrier thickness does not significantly changes linearity, but leads to unfavourable electric field distribution. On the other hand reduced Al percentage in the barrier layer reduces electric fields (and hence increases operating voltage) but at the expense of degraded linearity. A GaN cap allows a reduction in electric fields and hence an improvement in operating voltage without a significant penalty in linearity.

In the frame of this project all epitaxial structures had GaN cap. Investigation conducted at FBH out of this project revealed importance of the gate-to-channel separation in general and n-type GaN cap in particular for device linearity [3]. Based on these findings all structures grown at FBH included the 5 nm n-GaN cap. The standard cap at QinetiQ is unintentional doped (UID) GaN of ~ 3 nm.

In Process 2 structure E6 from QinetiQ with n-GaN cap was compared with QinetiQ structure E7, where the cap was kept undoped with the remaining layers being similar. The results indicate somewhat better linearity at 15 dBm and 25 dBm output power levels for transistors on E7 as follows from comparison of the C/I3 ratio. However, this improvement

is accompanied by reduced microwave performance. Thus, the maximum output power drops by ~ 0.6 W/mm and power-added efficiency by ~ 4 % for structure E7 as compared to E6. In addition, the structure E7 had one of the strongest memory effects with a difference between low and high tones up to 4 dBc at 15 dBm power level.

Since the total gate-channel separation and buffer structure was unchanged for the discussed structures, it is the cap, which produces the observed changes in overall performance of the transistors. Based on literature overview and simulation results the effect of n-GaN cap can be explained by modification of the electric field distribution between gate and drain.

Buffer Doping

The buffer doping was not discussed as a possible variation for linearity assessment, but was known to be absolutely necessary for preventing buffer punch-through effect and premature breakdown of transistors. The off-state breakdown voltages measured in Process 1 clearly indicated the necessity of the buffer doping for reliable operation of power transistors at VDS = 28 V.

Two types of doping were used in Process 2. These are carbon (proposed by FBH) and iron (as a standard doping at QinetiQ). It was proven that buffer doping results in suppression of punch-through effect, but degrades maximum output power up to 2 W/mm and lowers power-added efficiency up to 9 %. From linearity prospect doping is not desirable. Figure 2 clearly shows reduced C/I3 ratios for the transistors on epitaxial layers with doped buffer and high breakdown voltages, independently on the type of doping. The reduced linearity is accompanied by stronger memory effects.

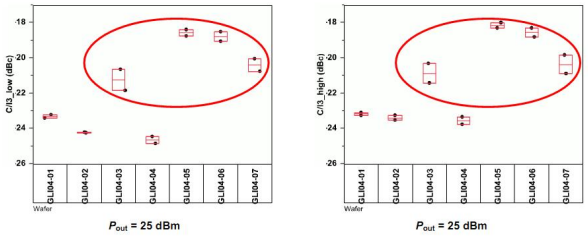

Figure 2: Third order intermodulation distortion ratio (C/I3) at 25 dBm output power level. Both low (left) and high (right) tones are shown (Wafers with doped buffer and high breakdown voltage outlined).

The aforementioned problems in linearity and microwave performance are most probably associated with incorporation of traps as a result of doping. Pulsed I-V measurements indicate increase of dispersion for doped versions of the buffer. The optimization of doped buffer structure by introducing channel UID GaN layer of a thickness adjusted to the doping concentration is required. But this optimization was not the primary goal of the current project.

AlN spacer layer

The AlN spacer layer was recommended for improvement of linearity based on the outcomes of the simulation study. Two wafers with AlN spacer (E2) were included in Process 1. The experimental results were not conclusive as the wafers with epitaxial structures E2 exhibited extremely high ohmic contact resistances (as a result of rapid thermal anneal with standard parameters) and a significant non-uniformity of measured parameters (as attributed to non-uniform thickness of the AlN spacer).

Device layout and linearity

Gate length variation

The effect of short gates seems to be controversial. Literature overview lists short gates as the most important and promising step for improved linearity, while in simulation the gate length reduction (from 0.4 µm) degrades linearity.

Because of decision to use 0.25 µm gate length technology for primary processes in the project a direct comparison of transistors with different gate lengths was not possible.

An indirect confirmation of improved linearity due to shorter gates can be discussed based on the results of a standard 0.5 µm optical gate technology used for the fabrication of X-band MMICs. The cross-comparison of transconductance profiles for structures E3, E6 and E9 in Figure 3 shows the most non-linear profile for the 0.25 µm gate length structures E3 and E6. It should be noted that the comparison given on Figure 3 is indirect, since epitaxial structure E9 used for the fabrication of MMICs differs from those used in Process 2.

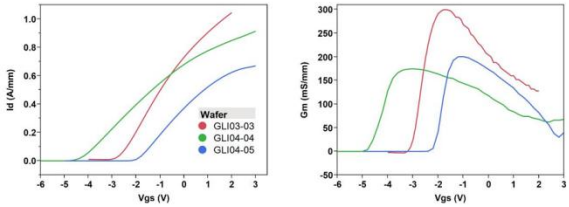

Figure 3: Comparison of transfer characteristics and derived transconductance profiles for transistors on wafers GLI03-03 (E9), GLI04-04 (E3) and GLI04-05 (E6)

The degradation of linearity for longer gates is consistent with the discussion for AlGaN back-barrier above, as the dynamic range reduces due to positive shift in pinch-off voltage caused by combination of epitaxial structure and the long gates. In the particular example this shift is in combination with an increased drain current resulting in a higher value for the maximum transconductance.

Source-gate distance variation

Simulation shows that source-gate spacing reduction should result in a significant degradation in linearity. In contrast from literature the opposite is reported.

From variations of source-gate distance (L_{SG}) from 0.25 µm up to 2 µm in Process 1 it was found that a minimum distance of 0.5 µm is required for acceptable yield.

Figure 4 shows transfer characteristics and trans-conductance profiles for 2×125_A2 transistors with L_{SG} = 0.5 µm and 2.0 µm. Source resistances (RS) are 0.48 Ωmm (L_{SG} = 0.5 µm) and 1.15 Ωmm (L_{SG} = 2.0 µm), respectively. The increased source resistance results in linearization of the transconductance profile in expense of reduced drain current and maximum transconductance.

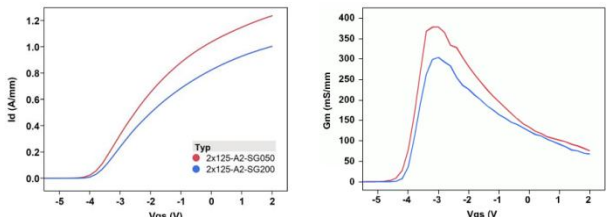

Figure 4: Comparison of typical transfer characteristics and transconductance profiles measured for transistors 2×125_A2 with gate-source distance 0.5 µm and 2.0 µm on wafer GLI02-11 (E4) from Process 1. Drain bias is 15 V.

It is expected from simulation that the device with increased L_{SG} has improved linearity due to increase in access source resistance. However, the improved (more flat) transconductance profile by the increased source resistance does not necessary lead to a better C/I3 ratio. This contradiction can be explained by looking at “intrinsic” linearity of transcon-

ductance profile for the two transistors. Figure 5 shows “intrinsic” transfer characteristic and corresponding trans-conductance curve calculated by subtracting voltage drop across the source resistance.

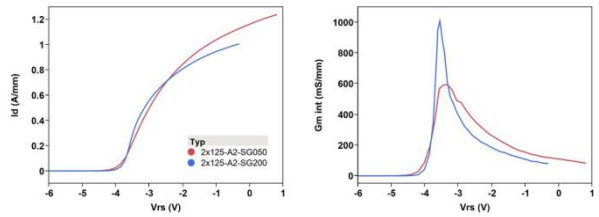

Figure 5: Calculated “intrinsic” transfer characteristics and transconductance profiles obtained from characteristics shown on Figure 4

A significant difference in “intrinsic” linearity of transistors can be seen on Figure 5. The “intrinsic” linearity for the transistor with 2.0 µm gate-source distance is significantly worse. The difference may come from the fact that the total source-drain distance is also changed in this experiment.

We suggest that the results observed in IMD measurements are influenced by both “intrinsic” linearity of the device and linearization due to increased source access resistance.

Source connected field plates

Based on literature and simulations field-plates can be beneficial for linearity and/or improvement in operating voltage.

Figure 6 reveals no significant difference in terms of transconductance profile linearity for two types of transistors 2×125_A2 (standard) and 2×125_A2_SFP15 with source-connected field plate (SFP). The latter has 1.5 µm extension of field plate from the gate head edge to the drain side. Despite absence of effect on linearity source-connected filed plates are known from literature and previous experience to be beneficial for power added efficiency and breakdown voltage due to reduced electric field on the drain side of the gate. It should be noted that the effect of field plates becomes more pronounced with the increase of operation VDS voltage. At operation voltage 28V the effect was expected to be limited.

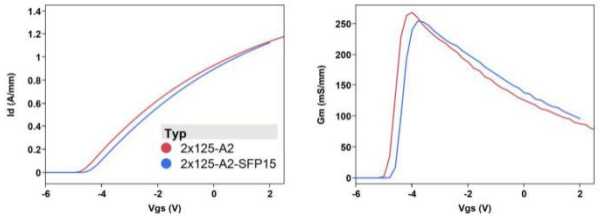

Figure 6: Comparison of typical transfer characteristics and transconductance profiles measured for transistors 2×125_A2 (standard) and 2×125_A2_SFP15 (with source-connected field plate) on structure E3 from Process 1. Drain bias is 15 V.

Linearity of power transistors

Load-pull measurements at 2 GHz demonstrated superior performance for power bars from epitaxial structures E3 with AlGaN back-barrier (FBH) and E6 with iron buffer doping (QinetiQ). The best values for standard 5×8×250 µm power bars are 33.1 W of output power and 66 % of efficiency achieved on epitaxial structure E3. In general, transistors with reduced 0.5 µm gate-source distance delivered up to 4 W higher output power with comparable or a few percent higher efficiency.

IMD measurements confirmed superior performance of power bars from epitaxial structures E3 and E6 at the -25 dB IMD3 limit. Again the best results in terms of output power and efficiency were obtained for power bars with AlGaN back-barrier. Two-tone data at -25 dB IMD3 ratio did not confirm advantages of the reduced gate-source distance for overall performance of power bars, which can be in part due to test in the same fixture. The standard 5×8×250 µm power bars from E3 (AlGaN back-barrier) structure were used for the realization of L-band amplifier demonstrator. Power bars have been packaged and characterised in a transistor test bench before designing L-band high power amplifiers.

L-band high power amplifier

The design objective is to get the highest two-tone output power where IMD3 is lower than -25dB. This is achieved by going as low in IQ as possible while keeping IMD3 better than -25dB. With respect to IMD3 performance, transistor amplifier data in Figure 7 demonstrate that there is a small advantage of decreasing the quiescent current (IQ) below the nominal setting of 0.5 A. Reducing IQ is also seen to increase two-tone efficiency slightly at a minor gain penalty.

Figure 8 shows a realised L-band amplifier. Fundamental, 2nd, and 3rd harmonic impedance components are controlled and tuned across 6% bandwidth.

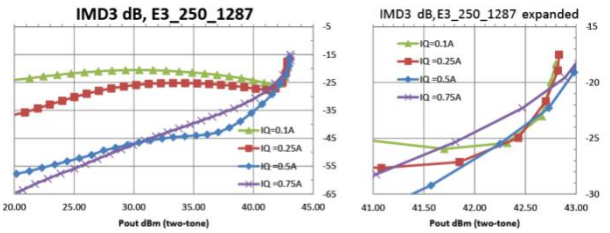

Figure 8: IMD3 transistor test bench measurements across the resultant output powers (with IQ as parameter).

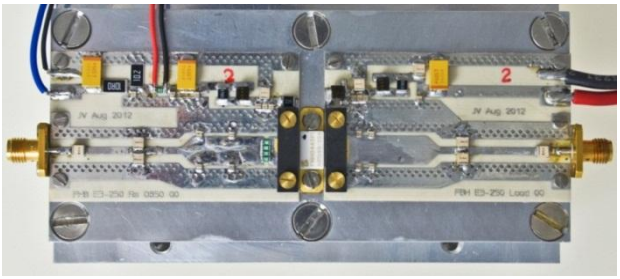

Figure 8: Photograph of realised L-band high power amplifier

The measured performance of the amplifier is given in the table below. Output power, efficiency and gain is indicated for IMD3 = -25 dB.

Parameter L-Band Amplifier	E3_250_1287 VDD=28V, I_Q=0.2A
Frequency Range	1.49 GHz to 1.59 GHz 0.2dB Single Tone Bandwidth
Output Power, Two-tone @ IMD3=25 dB	42.4 dBm~17.5W @ 1.56 GHz
PAE % , Two-tone @ IMD3=25 dB	49.4 % @ 1.56 GHz
Bandwidth	100MHz 0.2dB BW -10MHz displacement
Gain, Two-tone @ IMD3=25 dB	12.4 dB @ 1.56 GHz
IMD3, Δf=0.1 to 10 MHz	≥ 25 dB
Output Power, Single Tone	44.2 dBm~26.2W @ 1.56 GHz
PAE %, Single Tone	54.7% @ 1.56 GHz
Gain and compression, Single Tone	11.7 dB, -1.4 dB comp. @ 1.56 GHz

The ratio of two-tone to single-tone is close to a factor that applies if the limiting nonlinearity for both intermodulation and gain compression lies between a hard limiter and a 3rd order polynomial.

With these close to theoretical limits result there is no other way of improving the two-tone output power than to raise the power capabilities of the applied transistors. If the efficiency shall be improved, some sort of linearization techniques must be employed, for instance by a gain expansion, gain compression sequence.

V. CONCLUSION

From initial on-wafer linearity assessment for two-finger 2×125-µm-wide transistors and assessment of linearity for power transistors it was found that cross-comparison of transconductance profiles in most cases correlates with the outcomes of IMD results. Therefore this simple approach is a powerful linearity evaluation technique.

With respect to the epitaxial choice the results indicate improved linearity for epitaxial structure E3 with inclusion of AlGaN back-barrier. The linearization of transconductance in this case is due to a relatively low value of maximum transconductance and one of the most negative pinch-off voltages in the ensemble of compared epitaxial structures. A cross-comparison of epitaxial structures in terms of the C/I3 ratio confirmed improved linearity for transistors fabricated on E3 structure.

This improved linearity was achieved not in expense of microwave performance. A little effect of n-GaN cap was observed on linearity of transistors, but it was beneficial for the overall microwave performance. From linearity prospect doping in the buffer of HFET structures and AlN spacer were found to be undesirable. Despite observed degradation of maximum output power up to 2 W/mm and lower power-added efficiency for transistors on structures with doped buffer, doping is used by many leading groups and companies for prevention of leakages in the buffer.

It was demonstrated that linearity degrades for longer gates, as the dynamic range reduces due to positive shift in pinch-off voltage caused by combination of epitaxial structure and the long gates.

Source-connected field plates were found to have limited impact on linearity, while they are beneficial for microwave performance of power bars, especially at high operation voltages.

The linearization due to increased access source resistance was found not to be straightforward. Transistors with source-gate distances 0.5 µm and 2.0 µm, respectively, were fabricated and compared in terms of linearity. It was shown that the linearization of transconductance profile due to increased source resistance not necessarily leads to a better C/I3 ratio.

This fact can be explained by the "intrinsic" linearity of the transconductance profile, which was found to be strongly non-linear for transistors with increased source-gate distance and source resistance, respectively. It was suggested that the results observed in IMD measurements are influenced by both "intrinsic" linearity of the device and linearization due to increased source access resistance. It remains unclear which mechanism is dominant at particular bias conditions.

Overall the linearity study performed in the project indicated importance of the access source resistance, which can be influenced by transistors design and by epitaxial structure.

Variations in epitaxial structures open more degrees of freedom for the linearity improvement, since improved linearity can be achieved by keeping output power (maximum drain current), efficiency and "intrinsic" linearity without degradation.

IMD measurements confirmed superior performance of power bars from epitaxial structures E3 and E6 at the 25 dB IMD3 limit. The best results in terms of output power and efficiency were obtained for power bars with AlGaN back-barrier. Two-tone data at -25 dB IMD3 ratio did not confirm advantages of the reduced gate-source distance for overall performance of power bars.

The realised L-band high power amplifier from structure E3 reaches a two-tone output power of 17.5 W at IMD3 = -25 dB close to theoretical limits for hard limiting nonlinearity given the single-tone output power capability of the transistor.

VI. ACKNOWLEDGMENT

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