CMOS Process-Compatible High-Power Low-Leakage AlGaN/GaN MISHEMT on Silicon

Marleen Van Hove, Sanae Boulay, Steve Stoffels, Xuanwu Kang, Dirk Wellekens, Karen Geens, Michel Mélotte, and Stefaan Decoutere

***Abstract*—This document summarises results from the "Development of highly manufacturable processes for wide band gap technology compatible with a Si production environment" project (ESA/ESTEC Contract no. 20713/NL/07/SF). The aim of the project was to develop processing techniques for manufacture of GaN-on-Si power devices compatible with processing in a Si CMOS production environment.**

We report on a novel Au-free CMOS compatible process for fabrication of AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors (MISHEMTs). The process starts from a 150 mm GaN-on-Si substrate and uses an embedded Si_3N_4/Al_2O_3 bilayer gate dielectric, encapsulated by a high temperature low pressure chemical vapor deposited (LPCVD) nitride layer. Power devices with 20 mm gatewidth reach a maximum output current of 8 A, a breakdown voltage of 750 V, and a specific on-resistance $R_{on,sp}$ of 2.9 mΩ·cm^2. The off-state drain leakage at 600 V is 7 µA. Robust gate dielectrics with large gate bias swing are also demonstrated. The overall performance achieved represents current state of art.

***Index Terms*—GaN-on-Si, Au-free, gate dielectric, metal-insulator-semiconductor high electron mobility transistor (MISHEMT), high voltage, high temperature, heavy ion radiation.**

I. Introduction

GAN-BASED high-electron mobility transistors (HEMTs) have attracted a significant amount of interest for high-frequency and also high-power applications because of their potential for fast and low-loss switching, high breakdown voltage, high operating temperature and radiation robustness. The majority of devices have been realized to-date using the AlGaN/GaN material system using Schottky gate metallisation schemes (e.g. Ni/Au) and processed on costly SiC substrates. However, for mass market penetration of the power conversion market it is important to reduce the cost of GaN power devices by adopting processing techniques that make use of the economies of scale of the Si industry [9]. Therefore a key aim of the work performed on the ESA funded "Development of highly manufacturable processes for wide band gap technology compatible with a Si production environment" project was to fabricate GaN power devices on large diameter Si substrates and to develop CMOS compatible processing techniques.

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II. Device Design

AlGaN/GaN HEMTs with Schottky gates and without surface passivation suffer from high gate leakage, current dispersion and a variety of reliability issues. A unique feature of the work performed in this project was the use of a high-quality surface passivation, achieved by in-situ metal-organic vapor deposited (MOCVD) Si_3N_4 [1], [2], [3].

For power applications it is important to reduce the gate leakage current to minimize the power consumption in the off-state. To achieve noise immunity and gate-bias margin, a large gate-bias range of operation is also desired. For this reason low gate leakage is essential for both reverse and forward gate biasing conditions. To suppress the gate leakage a metal-insulator-semiconductor (MIS)HEMT is often fabricated by inserting a gate dielectric between the Schottky gate and the AlGaN barrier.

An ideal gate dielectric would have a high dielectric constant to improve device transconductance. It would also have a large conduction band offset to suppress gate leakage.

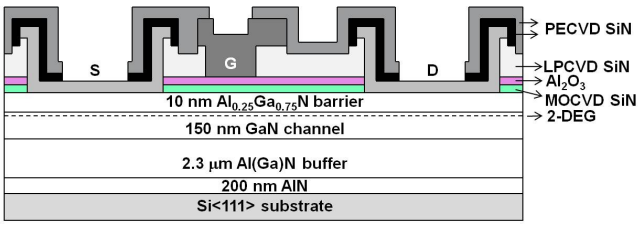

Fig. 1. Schematic diagram of the device.

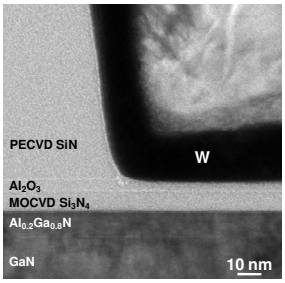

Fig. 2. TEM cross-section of the gate area after full device processing.

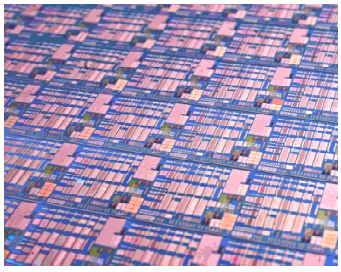

Fig. 3. Detail of a fully processed 150 mm GaN-on-Si wafer.

Compared to Si_3N_4, Al_2O_3 has a larger bandgap (~7 eV vs ~5 eV), higher dielectric constant (ε ~9) and high breakdown field (~10 MV/cm) [4], making it a very attractive dielectric for realizing MISHEMT devices. High-quality Al_2O_3 films are usually deposited by atomic layer deposition (ALD). Unfortunately the density of interface states (D_{it}) is still large with this growth technique: in the order of 10^{12} cm^{-2} eV^{-1} or higher [5], [6], and is believed to result in devices with poor breakdown behavior [7], [8]. This Al_2O_3 breakdown problem had to be overcome during the course of the project where we were able to demonstrate a novel concept for manufacture of robust devices using a Si_3N_4/Al_2O_3 bilayer as both gate dielectric and surface passivation.

The devices are fabricated on 150 mm-diameter Si substrates through a fully Si-CMOS process-compatible process using stepper lithography, patterning by dry etching and Au-free metallization schemes. The process can be run in a standard CMOS fab because only the commonly-used metals W, Ti, Al and Cu were used. Moreover, the contamination control of Ga, being a p-type dopant for Si, was initially felt to be a cause for concern. However, our data shows that by optimization of some process steps, the Ga contamination level stays well below the Si contamination risk limit allowing the approach to be readily introduced in a standard Si process flow.

III. Device Fabrication

Fig. 1 shows a simplified cross-sectional view of the fabricated MISHEMT. The undoped AlGaN/GaN/AlGaN double heterostructure epilayer was grown by MOCVD and consists of a 200 nm AlN nucleation layer, a buffer consisting of 450 nm $Al_{0.70}Ga_{0.30}N$, 800 nm $Al_{0.40}Ga_{0.60}N$ and 1050 nm $Al_{0.18}Ga_{0.82}N$, a 150 nm GaN channel, a 10 nm $Al_{0.25}Ga_{0.75}N$ barrier layer and a 5 nm or 10 nm in-situ grown Si_3N_4 surface passivation layer. Next, 5 nm or 10 nm Al_2O_3 was deposited by ALD at 300 °C using $Al(CH_3)_3$ and H_2O as precursors. To improve the interface quality, the ALD film was annealed at 700 °C for 1 min in forming gas (5% H_2, 95% N_2). This was followed by 120 nm low pressure chemical vapor (LPCVD) nitride deposited at 800 °C. The transmission electron microscopy (TEM) cross-section of the gate area after full device processing, shown in Fig. 2, illustrates the amorphous bilayer gate dielectric on top of the AlGaN barrier. Ohmic contacts were formed by etching the triple dielectric stack with a 5 W SF_6 plasma for the Si_3N_4 layers and a 40 W Cl_2-based plasma for the Al_2O_3 layer. This was followed by 20/100/20 nm Ti/Al/W deposition, dry etching of the metal stack and alloy at 600 °C for 1 min in N_2. The contact resistance was 0.65 Ω·mm. Before N-implant isolation (160 keV, 3×10^{13} at/cm^2), the ohmic metal was capped by a patterned plasma enhanced chemical vapor deposited (PECVD) nitride at 400 °C. The gate was formed by selective removal of the LPCVD nitride in a 5 W SF_6 plasma using Al_2O_3 as an etch stop layer, followed by deposition and dry etching of the 30/20/250 nm W/Ti/Al gate metal stack. A gate-connected fieldplate was formed by extending the gate metallization by 1 µm to the drain side. The process was completed by Al and Cu interconnect metallization layers. All device geometries contained multiple gate fingers, ranging from small test devices having a total gate periphery of 200 µm up to large periphery power transistors with 10 mm, 20 mm, 40 mm, 60 mm and 100 mm total gatewidth respectively. For all transistors, the gate length is 1.5 µm, the gate-source distance is 1.25 µm and the gate-drain distance is 9.5 µm. Fig. 3 shows a detail of a fully processed 150 mm GaN-on-Si wafer.

IV. Device Characterization

Initially, small 200 µm gatewidth test devices were characterized on wafer. As an example Fig. 4(a) shows the DC transfer characteristics for devices using the 10/5 nm Si_3N_4/Al_2O_3 as a gate dielectric. The subthreshold slope is 80 mV/decade. The drain leakage and gate leakage in pinch-off is below 1×10^{-10} A/mm. The forward-bias gate leakage curves for wafers with 10/5 nm and 5/10 nm Si_3N_4/Al_2O_3 gate dielectric are compared in Fig. 4(b) to a reference wafer with a single 15 nm Al_2O_3 layer gate dielectric. By adding in-situ Si_3N_4 below Al_2O_3, the leakage current is reduced by several orders of magnitude. This leakage difference is due to N-vacancies at the AlGaN interface that act as deep donor-like states that can only be adequately passivated by the use of an in-situ nitride [10], [11]. Indeed, the $\ln(I_G)$ versus $1/V_{GS}$ dependence, as shown in the inset of Fig. 3(b), is consistent with trap-assisted-tunneling [12] for the Al_2O_3-only case, whereas it is not for the bilayer gate dielectric.

The off-state high voltage drain leakage current was mapped over the 23 dies on the 150 mm wafers. For all thickness combinations of the Si_3N_4/Al_2O_3 gate dielectric bilayer, the hard device breakdown voltage was 850 ± 90 V, in agreement with the expected value for a 2.3 µm-thick GaN-based buffer on a Si substrate and for 9.5 µm gate-drain distance [13], [14], whereas the breakdown was poor and very spread for the Al_2O_3-only reference case. The improved breakdown behavior is believed to be related to the higher-quality semiconductor/dielectric interface, as is known for in-situ Si_3N_4 [1]. This is supported by the reduction in gate-current (Fig. 3b) and disappearance of the trap-assisted tunneling dependence. It is likely that insertion of the in-situ Si_3N_4 also improves the interface with the Al_2O_3, analogous to a SiO_2 transition layer for high-k dielectrics on Si [10].

The suppression of dispersion is a key factor for successful implementation of power devices in converters. Fig. 5 shows the pulsed I-V measurements for two different quiescent bias conditions: (V_{GS}, V_{DS}) = (0 V, 0 V) and (-5 V, 50 V). The pulsed drain current at V_{DS} = 10 V and V_{GS} = 3 V is 0.6 A/mm. The graph shows low dispersion (<5%) till 50 V, which is the limit of our experimental set-up.

Next, using the processing method detailed above, 20-mm wide power transistors were fabricated. The pulsed I_D-V_{DS} output current characteristics are shown in Fig. 6. The on-resistance was extracted at V_{GS} = 2 V, V_{DS} = 1 V as 9.1 Ω·mm. Taking into account the full active area of the device

(1 mm × 0.63 mm) with exclusion of the bondpath area, the specific on-resistance $R_{on,sp}$ was calculated as 2.9 mΩ·cm^2. Fig. 7 shows the high-voltage off-state leakage. The off-state drain leakage at 600 V was as low as 7 µA which is to our knowledge among the best values reported for high power GaN-on-Si devices. The drain current is limited by buffer leakage as determined from isolation test-structures.

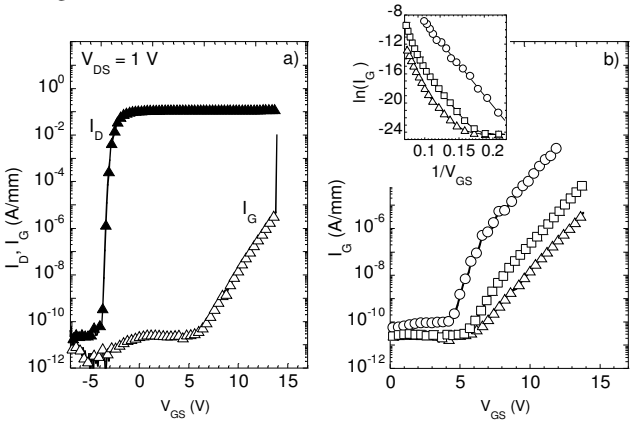

Fig. 4. (a) DC I-V transfer characteristics (I_D and I_G versus V_{GS}) of a MISHEMT with a bilayer gate dielectric consisting of 10 nm in-situ Si_3N_4 and 5 nm ALD Al_2O_3; (b) gate-source bias dependence of gate current in MISHEMT diodes with 15 nm Al_2O_3 (circles), 5/10 nm Si_3N_4/Al_2O_3 (squares) and 10/5 nm Si_3N_4/Al_2O_3 (triangles).

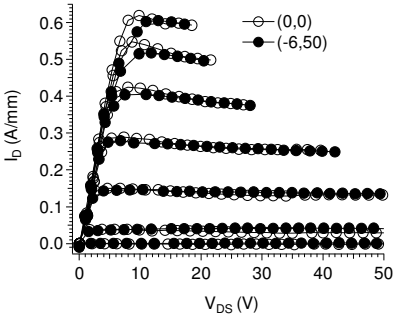

Fig. 5. Pulsed I-V characteristics (from V_{GS} = 3 V, step 1 V) from quiescent bias points (V_{GS}, V_{DS}) = (0 V, 0 V) (open symbols) and (V_{GS}, V_{DS}) = (-5 V, 50 V) (closed symbols). The pulsewidth is 400 ns and the pulse separation is 1 ms.

V. Device Stability at High Temperature and Under Heavy Ion Radiation

Gallium nitride devices are very promising for space applications, because they are expected to behave very well in harsh environments due to their wide band gap and high bond strength. Two key aspects of device stability in harsh environments are: high-temperature stability and stability under heavy ion radiation.

For the high temperature stability characterisation small devices with 500 µm total gate width were tested, as well as power transistors with a total gate width up to 40 mm while the gate-to-drain distance was 5 µm for 500 µm-width transistors and 9.5 µm for the 40 mm power transistors. The results are compared to a Si VDMOS power MOSFET reference device.

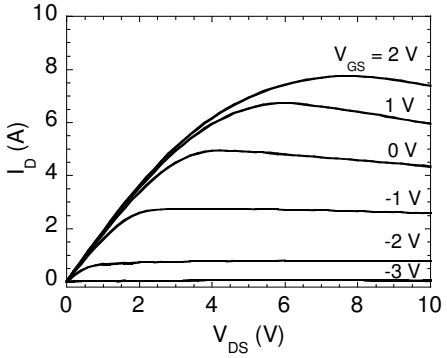

Fig. 6. Pulsed I_D-V_{DS} curves (pulsewidth 1 ms) of a 20 mm-wide power transistor. The maximum output current is 8 A and the specific on-resistance is 2.9 mΩ·cm^2.

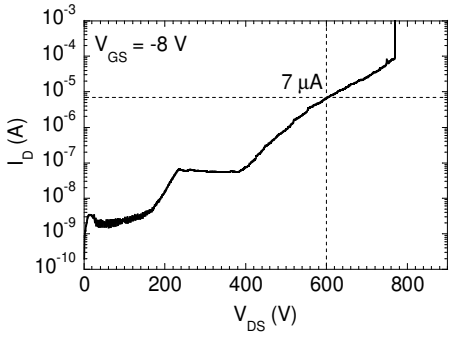

Fig. 7. High voltage off-state drain leakage of a 20 mm-wide power transistor. The off-state drain leakage at 600 V is 7 µA.

The devices were tested in the temperature range 25-200°C. Characteristics of drain current (I_D) versus gate voltage (V_{GS}) and drain voltage (V_{DS}) were recorded at different temperatures to determine the main DC parameters, such as the threshold voltage, transconductance, maximum current and on-resistance. Furthermore, the gate and drain leakage currents were measured at different temperatures in the voltage range V_{DS} = 0-400 V.

An important issue in the thermal behavior of power devices is the risk of thermal runaway. Fig. 8 shows two sets of I_D-V_{GS} characteristics at different temperatures, one for the Si VDMOS reference device, the other for a GaN power device. In the power MOSFET the curves at different temperatures show a crossing point, where the temperature coefficient changes from negative to positive. This crossing point is a result of a reduction in threshold voltage and mobility degradation with temperature. Above this point the current at high temperature is reduced. This effect improves the thermal stability as the device heats up in this operating region, but the mobility reduction reduces the current at high temperature and hence, the selfheating becomes self-limited. Therefore, the thermal stable point should be as low as possible. In the case of our GaN demonstrator device, it is evidently at a much lower current level than in the silicon

device. This is an important asset of the GaN device over the power MOSFET device.

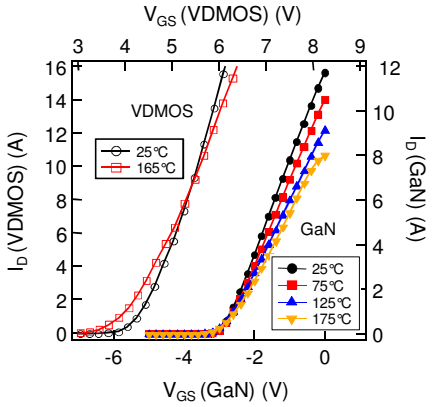

Fig. 8. I_D-V_{GS} for GaN and MOSFET VDMOS power device at different temperatures.

The on-resistance of the depletion-mode GaN transistors was determined from the I_D-V_{DS} characteristics in the linear region (V_{GS} = 0 V, V_{DS} = 1 V). As the temperature increases, the on-resistance increases almost linearly and roughly doubles between 25°C and 200°C as a result of mobility degradation. This is shown in Fig. 10, which represents the data normalised to the value at 25°C. The same increase in R_{on} is observed for small (500 µm) devices (●) and 20 mm power transistors (■). Fig. 10 also shows a comparison with the VDMOS power transistor (▲). Evidently, a much higher R_{on} increase with temperature is observed compared to the GaN device.

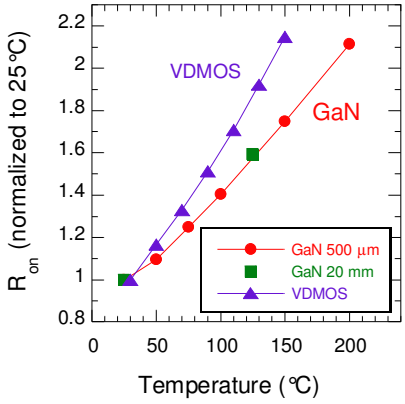

Fig. 9. On-resistance change with temperature for 500 µm-width and 20 mm-width power GaN transistors in comparison to a Si VDMOS power device.

Furthermore, the drain leakage currents ($I_{D,leak}$) were measured in cut-off conditions (V_{GS} = - 7 V) with V_{DS} swept between 0 V and 400 V. The increase of $I_{D,leak}$ with temperature for the 20 mm GaN power transistors is shown in Fig. 10 for different V_{DS} and compared to the behaviour of the Si VDMOS reference device. For both devices the drain leakage current exhibits an exponential increase over the entire temperature range and for different V_{DS} values. Although the current increase with voltage is larger in the GaN device, its sensitivity to a temperature increase is much smaller than for the VDMOS device, which is another asset of the GaN power transistor.

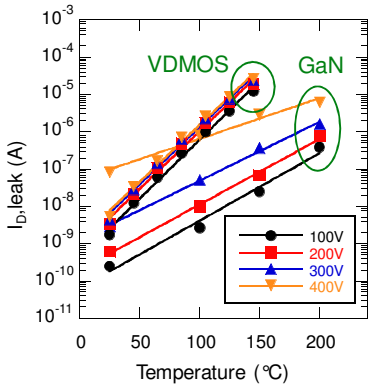

Fig. 10. Drain leakage current versus temperature for different V_{DS}: comparison between GaN and VDMOS device.

AlGaN/GaN HEMTs have promising applications in space due to the inherent strength of the material for different ionizing and non-ionizing radiation types as indicated in previous work [15-16]. In other work, authors identified single event gate rupture (SEGR) of the AlGaN barrier, as one of the main radiation induced failure modes for this type of transistor [17]. In this project we have tested for the first time the stability of a high voltage GaN technology with an insulated gate under high energy heavy ion irradiation and have used statistical distribution functions to evaluate the impact of several parameters on the degradation. During this testing the devices were biased in the off-state with a high voltage drain bias. Using a gate dielectric has advantages for creating components with low gate leakage, but can introduce extra problems when irradiated, such as charge trapping in the gate dielectric or dielectric rupture [18].

As a first step to evaluate the radiation hardness of the technology, we have performed high energy heavy ion irradiation with various ion species: Ne, Ar, Kr and Xe. The radiation experiment was performed at the cyclotron in Louvain-la-Neuve, Belgium. During the test run the components were biased in the off-state with a high voltage applied to the drain, ranging from 75 V to 480 V. Both gate and drain bias were varied for different experiments to study the impact on the radiation damage. The drain and gate currents were continuously monitored during radiation testing. It was observed that during irradiation, parasitic switching events occurred, during which the transistor switched on without an external control of the gate potential. During these events the drain current increased from its nominal value in the off-state. The effect of the fluence was studied first and, as can be seen in Fig. 11a, we observed an increasing degradation for higher fluences. The device geometry and gate and drain bias were varied in a next step to study the impact of the electrical fields in the component. It was found that the gate bias did not have a discernable effect on the results. The data indicated a trend of increasing gate leakage after

irradiation for a higher drain bias, shown in Fig. 11b. It was also found that the device with the smaller gate-drain distance exhibited more degradation. This indicates that the electrical fields in the component act as an acceleration factor for the radiation-induced gate degradation. Plotting on-resistance data versus ion species (Fig. 12) revealed however that the on-resistance exhibited a progressive degradation for the ions with higher atom number. Furthermore, we also observed V_t shifts, both positive and negative, and spikes in I_G for forward gate bias, both shown on Fig. 13. The spikes might indicate that after irradiation a percolation path was formed through the gate insulation. However, the components were still fully functional after irradiation, albeit with a leaky gate. The level of gate leakage was however still on the same order of magnitude as obtained from Schottky gate HEMT realisations (10-100 µA/mm).

In conclusion, we have observed that MISHEMTS are extremely hard for single event burnout (SEB), with no observed SEB events during the entire test run. As also observed in other works, the main degradation mechanism is SEGR, however, for our case the degradation was related to the gate dielectric and not the AlGaN barrier layer.

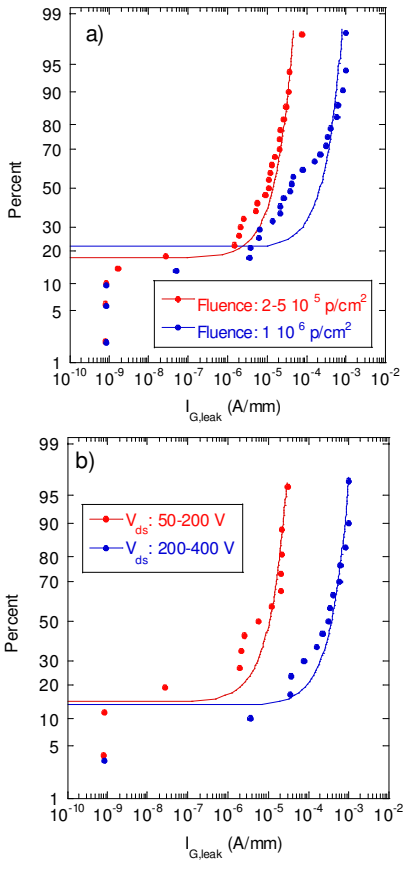

Fig. 11. Probability plot for an exponential distribution for the gate leakage current after irradiation for different fluences (a) and for different drain biases for the devices with L_{GD} = 5 µm (b).Typical values before irradiation were 10^{-10}A/mm.

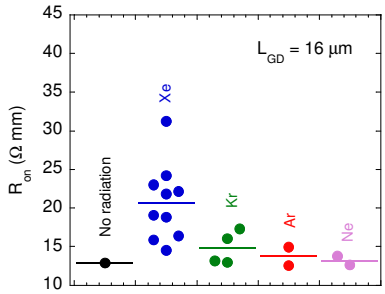

Fig. 12. Increasing degradation of the on-resistance after irradiation with heavier ions.

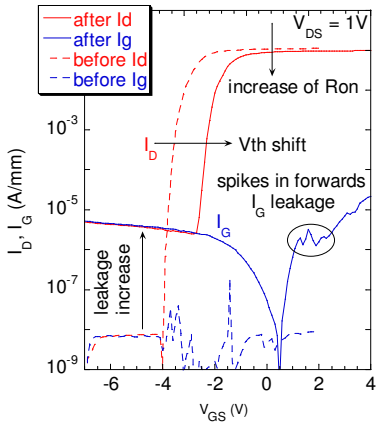

Fig. 13: Typical transfer-characteristics measured before (dotted line) and after (solid line) the radiation experiment with Xe and applied V_{DS} = 384 V, V_{GS} = -8 V. In the picture typical degradation effects induced by radiation are highlighted.

VI. Benchmarking

Table 1 shows the benchmarking of the main electrical parameters of the 60 mm imec project demonstrator devices in comparison to commercially available or prototype Si, SiC and GaN power devices. The selection criteria are based on the maximum drain-source voltage (600 V) and on the DC drain current (12 A). Note that the EPC GaN device is E-mode with a V_{th} of +1.4 V, while both the microGaN and imec GaN devices are D-mode with a V_{th} of -2.8 V and -3.7 V respectively. From this benchmark comparison we conclude that the imec devices are "state-of-the-art" for all parameters. In the comparison with the EPC devices, the imec devices have a larger on-resistance, but much reduced values for the capacitances resulting in devices with, most probably, higher switching speed. In comparison to both the GaN EPC and microGaN devices, especially the low values for the drain and gate leakage of the imec devices are striking.

VII. Conclusion

The goal of the project was to develop processing techniques for manufacture of GaN-on-Si power devices compatible with processing in a Si CMOS production environment and can be viewed as part of the wider ESA strategy that is aimed at the

development of a European commercial supply chain for space compatible GaN-on-Si power devices. Starting from an early GaN-on-Si power process in a III-V lab environment, we were able to demonstrate a very competitive, if not the best-in-class, Si CMOS-compatible D-mode process on 150 mm Si wafers. Moreover, imec was in 2012 the first in the world to demonstrate GaN-on-Si E-mode power devices in a 200 mm Si CMOS fabrication facility.

	Si power MOSFET - ST - STB19NF20	**Si power MOSFET - ST** - STL18NM60N	**Si CoolMOS - INFINEON** - IPW60R250CP	**Si IGBT - IR** - IRGB4045DPbF	**SiC MOSFET - Cree** - CMF10120D	**GaN E-Mode - EPC** - EPC1010	**GaN D-Mode - microGaN** - MGG1T0617T	**GaN D-Mode - IMEC – 60 mm** MP17
VBD (V)	200	600	600	200	1200	200	600	600
ID (A)	15	12	12	12	24	12	12	12
Vth (V)	+3	+3	+3	+4	+2.4	+1.4	-2.8	-3.7
Ron (Ω)	0.15	0.26	0.22	-	0.16	0.03	0.2	0.1😐
ID,leak (μA)	1	1	1	25	0.5	50	500	30 ☺
IG,leak (μA)	0.1	0.1	0.1	0.1	0.25	200	500	3 ☺
CISS (pF)	800	1000	1200	350	930	440	9	113 😐
COSS (pF)	165	60	54	29	63	310	32	17 ☺
CRISS (pF)	26	3	1	10	7.5	30	8	8.4 😐
Qg (nC)	24	35	26	19.5	11.8	7.5	7.4	8.6 😐

Table 1. Benchmarking of main electrical parameters of the imec 60 mm powerbars in comparison to Si, SiC and Ga power devices.

The process flow is a MISHEMT that includes an *in situ* Si_3N_4 / ALD Al_2O_3 bilayer as the gate dielectric. With this new and unique concept we were able to reach all targeted specifications of the demonstrator. We benchmarked the electrical data with Si, SiC and GaN commercial or prototype power products and concluded that our devices are very competitive since they offer improved performance (leakage, gate charge, capacitance, ...) over competitor products. Moreover, the devices were successfully characterized for high temperature operation and evaluated under heavy ion radiation. The heavy ion radiation tests showed that the imec approach was robust in terms of burn-out, however radiation induced damage to the gate dielectric did occur degrading transistor leakage and changing threshold voltage parameters. Future work shall investigate approaches to realize E-mode devices with improved radiation robustness.

ACKNOWLEDGMENT

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