Abstract

Advanced Development of III-Nitride Material for High Power Components

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This document summarises results from the "Advanced Development of III-Nitride Material for High Power Components" project (ESTEC contract. no. 20073/06/NL/PA). It was aimed at the development of high quality AlGaN/GaN epitaxial layers suited for microwave device application and to demonstrate AlGaN/GaN HEMT transistors based upon optimized heterostructures. With the goal of replacing low thermal conductivity sapphire, three different types of substrates were studied in this project: SiC, Si and self-standing GaN pseudo-substrates. The project enabled IMEC (Belgium) to improve its III-Nitrides epitaxial growth, its GaN technology and its device measurement capability. In particular, the development of a specific in-situ SiN passivation was found to be of great significance for GaN electronics. The project further enabled LUMILOG (France) to develop semi-insulating GaN substrates suited for microwave electronics application.

***Index Terms*— III-Nitrides, GaN, GaN-on-Si, GaN substrates, HEMT, RF, Power, GaN for SSPA space applications**

I. INTRODUCTION

Regarding the unique properties (high breakdown field, high power density, high temperature operation, robustness) that the wide bandgap confers to AlGaN compound semiconductors, as well as the excellent transport properties obtained in the 2DEG (two-dimensional electron gas) formed at the AlGaN/GaN heterostructure, III-Nitrides are now broadly recognized as a key technology for many space applications. The success of the ESA-MODs workshops, with the last one held in Ulm in March 2009, is, among others, a strong indicator of the interest of the space community for components and systems based on these wide band gap semiconductors [1]. Space applications range from satellite communication (power amplifier, receivers, low-noise amplifiers…) to solar power converters or even solar-blind detectors.

The active parts of III-Nitride components (e.g. the transistor channel) require the development of high quality epitaxial growth techniques. Today, the most successful technique to grow advanced III-N heterostructures is Metal-Organic Vapor Phase Deposition (MOCVD). Regarding the importance of the III-Nitride technology for space, it appears of strategic importance to develop in Europe a high quality source of epitaxial material, suitable for fabrication of high performance devices. At IMEC, significant improvement in Metal Organic Vapour Phase Epitaxy (MOVPE) growth of GaN heterostructures has been demonstrated over the last ten years. This has been first achieved in the ESA contracts: ATHENA [2] and EpiGaN [3] and confirmed by both material and device assessment. A similar methodology of material optimisation through device evaluation has been used within this project, with a further focus on development of device design capability and device characterization assessment through implementation of semi-automated measurement. We report here the major achievements obtained within this "Power-GaN" project.

II. OBJECTIVES

The objectives were to develop a GaN-on-SiC technology for RF power amplification on 2" and 3" substrate diameter, to investigate the use of GaN-on-Si for similar application on larger wafer diameter and to further address lattice matched GaN-on-GaN substrate/device performance using specifically developed semi-insulating GaN substrates.

SiC, thanks to high thermal conductivity, is preferred for better and easier thermal management. As its availability is today limited to 3" (lately 4") and its cost remains prohibitive for several applications, Si (111) offers excellent prospects to reduce the cost of GaN components, since it is available in larger wafer diameters (4", 6", or even 8"). However, the large crystal and thermal mismatch requires advanced strain engineering expertise to control stress inside the epitaxial layer stack. Last but not least, homoepitaxy should offer the best technical solution (low dislocation density): however, this not-yet mature technology, especially for semi-insulating material, severely hinders the potential advantage of this substrate.

Besides substrate selection, a second key objective of the project was to drive the optimisation of GaN technology for manufacture of RF power transistors. This has occurred through the development of appropriate scaling techniques (combining thermal management, experimental data and device simulations) and device design optimisation in order to allow fabrication of large gate width power transistors

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(Wg>1mm) for three operating frequency bands (L, C and X band). Another objective was to develop appropriate test and evaluation techniques, including on-wafer mapping measurement capability [4]. Last but not least, a first preliminary reliability study of GaN HEMT devices has been performed.

The activities of the "Power-GaN" ESA-contract covered thus a large scope ranging from MOCVD epitaxy and material characterization, III-Nitride device design, processing and characterization, up to device reliability assessment and device modeling.

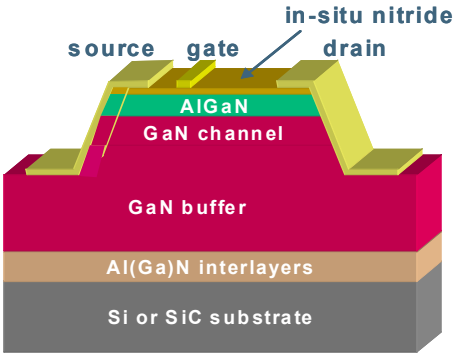

Figure 1: Schematic of the epitaxial structures and associated transistor.

III. III-Nitride Hetero-Epitaxial growth

The epitaxial growth of the AlGaN/GaN heterostructures has been achieved by MOCVD either on semi-insulating SiC, on highly resistive Si (111) (ρ> 5000 Ω.cm) or on GaN substrates, as shown in Figure 1. The starting layers deposited onto the substrates, as well as the buffer layer growth strongly depends on the substrate choice, whereas the optimization of the active part of the heterostructure is essentially independent from substrate selection and relates to the target device performance. Major progress has been made within this project on GaN epitaxial growth; the growth on large diameter Si substrates; the elimination of buffer traps responsible for drain lag effect in the devices; and the use of in-situ SiN passivation [5].

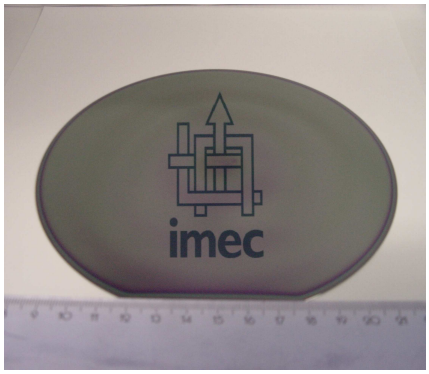

Figure 2: First worldwide demonstration of crack-free growth of AlGaN/GaN HEMT on 150mm Si substrate

Moreover, the reproducibility of IMEC MOCVD epitaxy has been monitored throughout the complete period of the contract and shows a very accurate reproducibility of the electrical and crystalline characteristics, associated with a reduction in wafer bow over time.

Buffer Growth Optimisation

First, an analysis of the incoming substrates is systematically performed. Positive evolution in the SiC substrate quality (from Cree Inc) has been noticed during the course of this project, particularly when moving from 2" to 3" wafer diameter. In the case of heteroepitaxial growth, high quality, highly resistive (>10 GΩ) GaN layers were realized without any intentional p-type doping. Remarkably, the total threading dislocation density in heteroepitaxial GaN layers is in the same order of magnitude (around 10^9 cm^{-2}) for Si and SiC substrates and was found to be comparable to sapphire. For Si and SiC, the growth consists first of a thin high temperature grown AlN layer. In the case of SiC, it is followed by the deposition of a 1.3 µm thick GaN buffer layer at temperature above 1050°C. However, for GaN grown on silicon, the large thermal mismatch between GaN epitaxial layers and silicon substrates requires the growth of an intermediate buffer: if not, it leads to significant wafer bowing or even to severe cracking of the epitaxial nitride layers.

To overcome this problem IMEC has developed stress-engineered structures, based on the use of composition step-graded AlGaN intermediate layers. Initially, AlGaN/GaN HEMT structures were grown on 4"diameter Si wafers. **It is a major achievement of this project that AlGaN/GaN HEMT growth has been also optimized on 6" (150mm) wafer diameter, leading to the first worldwide demonstration of GaN wafers fabricated on 6" silicon substrates that are suited for power electronics application (see figure 2) [6]**. The control of the stress in the heterostructures to achieve epiwafers flat enough to be processed (stepper or even contact lithography) has been monitored using unique advanced in-situ growth monitoring: in the beginning of the contract standard HEMT wafers showed a bow as high as 100µm. At the end of the contract, it was possible to reproducibly and controllably achieve a bow below 20µm, which is within an acceptable range for most processing equipment.

Besides strain control and growth trials on large wafer diameter, the optimization process has also focused on obtaining a highly semi-insulating GaN buffer, with very low trap density. It is widely known in III-Nitride technology that traps lead to severe degradation of the RF performance as compared to the static DC characteristics: this is the so-called "DC-RF dispersion". These effects are enhanced by the high field operation conditions, desired to obtain high power density. The origin of this dispersion can be explained either from the presence of traps in the buffer layers or on the surface (gate edge or eventually below the gate) of a transistor (HEMT). Reducing these dispersion effects starts with trap reduction in the buffer. The understanding of the growth

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mechanism, dislocation density and traps incorporation has been achieved thanks to a detailed study combining Photoluminescence, Transmission Electron Microscopy (TEM), X-Ray and electrical characterization. It was shown that drain lag problems in GaN MOCVD layers relate to yellow luminescence in the GaN buffer. The primary role of carbon incorporation has been evidenced. This allowed to remove dispersion induced by trapping into the material [7].

Finally, to obtain good RF performance on Si substrates, one needs to optimize the interface between the Si substrate and the AlN layer. During the start of the MOCVD epitaxial growth, Al and N species may react with the Si substrate resulting in the formation of a doped layer. Also, an inversion layer may be created at the interface of Si and any high bandgap material. Both phenomena cause a conductive layer to be formed which causes capacitive losses for RF signals. We have characterised this effect by measuring transmission line losses in coplanar waveguides (CPW) deposited on the buffer layer stack (i.e. the HEMT layer stack with the AlGaN cap layer and SiN passivation etched off). As a reference, we also fabricated CPW transmission lines on a blank HR-Si wafer. As is clearly depicted in figure 3, optimised growth conditions reduce RF losses to a level that comes very close to the best-case reference situation on high resistivity silicon. The attenuation of the RF signals on the CPW 50 ohm lines with the optimized buffer remains below 0.3dB/mm for frequencies up to 6GHz.

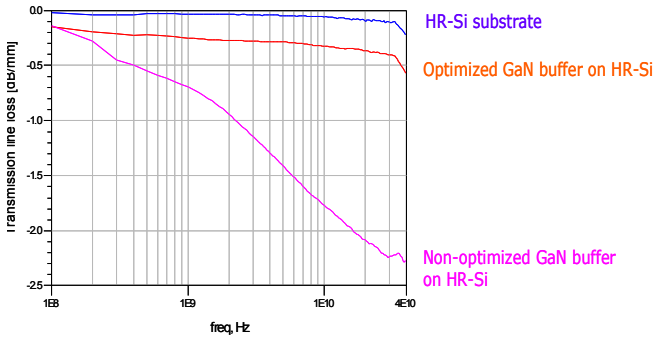

Figure 3: Transmission line losses of coplanar waveguides on different GaN buffers and on highly resistive Si substrate.

Transistor channel and In-situ Si_3N_4 passivation

The Two-Dimensional Electron-Gas (2DEG), which forms the channel of the transistor, is formed by deposition of a 22nm thick AlGaN layer, with 30% of Al and a thin (<5nm) in-situ Si_3N_4 passivation layer. We have proposed and developed this unique in-situ passivation concept based on growth of SiN deposited on top of the AlGaN cap layer in the MOCVD reactor in the same growth run as the rest of the layer stack. The in-situ Si_3N_4 layer has been shown to play two important roles in addition to surface passivation; (i) protecting the top AlGaN surface from external contamination, when exposed to air or during processing and (ii) preventing stress relaxation of the strained AlGaN layer grown on top of the GaN (i.e. by preventing the migration of Ga that causes the formation of strain-mitigating grooves in the AlGaN). The in-situ passivation technique thus allows AlGaN barrier layers to be fabricated with a high Al percentage and hence high sheet charge. As a result, far lower 2DEG sheet resistivity (25% lower) can be achieved on in-situ passivated HEMT layers, as compared to HEMT grown without any SiN in-situ passivation layer. Contact less sheet resistivity mappings for a HEMT layer stack grown using this technique on 100mm and 150 mm diameter Si wafers are shown in figure 4: a mean value of 260Ω/sq. is measured, with a uniformity as good as 1.4%. In a reproducible and controlled way, the HEMTs on SiC also show excellent sheet resistivity values (typ. below 300Ω/sq.) and very high uniformity (typically below 2%).

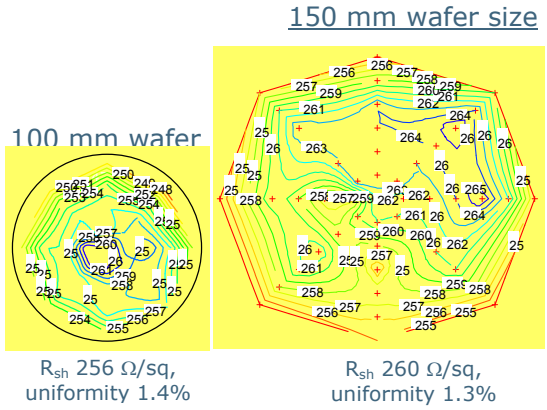

Figure 4: Contact-less Sheet resistivity mapping of SiN/AlGaN/GaN HEMT on Si (111) Substrates

A further important consequence of the role played by in-situ SiN passivation in strain control for HEMT devices resides in the excellent stability of the material at elevated temperatures. Annealing stress tests have been conducted on different epilayer stacks, without any cap, with GaN cap, and with SiN cap. With a SiN cap, no degradation of the channel properties (mobility and carrier density) was observed before and after annealing, up to a temperature of 900ºC. As strain relaxation within the material has often been pointed out in the literature as a cause of degradation during device stress tests, this creates a very good perspective for high reliability device fabrication. Figure 5 illustrates the improved surface morphology obtained using the in-situ SiN cap layer.

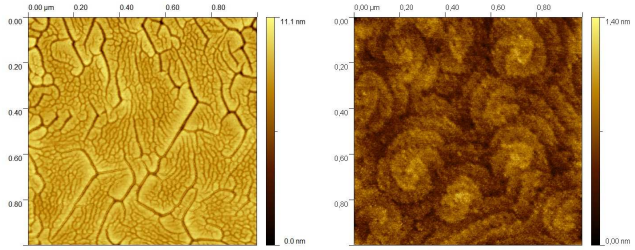

Figure 5: Atomic Force Microscopy of uncapped (left -rms roughness: 1.45nm) and SiN capped (right – rms roughness: 1.15nm) AlGaN/GaN HEMT layers (30% Al in the 22nm thick top AlGaN).

IV. III-NITRIDE RF POWER TRANSISTORS

Device Design Optimisation

A generic mask has been designed for this project, with device designs aiming at operation either in L, C or X band,

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and was used for processing on either Si or SiC substrates. NB: A simpler mask set from a previous project (non-optimised design) was used for processing on GaN substrates.

The device design optimization for SiC and Si substrates has been conducted first through a thermal management study: a finite-element model, supported by comparison with experimental data (Raman measurements of channel temperature in collaboration with Bristol University), has been used to first determine the optimum gate pitch, for the given power densities and as a function of the nature of the substrate. Influence of substrate thinning and vias has also been addressed: as shown in Fig 6, thinning of Si substrate allows to compensate for the lower thermal conductivity of Si compared to SiC. An in-depth RF analysis was then performed, based on measurement results through parameter extraction on the one hand, and on theoretical simulations, on the other hand. Devices with gate width up to 7.2 mm, based on gate fingers with a width ranging from 100 µm to 300µm and with varying gate pitch (50µm to 120µm) were designed. An example of transistors included on the mask set is shown in figure 7.

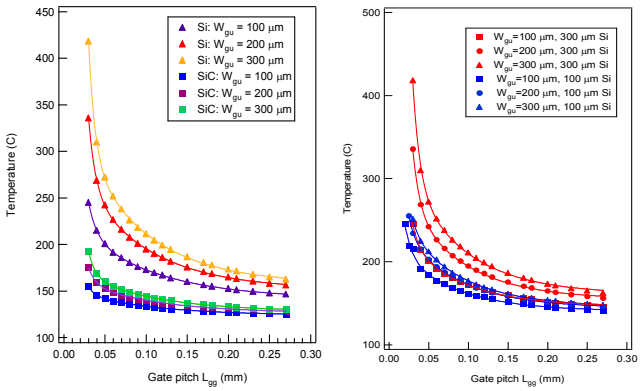

Figure 6: *Left:* Maximum device temperature for HEMT on Si / SiC at P_{diss} = 4W/mm, for different W_{gu} and as a function of the gate pitch L_{gg}. *Right:* Influence of Si substrate thinning on the maximum HEMT temperature.

GaN Technology

The III-Nitride process consists of : a mesa isolation step using an ICP plasma etch based on Cl_2 chemistry; the deposition of TiAlMoAu ohmic contacts that were consecutively rapid thermally annealed at 850°C; the deposition of an interconnect metallisation; the definition of the gates by e-beam lithography producing 500nm long MoAu gates; the deposition and subsequent patterning of a second SiO_2 dielectric layer on top of which source-connected field-plates are eventually defined and finally the fabrication of air-bridges using Au-electroplating. The two critical process steps for high performance devices are the gate and the final passivation layer, which may lead, if not properly processed, to additional current leakage and/or dispersion in the device. A new approach for gate pattern definition has been proposed in this project and revealed to lead to better reliability data: it consists in defining the gate pattern in a thick SiN layer deposited in-situ by MOCVD (>100nm). The gate leakage current achieved either with this method or by keeping the in-situ SiN below the gate are comparable (< 10^{-5} – 10^{-6}A/mm). However, to-date this process has only been successful when used with optical gate lithography processing techniques and needs to be further developed for use with e-beam lithography i.e. to allow sub 0.8µm gate-lengths to be used and high frequency (>10GHz) microwave devices realised.

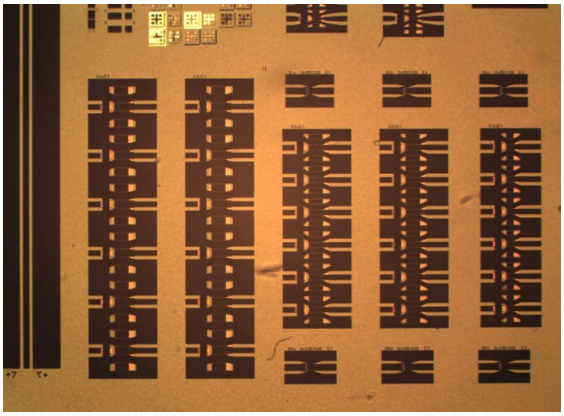

Figure 7: AlGaN/GaN Power bars

Device Results: SiN/AlGaN/GaN HEMT on SiC substrates

HEMT-on-SiC power devices for RF applications were processed on 3" diameter wafers and showed excellent on-wafer power performance from L-band to X-band. CW active load-pull power measurements were performed at 2GHz for 1.5µm gate length transistors. Typical performance obtained was a linear gain of 25dB, a maximum output power of 4.5W/mm, associated with a power added efficiency of 51%, at a drain-source voltage of 25V. CW loadpull measurements were performed on wafer for a 10x250µm device (2.5mm gate width) giving an output power of 39dBm (7.9W or 3.18 W/mm) in L-band (2GHz). The obtained efficiency and linear gain were 37.2% and 14.5dB respectively at 40V bias voltage. **This represents an order of magnitude improvement in absolute output power obtained for a single device fabricated by IMEC prior to the start of this project.**

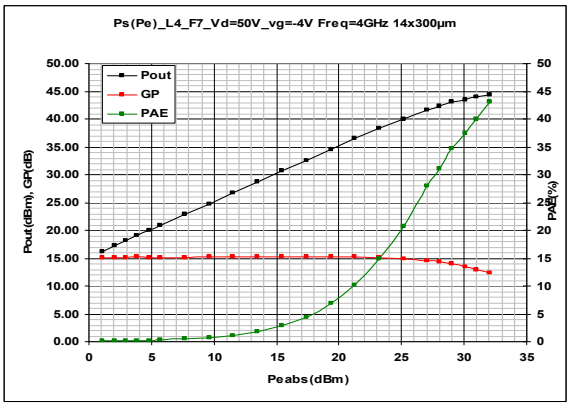

Figure 8: Pulsed Load pull measurement for HEMT on SiC substrates at 4GHz

However, since much of the on wafer measurement investigation was restricted by thermal dissipation limits, pulsed measurements were also performed. Figure 8 shows a pulsed power measurement made on a 14x300um (4.2mm total gate width) device. At 4GHz and V_{ds} = 50V a power density of 6.5W/mm was obtained which corresponds to a total absolute

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output power of 30W measured on-wafer. Due to the extremely linear gain, this occurs at only 2.5dB compression. On a similar device but with smaller gate periphery, a power density of 6.7W/mm has also been measured with 42% PAE and 15dB gain at 8GHz. Remarkably, the gate leakage current was always in the 10^{-5} to 10^{-6} A/mm range or lower.

SiN/AlGaN/GaN HEMT on Si substrates

A similar process as the one developed for fabricating HEMTs on SiC substrates has also allowed IMEC to demonstrate very competitive RF device performance to those shown on SiC substrates, albeit with the proviso that the device design has to be slightly relaxed by using a slightly larger gate pitch. By minimizing the RF loss at the Si/AlN interface while at the same time maintaining low buffer trap density, it is possible to achieve a linear gain of 22dB and a power density as high as 7.9W/mm at a frequency of 2GHz [8]. For a 5mm gate width device a maximum on-wafer output power performance of 20W was demonstrated in pulsed conditions, as shown in Figure 9. At the bias voltage (40V) and input power level that are needed to obtain this output power, the gate current remains below 50µA/mm which should prove beneficial for long term reliability. Also during the pulsed measurement campaign a record performance X band device was also evaluated with 6.7 W/mm power density at 10 GHz and high associated gain of 14.5 dB. These results however do not represent the final limits of our GaN on Si technology as the on-wafer measurements were on un-thinned substrates which was severely limited thermally.

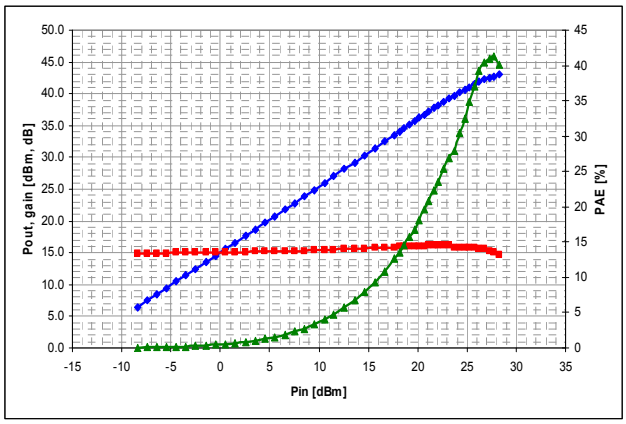

Figure 9: On-wafer pulsed load-pull measurement of HEMT-on-Si substrates with 10µs pulse width and 10% duty cycle at a drain bias of 40V: an output power of 20W is reached on a 5 mm gate width device.

IV. Lattice Matched AlGaN/GaN HEMTs

In a hetero-epitaxy process where GaN buffer layers are grown either on SiC or on Si, the dislocation density is typically in the order of 10^9 cm^{-2}; however, GaN-on-GaN epitaxy can reduce this value by 4 orders of magnitude. In view of optimizing the performance of III-Nitride devices, it appeared quite interesting to investigate the role of dislocations on device performance by developing homoepitaxial hetero-structures. However, self-standing GaN substrates are naturally n-type doped, and as such are useless for any RF application, due to high RF loss generated by the conducting GaN substrate.

LUMILOG has achieved within this project the development of semi-insulating 2" GaN free standing substrates, grown by High Vapour Phase epitaxy, suited for MOCVD epitaxy growth of GaN HEMTs. During the course of the project GaN substrates were supplied with a resistivity of 5×10^7 Ω.cm at 300K; a threading dislocation density lower than $\sim 1\times10^7 cm^{-2}$ and a wafer bow below 20 µm.

Contrarily to heteroepitaxy growth on sapphire or SiC substrates, the achievement of semi-insulating GaN layers required the incorporation of a p-type doping impurity. The crystal quality assessed by HRXRD ranges from 200-360 arcsec for symmetric peak (typ. on sapphire is 290 arcsec) and 200-540 arcsec (typ. on sapphire is 330 arcsec). These results show that better crystalline quality can be achieved as compared to heteroepitaxy.

RF devices were processed on several homoepitaxial wafers, using an optical lift-off pattern definition for the gate. A first impressive characteristic measured using mesa isolation test structures was the high breakdown voltage obtained for the GaN buffer: for two mesa structures separated by a distance of 2µm, the GaN-on-GaN material showed a breakdown voltage of 220V, whereas GaN-on-SiC epi only reached a breakdown of 180V for the same mesa separation distance.

Homoepitaxially grown devices also exhibited very low DC/RF dispersion and the small signal RF performance compared well with the best epilayers grown on SiC substrates (>17dB gain at 2GHz for 1.5µm gate length obtained for devices on GaN substrate). From these device results, IMEC has concluded that the high crystal quality of the GaN templates and HEMT layers is translated in good device performance. However, this could not yet be achieved uniformly over the wafer: indeed, despite the enormous progress observed during this project, GaN substrates still require further optimisation to improve the crystalline uniformity over the 2" wafer size. **A further development area for homoepitaxial HEMTs is the uniformity and substrate size, which needs to be increased to represent a realistic alternative to SiC substrates in the future.**

V. Preliminary Reliability study

As mentioned previously, IMEC has adopted a unique passivation approach, based on in-situ deposition of Si_3N_4 by MOCVD, and therefore it was important to get a first assessment of device behaviour under electrical stress. Preliminary accelerated dc stress tests (up to 90V) in class C bias operation, performed at high temperatures (up to 200°C), as well as under preliminary RF stress tests show the robustness of the technology. However it was observed that some burn-in phase was often required to stabilize the devices under test. These tests have been performed on HEMTs

deposited either on Si or on SiC substrates. In particular, a preliminary study of the impact of the gate technology on device performance degradation has been undertaken, by comparing the two types of gate processing technology used in Power GaN (lift-off or etched gate process) [9].

The lack of statistics precludes drawing any premature conclusion at this stage. However a few outcomes can be summarized here. First, a burn-in procedure seems to be required to ensure long device lifetime. Degradation of a device always appeared within the first hour; after one hour, the device usually remains very stable. Second, it appears that under high electric field conditions, the device degradation depends, in the first instance, on the gate module process rather than on the substrate choice (Si or SiC): in the case of an embedded gate deposited through the in-situ SiN passivation, (etched gate process), no dramatic failure of the devices-under-test was observed in high-field stress test conditions (pinch-off; bias voltage of 60V; temperature up to 200°C). Such HEMT-on-Si devices have even been shown to withstand bias voltages up to 200V for more than 600 hours without any degradation of the device characteristics, including the gate leakage current. Preliminary RF stress tests were performed: they show a quite stable device gain, although PAE and Pout show some drift.

These results provide a good starting point for the ESA-funded GREAT^2 project [11], where a systematic statistical study of the impact of epitaxy, device process and design on device lifetime is to be performed, using both DC and RF stress.

VI. Conclusions - Perspectives

GaN epitaxial growth has reached a maturity level such that outstanding RF power performance can be demonstrated either on SiC, Si or even GaN substrates. On-wafer load-pull measurements on devices fabricated during the course of this project show very good performance whether fabricated on either Si or SiC substrates. However, process reproducibility should still further be improved: in particular, the recently developed gate module, with patterning in thick in-situ SiN will further improve the device robustness and its reliability.

Despite excellent results, the development of very high power devices seems to still encounter limitations (high field, thermal management) that reduce the competitive advantages of this GaN technology over other available RF technologies. An interesting way to increase the intrinsic breakdown voltage is the use of double heterostructure, which also allows for a better confinement of the electrons in the channel [10]. Furthermore, only limited reliability data are today available. All these aspects require further in-depth investigation: the GREAT^2 project should allow a deeper understanding of device breakdown mechanisms, and related GaN device lifetime. An important point to consider for reliability is the impact of dislocations on device lifetime: in case they reveal to play a significant role, the use of GaN substrates may be required for specific applications. Further effort would then be needed to improve the uniformity and availability of larger wafer diameter of semi-insulating epi-ready GaN substrates.

Another area of growing interest, where III-Nitrides will bring a significant breakthrough over existing Si technologies, is High Voltage Switching devices for power conversion. This very large market area however requires cost-competitive technology, solely achievable by large area GaN-on-Si substrates. The concept of developing CMOS compatible processes for III-V fabrication has been proposed by IMEC to further control cost and is partly supported by ESA (ESTEC contract. no. 20713/07/NL/SF). This would represent a significant step forward for developing low cost power converters on Si, but with the advantages offered by GaN compound semiconductors.

ACKNOWLEDGMENT

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