ESA – NPI project

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NPI project between University of Padova and ESA-ESTEC

GaN HEMT Reliability Assessment and Identification of Degradation Mechanisms

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Objectives

The objectives of this project were to complement and augment the conventional Arrhenius based reliability evaluations that have been carried out within GREAT^2.

- Study the failure modes and mechanisms of tested GaN EHMTs related with the application of high drain-source voltages, by means of short tests;
- Develop techniques for the fast evaluation of GaN HEMT reliability, and confirm their accuracy by correlating them with conventional “long-term” accelerated test methods;
- Build a data base concerning failure modes of tested GaN HEMTs, and define rules on how to identify them.

People

University of Padova, Dept. of Information Engineering

- professor Enrico Zanoni
- professor Gaudenzio Meneghesso
- microelectronics group

ESA-ESTEC, TEC-QTC section

- Andrew Barnes
- Fabio Vitobello

Activity on GaN HEMT devices

3 years activity in Padova and in ESTEC laboratories

2 years activity by Antonio Stocco:

- ESTEC 1° placement (2 months): procedure standardization
- ESTEC 2° placement (3 months): DC step-stress on GH50 tech.
- Padova activity: characterization, storage tests, DC life-tests on GH50 tech.

1 year activity by Alberto Zanandrea:

- ESTEC 3° placement (7 months): reliability on GH25 technology and RF step stress set-up implementation

OUTLINE

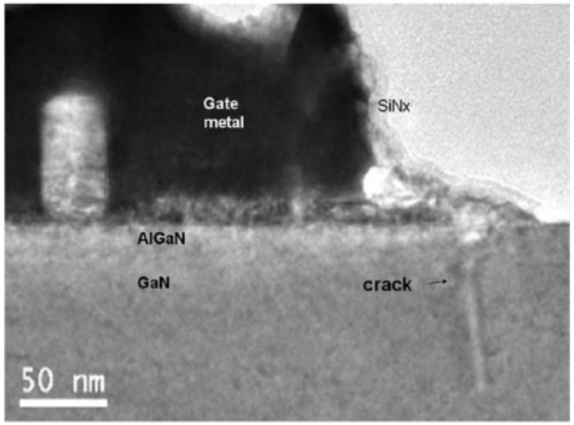
- **Literature review on GaN HEMT Physics of failure**
- **Test plan definition**
- **Thermal characterization**
- **Reliability tests on AlGaN/GaN ESA devices**
- **Storage tests**
- **Long-term reliability tests**
- **Reliability tests on GH25 technology**

Literature review on GaN HEMT physics of failure

Studies on GaN HEMT reliability physics and reports on industrial activities, testify a general trend towards a better understanding of failure mechanisms and of the way to control them.

Nevertheless, still there are a series of issues which need to be solved to achieve full GaN HEMT reliability:

- the origin of the time dependence of the gate leakage degradation mechanism;
- the failure mechanisms related with on-state operation;
- the effect of surface oxidation, oxygen indiffusion or possible corrosion effects;
- the effects of RF overstress and ESD should be studied;
- for space applications, the study of radiation hardness.



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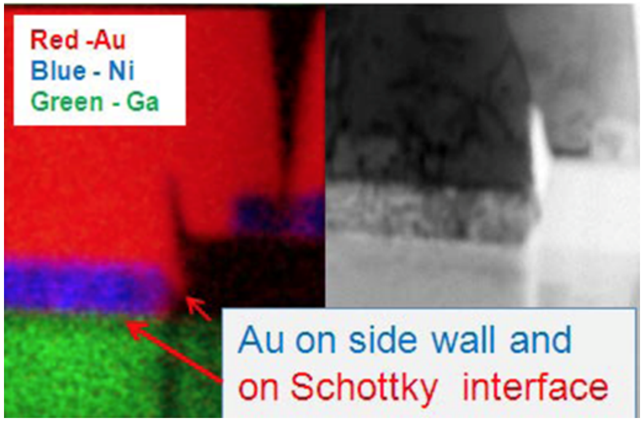

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Test Plan

0 - Characterizations over temperature (in ESTEC) ✓ **completed**

1 - Storage tests (in Padova) ✓ **completed**

1000-hours storage tests on 9 PCM at 3 temperatures

2 - DC step stress tests (*in Padova and in ESTEC*) ✓ **completed**

DC step stress on 6 PCM at 3 bias conditions

3 - DC life tests (in Padova) ✓ **completed**

1000-hours DC life tests on 9 packaged devices, on 3 bias conditions (same T_J)

4 - RF step stress tests (*in ESTEC*)

RF step-stress on 4 PCM, at 2 bias conditions increasing gain compression

5 - RF life tests (*in ESTEC*)

1000-hours RF life tests on 9 packaged devices, at 3 bias conditions (same T_J)

Test Plan: Procedure standardization

Standardization of the measurements procedure of the two labs for a correct data exchange during the following reliability tests.

- ✓ DC measurements
  - ⇘ main electrical parameters (I_{DSS}, g_m, V_{TH}, leakages)
- ✓ Pulsed measurements at different quiescent points
  - ⇘ Slump Ratio
- ✓ Redefinition of test-plan details

Thermal characterization

Temperature characterization: T range from -50°C to 125°C.

- ✓ DC measurements
  - ↳ main electrical parameters (I_{DSS}, g_m, V_{TH}, leakages)
- ✓ Pulsed measurements on big devices
  - ↳ Slump Ratio
- ✓ RF measurements
  - ↳ MAG, f_τ, parasitic capacitances

Main Achievements:

- ***Reduction of I_{DS} and gm and an increase of R_{ON} (mobility reduction)***
- ***decrease of all RF performance (MAG: -0.02 dB/°C)***
- ***Reduction of current collapse effect (6-8% S.R. increase)***

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Reliability tests on GH50 technology

Activity of the second placement in ESTEC laboratories

Intense reliability campaign by means of short-term step-stress tests, with the aim of identifying the voltage operating limits of this technology, and the main failure mechanisms involved.

- OFF-state condition (V_G = -7V);
- SemiON-state condition ($V_G > V_{TH}$);
- ON-state condition (V_G = 0V);

Main Achievements:

- ***very good OFF-state robustness up to around 220V***
- ***semi ON-state robustness around 160V***
- ***Increase of the failure voltage with increasing temperature***
- ***emission spot move close to the drain***

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Storage tests

Storage tests performed on ESA PCMs at 4 different temperatures

↳ understand the highest temperature that a technology can withstand without showing any variation of the device performances;

↳ how performances degrades along the time at different temperatures;

↳ identifying which effects are thermally activated.

T: 375°C, 350°C, 300°C, 325°C

(325 °C added to better understand the previous tests)

Main Achievements:

- ***375°C: more than 80% have reached the failure criteria in 1 hour (gate leakage); Small variation of other parameters (<10%);***
- ***350°C: less severe but similar to 375 (3-5 hrs reach the failure);***
- ***325°C and 300°C: gate leakage first increases but then recovers to the initial gate current level after 1000 hrs of stress.***

(SEM analysis is ongoing at ESA to understand the degradation Mechanisms)

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Long term reliability tests

DC life-tests performed on 9 large-periphery packaged devices

- to better understand the factors that limit the reliability of this technology on long time scale;
- to investigate how degradation effects induced by the bias condition are accelerated by the high test temperature,
- to estimate the device life-time in any real operating condition.

  - **OFF-state condition**
  - **semiON-state condition**
  - **ON-state condition**

Main Achievements:

- ***Very good robustness after 2000h at*** T_J ***= 175°C***
  1. ***Very stable main performances (within 5% change)***
  2. ***Small right threshold voltage shift (possibly thermally activated)***
  3. ***No leakage current increase (no gate-edge degradation)***
  4. ***Stable dynamic performances***

Reliability tests on GH25 technology

Activity of the third placement in ESTEC laboratories

Analysis of the stability of GH25 technology (Milestone 3)

- complete characterization campaign, including basic DC analysis, double pulse measurements, and S-parameters characterization;
- study of the device breakdown, with current-controlled measurements and off-state step stresses;
- long-term reliability DC tests along the typical load-line.

Main Achievements:

- ***Mature and reproducible technology process (DC, pulsed, RF);***
- ***Off state step stress up to 200 V show some increase of gate leakage;***
- ***Life test: three bias point (at 423 K) has been considered (Class A, B, and high current):***
  1. ***Degradation has been observed only in class A in 100 hrs***
  2. ***No degradation in the other bias points even after 300 hrs.***

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