Image Sensor Detailed Specification

STAR 1000 Detailed Specification

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Document history record:

Issue	Date	Description of change
Draft	July 11, 2003	• Origination
1.0	Aug. 5, 2003	• Completion of TBDs • Update of Figure 4a and 5b
1.1	Oct. 22,2003	• Par 4.6.2: Increased high test temperature • Par 5, Table 1b: Increased max temperature and storage temperature
1.2	Jan. 22, 2004	• Par 2, 4.4.1, 4.4.3 updated • Table 1c, 2, 3 7 updated • Figure 2a, 2b: update
1.3	May 12 2004	• Par 4.4.2: Lead material finish thickness corrected
1.4	June 7, 2004	• Appendix D: typical Electro-optical response curve: corrected wrong data
1.5	June 8, 2004	• Table 6: Electrical and electro-optical measurements on completion of environmental tests and at intermediate points and on completion of endurance testing
1.6	Dec. 13, 2004	• Table 1, 1d, 1e, 1f updated • Updated par 4.4.1: thermal resistance • Added Appendix F on observed annealing effects • Table 1: added spec 28a: temperature dependence of ADC ladder network
1.7	May 13, 2005	• Table 1c update • Par 1.9 “soldering instructions” added • Par. 1.10 updated • Table 1b updated
1.8	June 29 2005	• Correction of several typing errors • Par 1.11, 3, 4.1, 4.2 updated • Changed environmental temperature specification to 22±3°C • Table 1c, 1d, 1e, 1f, 4 updated • Added appendix F: observed effects during annealing after total dose irradiation
1.9	Dec. 22, 2005	• Added formulas in par 3 • Added par 4.10: LAT and screening • Tables 1c, 1e, 2, 3a, 3b, 4, 6, 7a, 7b, 7c updated
2.0	March 28, 2006	• Tables 1d, 1e and 1f removed • Par 4.10.2 and 4.10.3 removed • Par 4.2 updated • Par. 4.9.2 updated • Table 4 updated • Table 7a, 7b and 7c updated

Table of contents

1 General

1.1 Scope

This specification details the ratings, physical, geometrical electrical and electro-optical characteristics, test- and inspection-data for a CMOS Active Pixel image Sensor (CMOS APS) based on type STAR1000. The sensor has a format of 1024 by 1024 pixels at 15 µm pitch, and contains an on-chip 10-bit ADC

This specification shall be read in conjunction with the ESCC generic specification ESCC 9020.

1.2 Component type variants

A summary of the type variants of the basic CMOS image sensor is given in Table 1a: “Type variant summary”. The complete list of detailed specifications for each type variant is given in Tables 1c for each type separately.

All specifications in Table 1c are given at 25 ± 3 °C, under nominal clocking and bias conditions. Exceptions are noted in the ‘remarks’ field.

1.3 Maximum rating

The maximum ratings which shall not be exceeded at any time during use or storage are as scheduled in Table 1b.

1.4 Parameter derating information (Figure 1)

Not applicable

1.5 Physical dimensions and geometrical information

The physical dimensions of the assembled component are shown in Figure 2a. The geometrical information in Figure 2b describes the position of the die in the package.

1.6 Pin assignment

Figure 3a contains the pin assignment. The figure contains a schematic drawing and a pin list. A detailed functional description of each pin can be found in Appendix A.

1.7 Timing diagrams

Figure 3b contains the timing diagrams and the timing indications. Appendix B contains a user manual that gives more textual details on how to operate the sensor.

1.8 Functional diagram

Table 3c shows the functional diagram. The user manual in appendix B describes the functionality of the image sensor in more detail.

1.9 Soldering instructions

Soldering is restricted to manual soldering only. No wave or reflow soldering is allowed. For the manual soldering, following restrictions are applicable:

- Solder 1 pin on each of the 4 sides of the sensor
- Cool down period of min. 1 minute before soldering another pin on each of the 4 sides
- Repeat soldering of 1 pin on each side, including a 1 minute cool down period.

1.10 Handling precautions

The component is susceptible to damage by electro-static discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling. The following guidelines are applicable:

- Always manipulate the devices in an ESD controlled environment
- Always store the devices in a shielded environment that protects against ESD damage (at least a non-ESD generating tray and a metal bag)
- Always wear a wrist strap when handling the devices and use ESD safe gloves.

The STAR1000 is classified as class 1A (JEDEC classification – [AD03]) device for ESD sensitivity.

1.11 Storage information

The components must be stored in a dust-free and temperature-, humidity and ESD controlled environment.

- Devices must always be stored in special ESD-safe trays such that the glass window is never touched.
- The trays are closed with EDS-safe rubber bands
- The trays are sealed in an ESD-safe conductive foil in clean room conditions.
- For transport and storage outside a clean room the trays are packed in a second ESD-save bag that is sealed in clean room.

2 Applicable documents

The following documents form part of this specification and shall be read in conjunction with it:

Nr.	Reference	Title	Issue	Date
AD01	ESCC Generic Specification 9020	Charge Coupled Devices, Silicon,Photosensitive	Rev. C	Feb. 1998
AD02	APS-FF-DU-03-006	Electro-optical test methods for CMOS image sensors	1.1	29 nov 2003
AD03	JESD22-A114-B	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	B	June 2000

3 Terms, Definitions Abbreviations, Symbols and Units

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC basic Specification 21300 shall apply.

In addition the following table contains terms that are specific to CMOS image sensors and are not listed in ESCC21300

Symbol	Parameter
INL	**ADC integral non linearity**
DNL	**ADC differential non-linearity**
FPN	**Fixed pattern noise**

The following formulas are applicable to convert %Vsat and mV/s into e- and e-/s:

- $FPN[e-] = \frac{FPN[\%Vsat] * \overline{Vsat}}{conversion\_gain}$
- $Dark\_signal[e-/s] = \frac{Dark\_signal[V/s]}{conversion\_gain}$
- $DSNU[e-] = \frac{DSNU[\%Vsat] * \overline{Vsat}}{conversion\_gain}$
- Conversion gain for STAR1000: 11.5 µV/e-

4 Requirements

4.1 General

At this stage of the evaluation, the requirements for the procurement of the components specified herein are not finalized. These requirements will be based upon the ESCC Generic specification No 9020 for Charge Coupled Devices.

4.2 Deviations from generic specification

Lot acceptance and screening are based on ESCC 9020. Par. **Error! Reference source not found.** describes the lot acceptance and screening.

4.3 Mechanical requirements

4.3.1 Dimension check

The dimensions of the components specified herein shall be checked. They shall comply with the specifications and the tolerances as indicated in Figure 2a.

4.3.2 Geometrical characteristics

The geometrical characteristics of the components specified herein shall be checked. They shall comply with the specifications and the tolerances as indicated in Figure 2b.

4.3.3 Weight

The maximum weight of the components specified herein shall be as specified in Table 1c, item 5.

4.4 Materials and finishes

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the components specified herein to meet the performance requirements of this specification shall be used.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and a glass window.

Type	JLCC-84
Material:	Black Alumina BA-914
Thermal expansion coefficient	7.6 x 10^{-6} /K
Hermeticity	< 5 x 10E-7 atm cc/s
Thermal resistance (Junction to case)	3.633 °C/W

4.4.2 Lead material and finish

Lead material	KOVAR
1e Finish	Nickel, min 2 µm
2nd Finish	Gold, min 1.5 µm

4.4.3 Window

The window material shall be BK7G18 with anti-reflective coating applied on both sides.

The optical quality of the glass shall have the following specification:

Scratch max dimension	<=10 µm
Scratch max number	5
Dig max dimension	<=60 µm
Dig max number	25

The anti reflective coating shall have a reflection coefficient < 1.3% absolute and < 0.8% on average, over a bandwidth from 440 nm to 1100 nm.

4.5 Marking

4.5.1 General

The marking shall consist of a lead identification and traceability information.

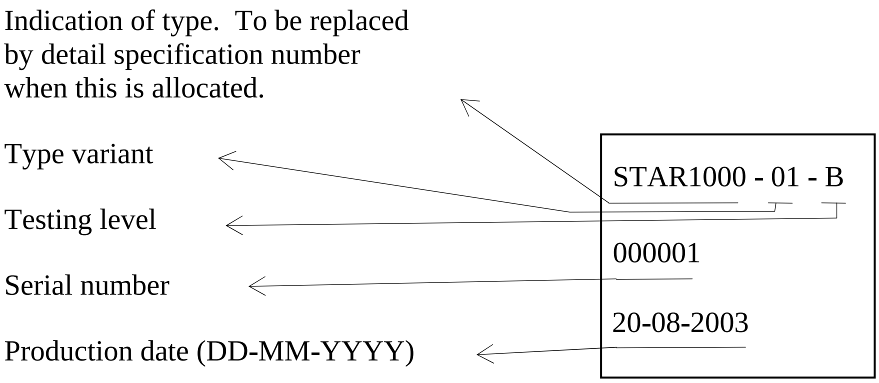
4.5.2 Lead identification

An index to pin 1 shall be located on the top of the package in the position defined in Note 1 to Figure 2a. The pin numbering is clock-wise, when looking at the top-side of the component.

4.5.3 Traceability information

Each component shall be marked such that complete traceability can be maintained.

The component shall bear a number that is constituted as follows:



4.6 Electrical and electro-optical measurements

4.6.1 Electrical and electro-optical measurements at reference temperature

The parameters to be measured to verify the electrical and electro-optical specifications are scheduled in Table2. Unless otherwise specified, the measurements shall be performed at a environmental temperature of 22±3°C.

For all measurements the nominal power supply, bias and clocking conditions apply. The nominal power supply and bias conditions are given in Figure 4a, the timing diagrams in Figure 3b

Remark: The given bias and power supply settings imply that the devices are measured in “soft- reset” condition.

4.6.2 Electrical and electro-optical measurements at high and low temperature

The parameters to be measured to verify the electrical and electro-optical specifications are scheduled in Table 3. Unless otherwise specified, the measurements shall be performed at -40 (-5 +0) °C and at +85 (+5 -0) °C.

4.6.3 Circuits for electrical and electro-optical measurements

Circuits for performing the electro-optical tests in Table 2 are shown in Figure 4.

4.7 Burn-in test

4.7.1 Parameter drift values

The parameter drift values for power burn-in are specified in Table 4 of this specification. Unless otherwise specified the measurements shall be conducted at a environmental temperature of 22±3°C and under nominal power supply, bias and timing conditions.

The parameter drift values (Δ) shall not be exceeded. In addition to these drift value requirements, also the limit values of any parameter -as indicated in Table 2- shall not be exceeded.

4.7.2 Conditions for high temperature reverse bias burn-in

Not Applicable

4.7.3 Conditions for power burn-in

The conditions for power burn-in shall be as specified in Table 5b of this specification

4.7.4 Electrical circuits for high temperature reverse bias burn-in

Not applicable

4.7.5 Electrical circuits for power burn-in

Circuits to perform the power burn-in test are shown in Figure 5b of this specification.

4.8 Environmental and endurance tests

4.8.1 Electrical and electro-optical measurements on completion of environmental test

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at a environmental temperature of 22±3°C. Measurements of dark current must be performed at 22±1°C and the actual environmental temperature must be reported with the test results.

4.8.2 Electrical and electro-optical measurements at intermediate point during endurance test

The parameters to be measured at intermediate points during endurance test of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at a environmental temperature of 22±3°C

4.8.3 Electrical and electro-optical measurements on completion of endurance test

The parameters to be measured on completion of endurance tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at a environmental temperature of 22±3°C

4.8.4 Conditions for operating life test

The conditions for operating life tests shall be as specified in Table 5b of this specification.

4.8.5 Electrical circuits for operating life test

Circuits for performing the operating life test are shown in figure 5b of this specification.

4.8.6 Conditions for high temperature storage test

The temperature to be applied shall be the maximum storage temperature specified in Table 1b of this specification.

4.9 Total dose radiation test

4.9.1 Application

The total dose radiation test shall be performed in accordance with the requirements of ESCC Basic specification 22900

4.9.2 Parameter drift values

The allowable parameter drift values after total dose irradiation are listed in Table 4. The parameters shown are valid after a total dose of 270Krad and 168h/100°C annealing.

4.9.3 Bias conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

4.9.4 Electrical and electro-optical measurements

The parameters to be measured, prior to, during and on completion of the irradiation are listed in Table 7 of this specification. Only devices that meet the specification in Table 1 of this specification shall be included in the test sample.

4.10 Lot acceptance and screening

This document describes the LAT and screening on the STAR250FM devices.

All tests on device level have to be performed on screened devices.

4.10.1 Wafer lot acceptance

This is the acceptance of the silicon wafer lot. This has to be done on every wafer lot with STAR250 and STAR1000 always being separated lots.

Test	Test method	Number of devices	Test condition	Test location
Wafer processing data review	PID	NA	NA	CY
SEM	ESCC 21400	4 naked dies	NA	IGG
Total dose test	ESCC 22900	3 devices	100 krad	ESTEC by CY
Endurance test	PID	6 devices	2000h at +125 C	IGG

Before and after total dose test and endurance test:

- Electrical measurements before and after
- Visual inspection before and after
- EO measurements before and after

4.10.2 Assembly lot acceptance

Test	Test method	Number of devices	Test condition	Test location
Special MPD in process control				MPD
Bond strength test	MIL-STD-883 method 2011	2	D	MPD
MPD Geometrical data review	Review	All		CY
Solderability Terminal strength Marking permanence	MIL-STD883, method 2003 MIL-STD 883, Method 2004 ESCC 24800	2	 D	IGG
Geometrical measurements Temperature cycling	PID MIL-STD 883, method 1010	4	 10 cycles - 55/+120	CY IGG
Thermal shock Moisture resistance RGA	MIL-STD 883 method 1011 MIL-STD-883, method 1004 MIL-STD 883, method 1018.3	4	B - 15 shocks - 55/+120 Procedure 1	IGG IGG ORS

Before and after the following tests are done:

- Electrical measurements
- Visual inspection
- Fine leak test
- Gross leak test

4.10.3 Periodic testing

Test	Test method	Number of devices	Test condition	Test location
Mechanical shock	MIL-STD 883, method 2002	2	B - 5 shocks, 1500g – 0,5ms – ½ sine, 3 axes	De Nayer lab
Vibration	MIL-STD 883, Method 2007	2	A - 4 sweeps, 20g 80 to 2000 Hz, 0,06 inch 20 to 80 Hz.	De Nayer lab
Constant acceleration	MIL-STD 883, Method 2001	2	D	De Nayer lab

Before and after the following tests are done:

- Electrical measurements
- Visual inspection
- Fine leak test
- Gross leak test

4.10.4 Screening

Test	**Test method**	**Number of devices**	**Test condition**	**Test location**
Xray		All		IGG
PIND	MIL-STD-883 method 2020	All	A	IGG
Stabilization bake	MIL-STD-883 method 1008	All	48h at 85C.	IGG
Visual inspection	PID	All		CY
RT Electrical measurements	PID	All		CY
Temperature cycling	MIL-STD-883 method 1010	All	B - 10 cycles - 40/+85	IGG
RT Electrical measurements	PID	All		CY
Burn-in	PID	All	240h at +85C.	IGG
Electrical measurements HT/LT/RT	PID	All	HT +85 C LT -40 C	CY
Fine leak test	MIL-STD-883 method 1014	All	Read and record.	IGG
Gross leak test	MIL-STD-883 method 1014		Perfluorocarbon test	IGG
Visual inspection	PID	All		CY

5 Tables and figures

Table 1a: Type variant summary

Variant	Number of FPN defects	Number of DSNU defects	Number of PRNU defects
01	0	0	0

Table 1b: Maximum ratings

No	Characteristics	Symbol	Limits		Units	Remarks
			Min	Max		
1	Any supply voltage		-0.5	+7	V	
2	Voltage on any input terminal		-0.5	Vdd + 0.5	V	
3	Operating temperature		-40	+85	°C	
4	Storage temperature (momentarily)		-40	+120	°C	Not longer than 1 hour.
5	Storage temperature (long term)		-40	+85	°C	
6	Soldering temperature		NA	260	°C	Hand soldering only; see par.1.9 for soldering instructions

Table 1c: Detailed specification all Type variants

Design specifications							
No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
1	Image sensor format		1024 by 1024 pixels				
2	Pixel size		15 by 15			µm	
3	ADC resolution		10 bit				
	Timing diagram		Figure 3b				

Mechanical specifications							
No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
4	Flatness of image area		NA	NA	10	µm	Peak-to-peak at 25 ± 3 °C
4b	Total tickness		2.7	2.8	2.9	mm	Package + epoxy + glass lid
4c	Die position, X offset		0.002	0.052	0.102	mm	
4d	Die position, Y offset		0.10	0.20	0.30	mm	
4e	Die position, parallelism		-0.05	0	0.05	mm	
4f	Die position, Y tilt		-0.05	0	0.05	mm	
5	Weight		6.3	6.55	6.8	g	

Window specifications							
No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
6	Spectral range for optical coating of window		440	NA	1100	nm	To be confirmed by window manufacturer
7	Reflection coefficient for window		NA	<0.8	<1.3	%	Over bandwidth indicated in 6
8	Optical quality: Scratch max width Scratch max number Dig max size Dig max number		NA	NA	 10 5 60 25	 μm μm 	

Environmental specifications							
No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
9	Operating temperature range		-40	NA	+85	°C	
10	Total dose radiation tolerance		230	NA	NA	Krad (Si)	Device still operating to specification in Table 1d
11	Equivalent proton fluence		$2.4E^{11}$	NA	NA	Proton/cm^2	Proton energy: 60MeV Device still operating to specification in Table 1e
12	SEL threshold		127.8	NA	NA	MeV cm^3 mg^{-1}	Device still operating to specification in Table 1f

Electrical specifications							
No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
13	Total power supply current stand-by		NA	53.8	56.6	mA	Under nominal bias conditions and at nominal pixel rate
14	Total power supply current, operational		NA	57.4	60.8	mA	Under nominal bias conditions and at nominal pixel rate
15	Power supply current to ADC, operational		NA	44.6	48	mA	Under nominal bias conditions and at nominal pixel rate
16	Power supply current to image core, operational		NA	12.8	14	mA	Under nominal bias conditions and at nominal pixel rate
17	Input impedance digital input		200	NA	NA	KΩ	Under nominal bias conditions and at nominal pixel rate
18	Input impedance Dark Reference input		200	NA	NA	KΩ	

Electrical specifications							
No	**Characteristics**	**Symbol**	**Limits**			**Units**	**Remarks**
			Min	**Typ**	**Max**		
19	Input impedance ADC input		200	NA	NA	KΩ	
20	Output impedance digital outputs		NA	NA	100	Ω	Note[1]
21	Output impedance analogue output		NA	NA	100	Ω	Note 1
22	Output amplifier voltage range		0.5	NA	4.5	V	Under nominal power supply and bias conditions, at 25 ± 3 °C
23	Dark reference offset		NA	0.6	0.93	V	Note [2]
25	Output amplifier gain setting 1		3.95	4.45	4.96		Note [3]
26	Output amplifier gain setting 2		2.05	2.30	2.55		Note 3~~3~~
27	Output amplifier gain setting 3		7.36	8.38	9.40		Note 3~~3~~
28	ADC ladder network resistance		1054	1174	1295	Ω	at 25 ± 3 °C
28a	ADC ladder network temperature coefficient			4,53		Ω/°C	Between -40°C and +85°C
29	ADC Differential non linearity		NA	3,89	8.4	LSB	
30	ADC Integral non linearity		NA	1,29	1.95	LSB	
31	ADC set-up time		NA	NA	250	ns	To reach 1% conversion accuray
32	ADC delay time		NA	NA	72	ns	To be confirmed after evaluation test

Electro-optical specifications							
No	**Characteristics**	**Symbol**	**Limits**			**Units**	**Remarks**
			Min	**Typ**	**Max**		
33	Saturation voltage output		0.99	1,11	1.24	V	
34	Linear range			95		Ke-	Within ±1%. Note [4]
36	Full well charge			135		Ke-	Note 4.
37	Quantum efficiency x Fillfactor			30	NA	%	Between 450 nm and 750 nm. Refer to appendix C for complete curve

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[1] Output impedance is specified under quasi-static conditions. During transients the output amplifier enters in current-limited mode and the output impedance increases, depending on the capacitive load of the external circuits.

[2] Dark reference offset specifies the offset between the applied dark reference voltage and the actual level at the analogue output terminal. Specified at gain setting 0

[3] Gain specification relative to gain setting 0.

[4] Full well charge and linear range are calculated from detailed electro-optical response measurements.. At this time not enough measurements are available for reliable determination of the minimum and maximum values.

Electro-optical specifications							
No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
38	Responsivity narrow band blue		21000	25300	NA	ADU	At 475 nm ±20 nm
39	Responsivity narrow band green		20500	24800	NA	ADU	At 526 nm ±20 nm
40	Responsivity, narrow band red		18400	23000	NA	ADU	At 630 nm ±20 nm
41	Charge to voltage conversion factor			11.5		μV/e-	Note [5].
42	Temporal noise, nominal clock rate		NA	0.61	0.72	mV	At 22 ± 3 °C and 5 MHz clock rate.
43	Temporal noise, reduced clock rate		NA	0.77	1.02	mV	At 22 ± 3 °C and 2 MHz clock rate.
44	Temporal noise, enhanced clock rate		NA	0.82	1.13	mV	At 22 ± 3 °C and 10 MHz clock rate.
45	Local fixed pattern noise standard deviation, nominal clock rate		NA	0.13	0.20	%Vsat	Note [6] At 22 ± 3 °C and 5 MHz clock rate
46	Global fixed pattern noise standard deviation, nominal clock rate		NA	0.38	0.62	%Vsat	Note [7] At 22 ± 3 °C and 5 MHz clock rate
47	Local fixed pattern noise standard deviation, reduced clock rate		NA	0.20	0.27	%Vsat	Note [8] At22 ± 3 °C and 2 MHz clock rate
48	Global fixed pattern noise standard deviation, reduced clock rate		NA	0.42	0.55	%Vsat	Note At 22 ± 3 °C and 2 MHz clock rate [9]
49	Local fixed pattern noise standard deviation, enhanced clock rate		NA	0.21	0.33	%Vsat	Note [10] At 22 ± 3 °C and 10 MHz clock rate
50	Global fixed pattern noise standard deviation, enhanced clock rate		NA	0.39	0.78	%Vsat	Note [11] At 22 ± 3 °C and 10 MHz clock rate

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[5] Charge to voltage conversion factor is calculated from the detailed electro-optical response measurements.. At this time not enough measurements are available for reliable determination of the minimum and maximum values.

[6] Percentage of full well charge, measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window FPNs.

[7] Percentage of full well charge, measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.

[8] Percentage of full well charge, measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window FPNs.

[9] Percentage of full well charge, measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.

[10] Percentage of full well charge, measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window FPNs.

[11] Percentage of full well charge, measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.

Electro-optical specifications							
No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
51	Number of FPN signal defects	Ndef1	See Table 1a: Type variant summary				
52	FPN limit for Ndef1		15			%	
53	Column FPN		NA	0.37	0.61	%Vsat	At22 ± 3 °C. Note [12]
54	Average dark signal		NA	13.5	28.2	mV/s	At 22 ± 1 °C,
55	Dark signal temperature dependency		NA	9.2	NA	°C	Specification indicates temperature rise for doubling average dark current.
56	Local dark signal non uniformity standard deviation		NA	0.79	1.03	%Vsat	At 22 ± 3 °C. Note [6~~7~~]
57	Global dark signal non uniformity standard deviation		NA	0.99	1.32	%Vsat	At 22 ± 3 °C. Note [7~~8~~]
58	Number of DSNU signal defects		See Table 1a: Type variant summary				
59	DSNU limit for Ndef1		15			%	
60	Local photo response non uniformity, standard deviation		NA	0.95	1.33	%	At 22 ± 3 °C. Note [13]
61	Global photo response non uniformity, standard deviation		NA	3.30	6.09	%	At 22 ± 3 °C Note [14]
62	Number of PRNU defects		See Table 1a: Type variant summary				
63	PRNU limit for Ndef1		15			%	Note 14
64	MTF X direction			0.26	NA		Note [15]
65	MTF Y direction			0.37	NA		

[12] Percentage of full well charge, measured in the complete FPA area.
[13] Percentage of signal (black offset subtracted), measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window PRNUs.
[14] Percentage of signal (black offset subtracted),, measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.
[15] MTF is calculated from the detailed electro-optical response measurements.. At this time not enough measurements are available for reliable determination of the minimum and maximum values.

Electro-optical specifications							
No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
66	Pixel to pixel cross talk X direction		NA	17.5		%	Note [16]
67	Pixel to pixel cross talk Y direction		NA	16		%	Note [16]
68	Anti-blooming capability		NA	X 1000	NA		Anti-blooming is not relevant for CMOS image sensors.

[16] Pixel to pixel optical crosstalk in % of charge in illuminated pixel. At this moment not enough measurements are available to define the minimum and maximum values.

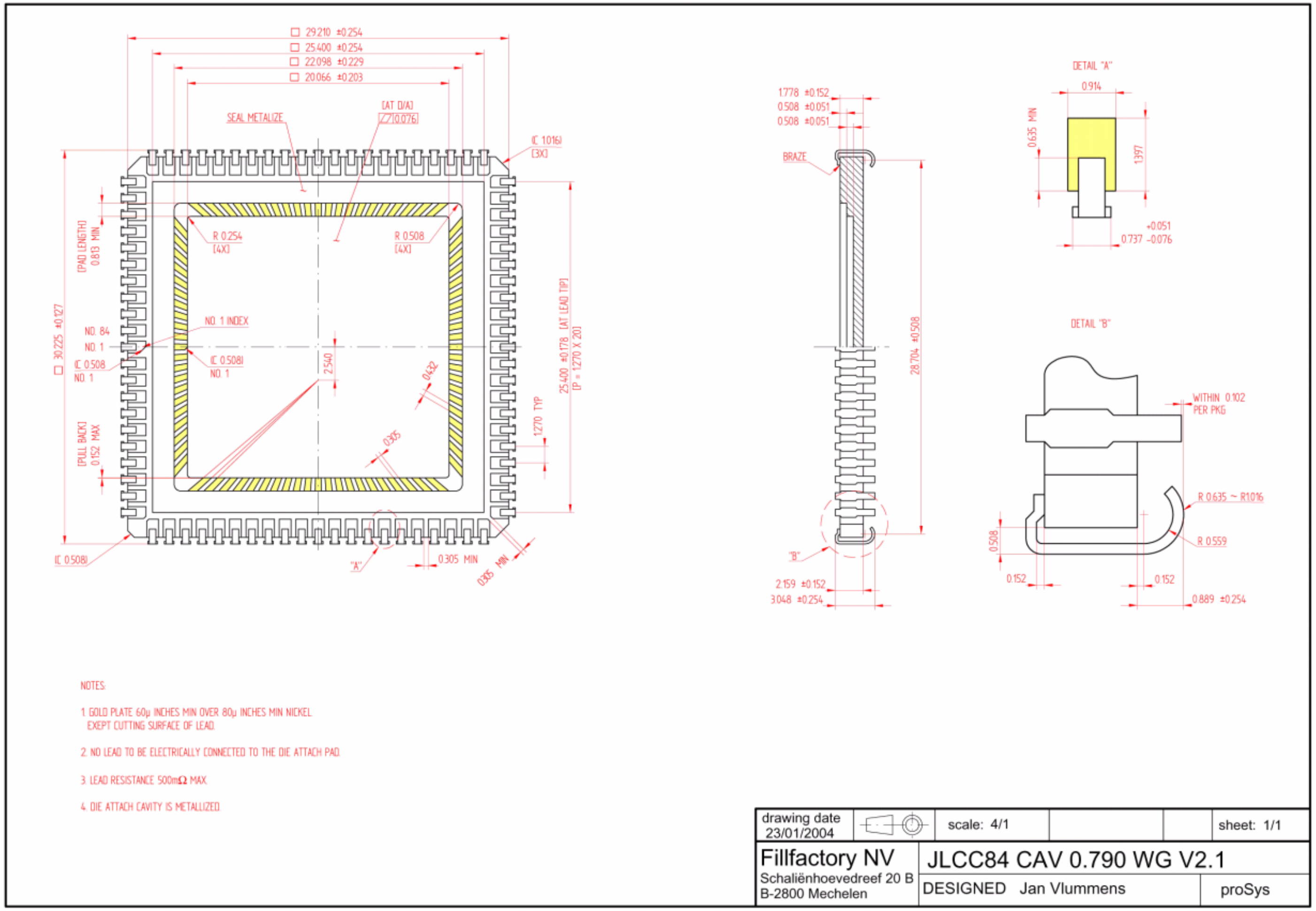


Figure 2a: Physical dimensions

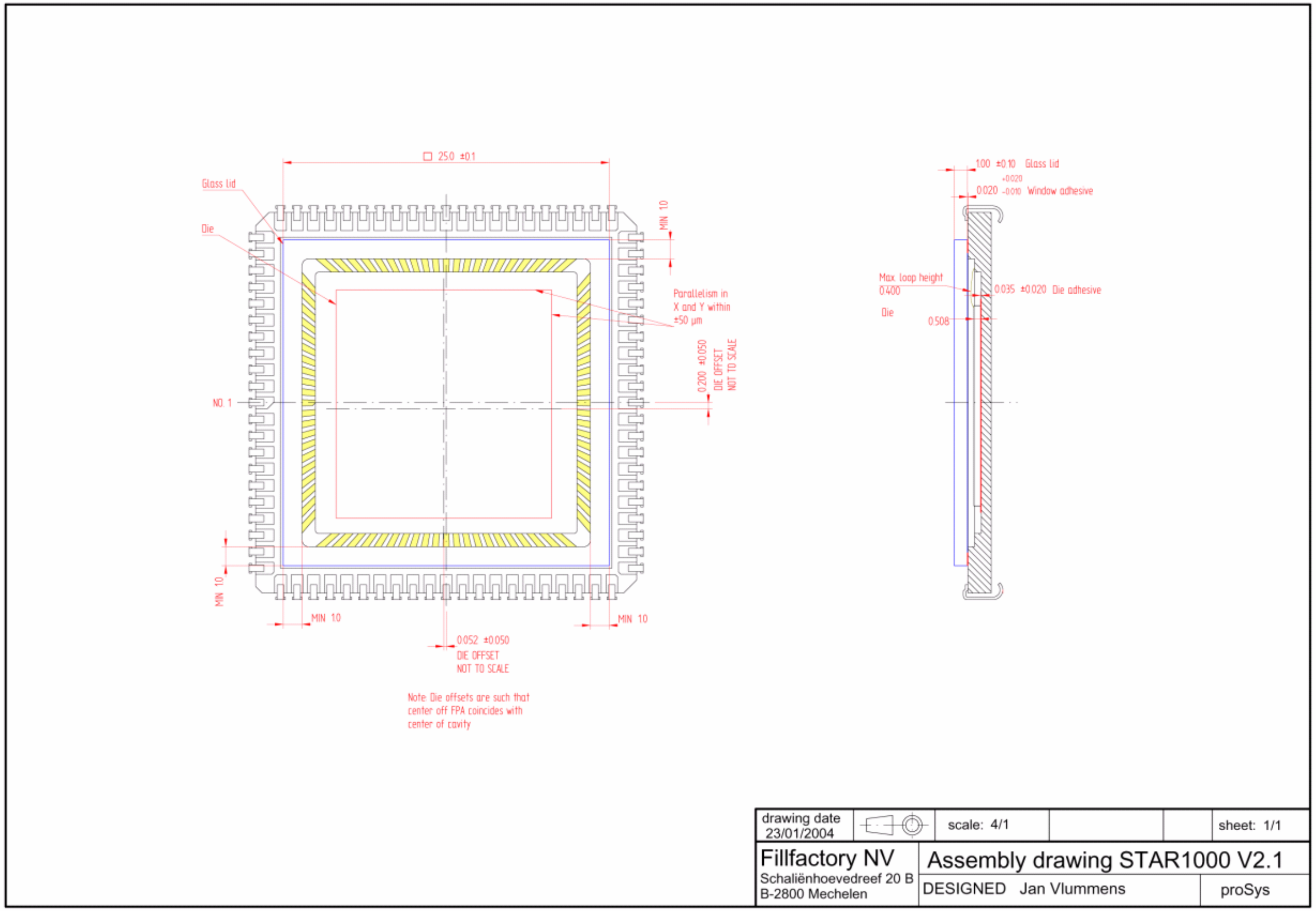
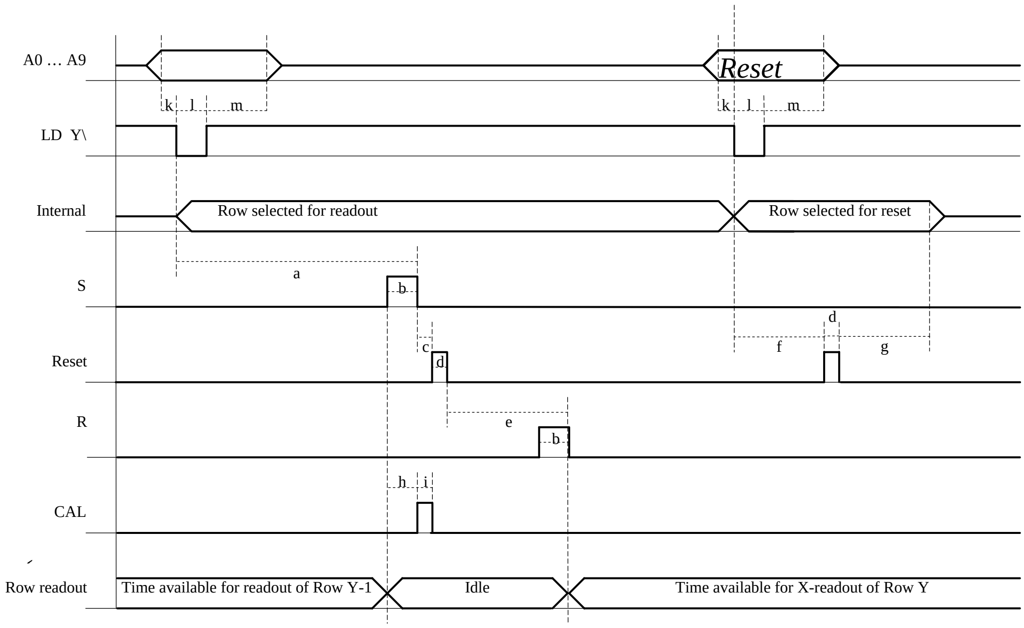


Figure 2b: Geometrical characteristics

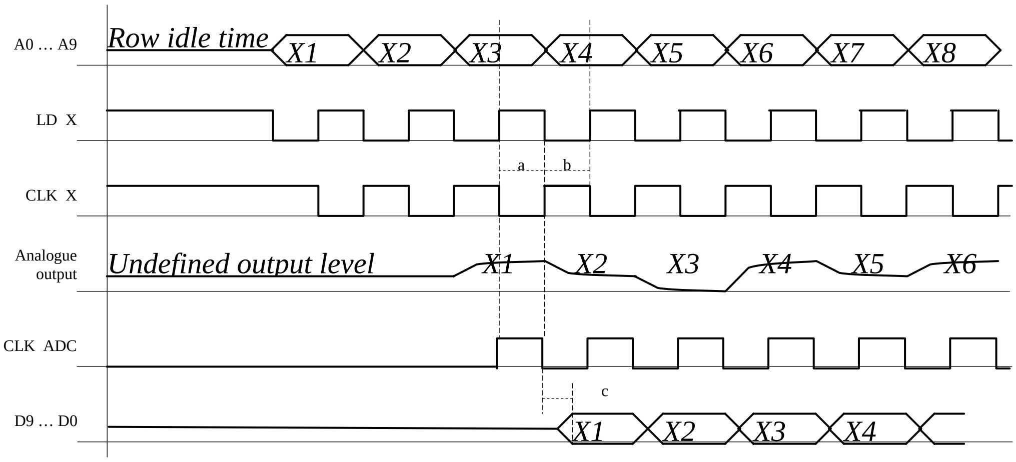
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	A3	**22**	A_IN1	**43**	n.c.	**64**	VDD_ADC_ANA
2	A4	**23**	A_SEL1	**44**	n.c.	**65**	VDD_ADC_DIG
3	A5	**24**	A_SEL0	**45**	n.c.	**66**	GND_ADC_DIG
4	A6	**25**	NBIAS_OAMP	**46**	n.c.	**67**	VDD_DIG_OUT
5	A7	**26**	PBIAS	**47**	n.c.	**68**	D1
6	A8	**27**	G1	**48**	TESTPIXARRAY	**69**	D2
7	A9	**28**	G0	**49**	FOTODIODE	**70**	D3
8	LD_Y	**29**	CAL	**50**	NBIAS_ANA	**71**	D4
9	LD_X	**30**	OUT	**51**	NBIAS_ANA2	**72**	D5
10	VDDA	**31**	BLACKREF	**52**	IN_ADC	**73**	VDDA
11	GNDD	**32**	VDDA	**53**	VDD_ADC_ANA	**74**	GNDA
12	GNDA	**33**	VDDD	**54**	GND_ADC_ANA	**75**	GND_AB
13	CLK_X	**34**	GNDA	**55**	VLOW_ADC	**76**	VREF
14	RESET_DS	**35**	GNDD	**56**	n.c.	**77**	VRES
15	VDDD	**36**	NBIAS_ARRAY	**57**	PBIASDIG2	**78**	D6
16	RESET	**37**	TESTPIX_OUT	**58**	BITINVERT	**79**	D7
17	S	**38**	TESTPIX_RESET	**59**	TRI_ADC	**80**	D8
18	R	**39**	n.c.	**60**	D0	**81**	D9
19	NBIAS_DEC	**40**	n.c.	**61**	CLK	**82**	A0
20	A_IN2	**41**	n.c.	**62**	VHIGH_ADC	**83**	A1
21	A_IN3	**42**	n.c.	**63**	GND_ADC_ANA	**84**	A2

Figure 3a: Pin assignment



Symbol	Min.	Typ.	Description
a	3.6 µs		Delay between selection of a new row and falling edge on S. Minimal value: For maximum speed a new row can already be selected during X-readout of the previous row.
b	0.4 µs		Duration of S and R pulse.
c	0	100 ns	Delay between falling edge of S and rising edge of Reset.
d	200 ns		Minimum duration of Reset pulse.
e	1.6 µs		Delay between falling edge of Reset and falling edge of R.
f	0	100 ns	Minimum delay between falling edge on R and rising edge of Reset.
g		100 ns	Minimum required extension of Y-address after falling edge of reset pulse.
h	100 ns	200 ns	Position of Cal pulse after rising edge of S. The cal pulse must only be given once per frame.
i	100 ns	1 µs	Duration of Cal pulse.
k	10 ns		Address set-up time.
l	20 ns		Load register value.
m	10 ns		Address stable after load.

Figure 3b1: Timing diagram: Reset and line-read-out timing



Symbol	Min	Typ	Description
a	40 ns		Address setup time
b	40 ns		Address valid time
c	0	60 ns	ADC output valid after falling edge of CLK_ADC

Figure 3b2: Timing diagram: Pixel read-out timing

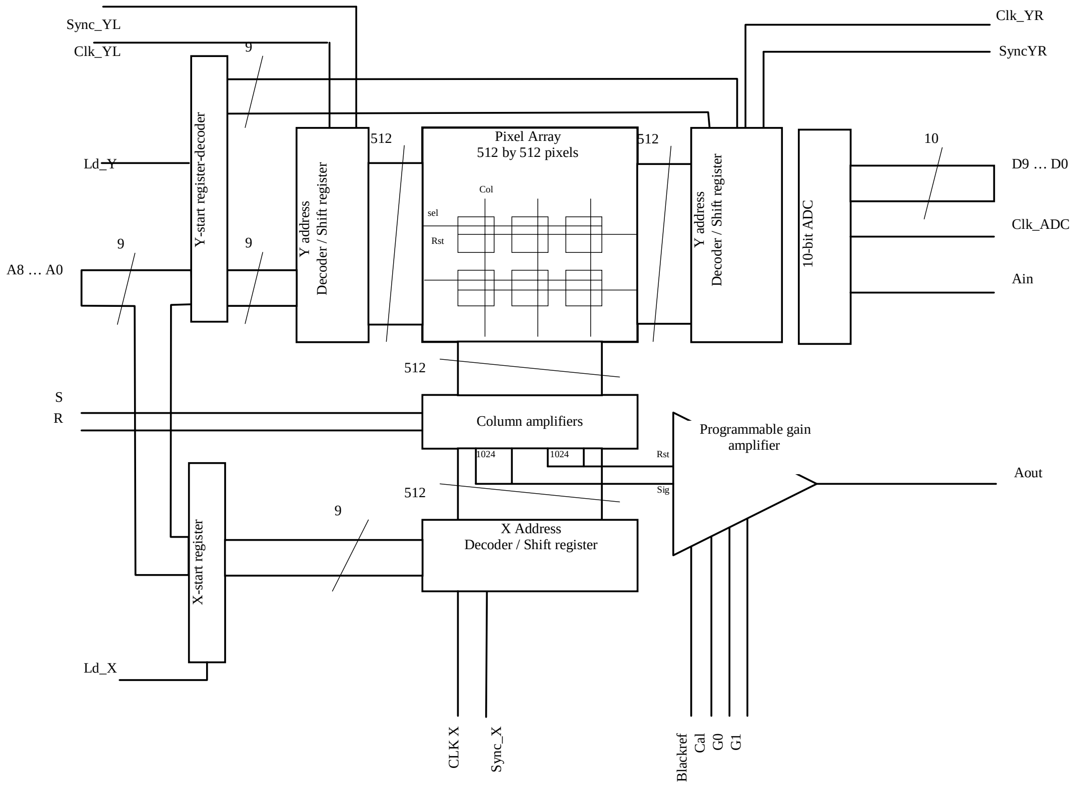


Figure 3c: functional diagram

Table 2: Electrical and electro-optical measurements at reference temperature

The limits in this table set the acceptance criteria for procurement of samples.

	Characteristics	Symbol	Test condition	Limit min	Limit max	Unit
0	Contact test, ESD input structures			No fail	No fail	
13	Total power supply current stand-by			NA	56.0	mA
14	Total PS current, operational			NA	60.1	mA
15	PS current ADC, operational			NA	47.3	mA
16	PS current to image core, operational			NA	13.8	A
23	Offset 0			-100	100	mV
25	Output amplifier gain setting 1			4.02	5.01	
26	Output amplifier gain setting 2			2.07	2.58	
27	Output amplifier gain setting 3			7.57	9.42	
28	ADC ladder network resistance			1078	1271	Ω
29	ADC Differential non linearity			NA	8.36	LSB
30	ADC Integral non linearity			NA	1.82	LSB
33	Saturation voltage output			1.01	NA	V
38	Responsivity narrow band blue			21900	NA	ADU
39	Responsivity narrow band green			21400	NA	ADU
40	Responsivity, narrow band red			19300	NA	ADU
42	Temporal noise, nom. clock frequency			NA	0.75	mV
43	Temporal noise, red. clock frequency			NA	0.97	mV
44	Temporal noise, enhanced clock freq.			NA	1.07	mV
45	Local fixed pattern noise standard deviation, nominal clock frequency			NA	0.22	%Vsat
46	Global fixed pattern noise standard deviation, nominal clock frequency			NA	0.57	%Vsat
47	Local fixed pattern noise standard deviation, reduced clock frequency			NA	0.25	%Vsat
48	Global fixed pattern noise standard deviation, reduced clock frequency			NA	0.52	%Vsat
49	Local fixed pattern noise standard deviation, enhanced clock frequency			NA	0.34	%Vsat
50	Global fixed pattern noise standard deviation, enhanced clock frequency			NA	0.70	%Vsat
51	Number of FPN signal defects			NA	table 1a	
53	Column FPN			NA	0.56	%Vsat
54	Average dark signal			NA	25.3	mV/s
56	Local DSNU standard deviation			NA	0.98	%Vsat
57	Global DSNU standard deviation			NA	1.26	%Vsat
58	Number of DSNU signal defects			NA	table 1a	
60	Local PRNU, standard deviation			NA	1.25	%
61	Global PRNU, standard deviation			NA	5.53	%
62	Number of PRNU defects			NA	table 1a	

Table 3a: Electrical and Electro-optical measurements at high temperature

	Characteristics	Symbol	Test condition	Limit min	Limit max	Unit
13	Total power supply current stand-by			NA	56.6	mA
14	Total PS current, operational			NA	60.6	mA
15	PS current ADC, operational			NA	47.7	mA
16	PS current to image core, operational			NA	13.9	A
28	ADC ladder network resistance			1341	1576	Ω
33	Saturation voltage output			1.05	NA	V
38	Responsivity narrow band blue			22100	NA	ADU
39	Responsivity narrow band green			21500	NA	ADU
40	Responsivity, narrow band red			19600	NA	ADU
44	Temporal noise, enhanced clock freq.			NA	2.37	mV
54	Average dark signal			NA	950	mV/s
56	Local DSNU standard deviation			NA	1.02	%Vsat
57	Global DSNU standard deviation			NA	2.84	%Vsat
58	Number of DSNU signal defects			NA	NA	
60	Local PRNU, standard deviation			NA	1.30	%
61	Global PRNU, standard deviation			NA	4.31	%
62	Number of PRNU defects			NA	table 1a	

Table 3b: Electrical and Electro-optical measurements at low temperature

	Characteristics	Symbol	Test condition	Limit min	Limit max	Unit
13	Total power supply current stand-by			NA	60.0	mA
14	Total PS current, operational			NA	63.9	mA
15	PS current ADC, operational			NA	51.1	mA
16	PS current to image core, operational			NA	13.2	A
28	ADC ladder network resistance			770	1013	Ω
33	Saturation voltage output			1.01	NA	V
38	Responsivity narrow band blue			22100	NA	ADU
39	Responsivity narrow band green			22200	NA	ADU
40	Responsivity, narrow band red			19700	NA	ADU
44	Temporal noise, enhanced clock freq.			NA	0.60	mV
49	Local fixed pattern noise standard deviation, enhanced clock frequency			NA	0.22	%Vsat
50	Global fixed pattern noise standard deviation, enhanced clock frequency			NA	0.41	%Vsat
54	Average dark signal			NA	NA	mV/s
56	Local DSNU standard deviation			NA	NA	%Vsat
57	Global DSNU standard deviation			NA	NA	%Vsat
58	Number of DSNU signal defects			NA	NA	
60	Local PRNU, standard deviation			NA	1.25	%
61	Global PRNU, standard deviation			NA	5.94	%
62	Number of PRNU defects			NA	table 1a	

Table 4a: Parameter drift values for burn in

The min and max limits of table 2 apply

Table 4b: Parameter drift values for radiation testing

Total dose radiation drift values							
No	**Characteristics**	**Symbol**	**Limits**			**Units**	**Remarks**
			Min	**Typ**	**Max**		
54	Average dark signal rise		NA	252	424	e-/s per Krad	At 22 ± 1 °C,
56	Local dark signal non uniformity rise		NA	5	10	e-/s per Krad	At 22 ± 1 °C
57	Global dark signal non uniformity rise		NA	6	14	e-/s per Krad	At 22 ± 1 °C

proton radiation drift values							
No	**Characteristics**	**Symbol**	**Limits**			**Units**	**Remarks**
			Min	**Typ**	**Max**		
54	Average dark signal		NA	35	NA	mV/s	At 22 ± 1 °C, Note [17]
56	Local dark signal non uniformity standard deviation		NA	2.5	NA	%	Note 17
57	Global dark signal non uniformity standard deviation		NA	2.7	NA	%	Note 17

Table 5a: Conditions for high temperature reverse bias burn-in

No	**Characteristics**	**Symbol**	**Test condition**	**Unit**
Not applicable				

Table 5b: Conditions for power burn-in and operating life tests

No	**Characteristics**	**Symbol**	**Test condition**	**Unit**
1	Ambient temperature	Tamb	85C	°C
2	All power supplies	Vdd	+5.5	V
3	Bias conditions		See Figure 5b	
4	X clock frequency		5	MHz

Table 6: Electrical and electro-optical measurements on completion of environmental tests and at intermediate points and on completion of endurance testing

	Characteristics	**Symbol**	**Test condition**	**Limit min**	**Limit max**	**Unit**
0	Contact test, ESD input structures			No fail	No fail	
13	Total power supply current stand-by			NA	56.0	mA
14	Total PS current, operational			NA	60.1	mA
15	PS current ADC, operational			NA	47.3	mA
16	PS current to image core, operational			NA	13.8	A
23	Offset 0			-100	100	mV

[17] The measurement results are based upon a very limited number of samples. Only typical specification values are available.

	Characteristics	Symbol	Test condition	Limit min	Limit max	Unit
25	Output amplifier gain setting 1			4.02	5.01	
26	Output amplifier gain setting 2			2.07	2.58	
27	Output amplifier gain setting 3			7.57	9.42	
28	ADC ladder network resistance			1078	1271	Ω
29	ADC Differential non linearity			NA	8.36	LSB
30	ADC Integral non linearity			NA	1.82	LSB
33	Saturation voltage output			1.01	NA	V
38	Responsivity narrow band blue			21900	NA	ADU
39	Responsivity narrow band green			21400	NA	ADU
40	Responsivity, narrow band red			19300	NA	ADU
42	Temporal noise, nom. clock frequency			NA	0.75	mV
43	Temporal noise, red. clock frequency			NA	0.97	mV
44	Temporal noise, enhanced clock freq.			NA	1.07	mV
45	Local fixed pattern noise standard deviation, nominal clock frequency			NA	0.22	%Vsat
46	Global fixed pattern noise standard deviation, nominal clock frequency			NA	0.57	%Vsat
47	Local fixed pattern noise standard deviation, reduced clock frequency			NA	0.25	%Vsat
48	Global fixed pattern noise standard deviation, reduced clock frequency			NA	0.52	%Vsat
49	Local fixed pattern noise standard deviation, enhanced clock frequency			NA	0.34	%Vsat
50	Global fixed pattern noise standard deviation, enhanced clock frequency			NA	0.70	%Vsat
51	Number of FPN signal defects			NA	table 1a	
53	Column FPN			NA	0.56	%Vsat
54	Average dark signal			NA	25.3	mV/s
56	Local DSNU standard deviation			NA	0.98	%Vsat
57	Global DSNU standard deviation			NA	1.26	%Vsat
58	Number of DSNU signal defects			NA	table 1a	
60	Local PRNU, standard deviation			NA	1.25	%
61	Global PRNU, standard deviation			NA	5.53	%
62	Number of PRNU defects			NA	table 1a	

Table 7a: Electrical and electro-optical measurements during and on completion of total-dose irradiation testing

	Characteristics	Symbol	Test condition	Limit min	Limit max	Unit
13	Total power supply current stand-by			NA	56.0	mA
14	Total PS current, operational			NA	60.1	mA
45	Local fixed pattern noise standard deviation, nominal clock frequency			NA	0.22	%Vsat
46	Global fixed pattern noise standard deviation, nominal clock frequency			NA	0.57	%Vsat
51	Number of FPN signal defects			NA	table 1a	
54	Average dark signal			NA	Table 4	e-/s
56	Local DSNU standard deviation			NA	Table 4	e-
57	Global DSNU standard deviation			NA	Table 4	e-
58	Number of DSNU signal defects			NA	Table 4	

Table 7b: Electrical and electro-optical measurements during and on completion of proton irradiation testing

Proton irradiation testing is performed with 2.4E11 protons at an energy of 60 Mev.

	Characteristics	Symbol	Test condition	Limit min	Limit max	Unit
13	Total power supply current stand-by			NA	56.0	mA
14	Total PS current, operational			NA	60.1	mA
45	Local fixed pattern noise standard deviation, nominal clock frequency			NA	0.22	%Vsat
46	Global fixed pattern noise standard deviation, nominal clock frequency			NA	0.57	%Vsat
51	Number of FPN signal defects			NA	table 1a	
54	Average dark signal			NA	table 4	
56	Local DSNU standard deviation			NA	Table 4	%
57	Global DSNU standard deviation			NA	table 4	%

Table 7c: Electrical and electro-optical measurements during and on completion of heavy ion irradiation testing

During heavy ion testing no specific tests or measurement are executed. Instead the image sensors are operated at nominal speed and power supply current is monitored.

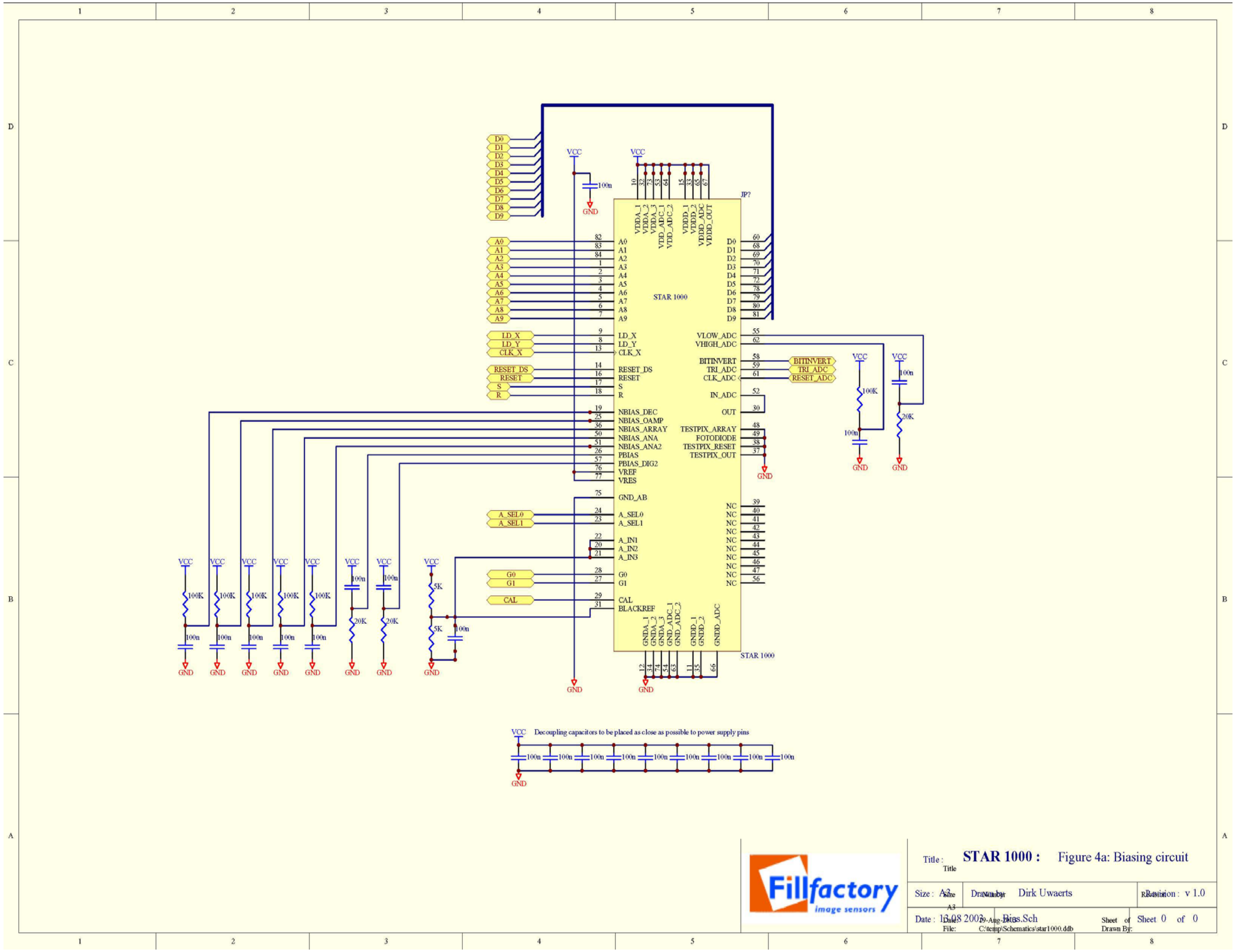
Heavy ion testing is performed with a total dose of 10E7 particles with an effective LET of 127.8 MeV/mg/cm2

	Characteristics	Symbol	Test condition	Limit min	Limit max	Unit
13	Total power supply current stand-by			NA	56.0	mA
14	Total PS current, operational			NA	60.1	mA

Not applicable

Figure 1: Parameter derating information

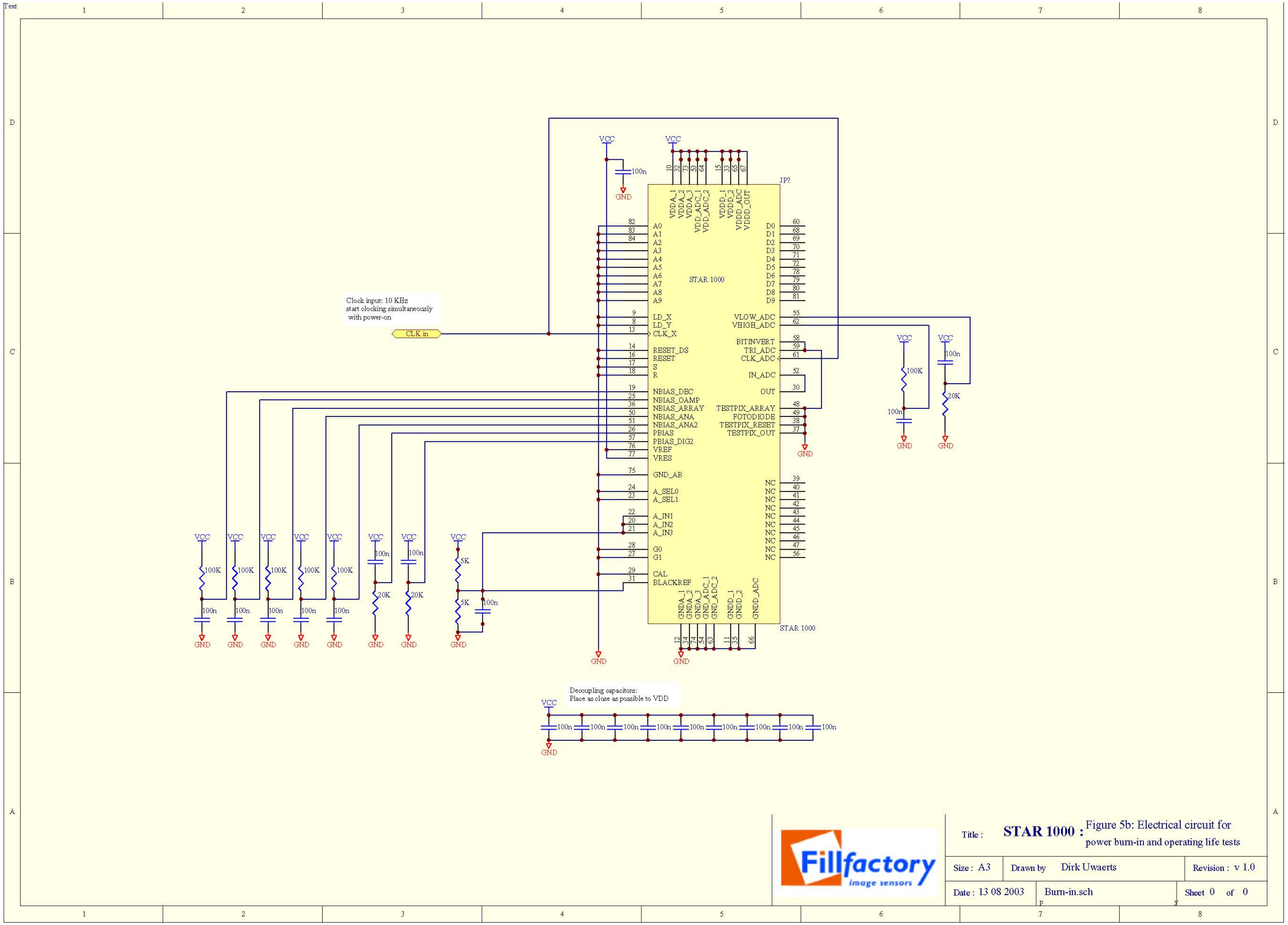
Figure 4: Circuits and diagrams for electrical and electro-optical measurements



STAR 1000 : Figure 4a: Biasing circuit
Decoupling capacitors to be placed as close as possible to power supply pins
Dirk Uwaerts
v 1.0
Bias.Sch

Not applicable

Figure 5a: Electrical circuit for high temperature reverse bias burn-in



STAR 1000
Clock input: 10 KHz
start clocking simultaneously
with power-on
CLK in
Decoupling capacitors:
Place as close as possible to VDD
VCC
GND
Title : STAR 1000 : Figure 5b: Electrical circuit for power burn-in and operating life tests
Size : A3
Drawn by Dirk Uwaerts
Revision : v 1.0
Date : 13 08 2003
Burn-in.sch
Sheet 0 of 0

The bias circuit for total dose radiation testing is identical to figure 5b

Figure 6: Biasing circuit for total dose radiation testing

Appendix A: Pin description

This appendix contains a pin description for the STAR1000 CMOS image sensor

Image core connection

Name	Type	Description
NBIAS_ARRAY	Analogue input	Connect with 1 MEG to Vdd and decouple to ground by 100 nF capacitor
PBIAS	Analogue input	Connect with 20K to ground and decouple to Vdd by 100 nF capacitor for 12.5 MHz pixel rate. (Lower resistor values yield higher maximal pixel rates at the cost of extra power dissipation)
GND_AB	Analogue input	Anti-blooming drain control voltage: Default: connect to ground. The anti-blooming is operational but not maximal. Apply 1 V DC for improved anti-blooming.
S	Digital input	Control signal for column amplifier. Apply pulse pattern – see sensor timing diagram.
R	Digital input	Control signal for column amplifier. Apply pulse pattern – see sensor timing diagram.
RESET	Digital input	Resets row indicated by Y-address. High active (1= reset row). Apply pulse pattern – see sensor timing diagram.
RESET_DS	Digital input	Resets row indicated by Y-address. High active (1= reset row). Apply pulse pattern – see sensor timing diagram. RESET_DS can be used for dual-slope integration (contact FillFactory for details). Connect to GND for normal operation.

Analogue inputs

Name	Type	Description
BLACKREF	Analogue input	Control voltage for output signal offset level. Buffered on-chip, the reference level can be generated by a 100K resistive divider. Connect to 2 V DC for use with on-chip ADC.
NBIAS_OAMP	Analogue input	Output amplifier speed/power control. Connect with 100K to VDD and decouple with 100 nF to GND for 12.5 MHz output rate. (lower resistor values yield higher maximal pixel rates at the cost of extra power dissipation).
NBIAS_DEC	Analogue input	Address decoder reference current. Connect with 100K to VDD and decouple with 100 nF to GND.
OUT	Analogue input	Analog output signal. To be connected to the analog input of the ADC.
G0	Digital input	Select output amplifier gain value: G0 = LSB; G1 = MSB

G1		00 = unity gain; 01 = x2; 10= x4; 11=x8.
CAL	Digital input	Initialize output amplifier. Output amplifier will output BLACKREF in unity gain mode when CAL is high (1). Apply pulse pattern (one pulse per frame) – see sensor timing diagram.
A-IN1 **A-IN2** **A-IN3**	Analogue input	Additional analog inputs. For proper conversion with on-chip ADC the input signal must lie within the output signal range of the image sensor. (approximately +2V to +4V).
A_SEL0 **A-SEL1**	Digital input	Selection of analog channel: 00 selects image sensor.

Digital inputs

Name	Type	Description
A0 **A1** **A2** **A3** **A4** **A5** **A6** **A7** **A8** **A9**	Digital input	Address inputs for row and column addressing. A9=LSB, A0=MSB.
LD_X	Digital input	Latch address (A0…A9) to X register (0 = track, 1 = hold).
LD_Y	Digital input	Latch address (A0…A9) to Y register (0 = track, 1 = hold).
CLK_X	Digital input	Clock X register (output valid & stable when CLK_X is high).

Analogue inputs

Name	Type	Description
IN_ADC	Analogue input	Input, connect to output of image sensor. Input range is between 2V and 4V: (VLOW_ADC & VHIGH_ADC).
VLOW_ADC **VHIGH_ADC**	Analogue input Analogue input	Low- and high reference voltages of ADC. Nominal input range is between 2V and 4V, to be fine-tuned when working samples are available. The resistance between VLOW_ADC and VHIGH_ADC is about 1.5 K. The required voltage settings on VLOW_ADC and VHIGH_ADC can be approximated by tying VLOW_ADC with 2 K to GND and VHIGH_ADC with 1 K to VDD.
PBIASDIG2	Analogue input	Connect with 20K to GND and decouple to VDD.
NBIASANA	Analogue input	Connect with 100K to VDD and decouple to GND.
NBIASANA2	Analogue input	Connect with 100K to VDD and decouple to GND.
D0	Digital output	ADC output bits.

D1		D0 = LSB, D9=MSB.
D2		
D3		
D4		
D5		
D6		
D7		
D8		
D9		
CLK	Digital input	ADC clock. ADC converts on falling edge.
TRI_ADC	Digital input	Tri-state control of digital ADC outputs. 1 = tri-state; 0 = output.
BITINVERT	Digital input	0 = invert output bits. 1 = no inversion of output bits.

Power and ground terminals

Name	**Type**	**Description**
VDD_ANA	Power	Power supply pixel array: 5 V DC. Connected internally to VDDA.
VRES	Power	Reset level for RESET: 5V.
VREF	Power	Reset level for RESET_DS: 5V DC. Apply different voltage for extended dynamic range.
GNDA	Ground	Analogue ground of imager (appears 2 times).
VDDA	Power	Analogue power supply of imager: 5 V DC (appears 2 times).
GNDD	Ground	Digital ground of imager (appears 4 times).
VDDD	Power	Digital power of imager: 5 V DC (appears 4 times).
GND_ADC_ANA	Ground	Analogue ground of ADC.
VDD_ADC_ANA	Power	Analogue power supply of ADC: 5 V DC.
GND_ADC_DIG	Ground	Digital ground of ADC.
VDD_ADC_DIG	Power	Digital power of ADC: 5 V DC.
VDD_DIG_OUT	Power	Power supply of ADC digital output. Connect to 5V for or normal operation. Can be brought to lower voltage when image sensor must be interfaced to low voltage periphery.

Test signals

Name	**Type**	**Description**
TESTPIX_OUT	Test structure	Output of single test pixel.
TESTPIX_RESET	Test structure	Rest input of single test pixel.

TESTPIXARRAY	Test structure	Array of 20 x 35 pixels where all photodiodes are connected in parallel.
FOTODIODE	Test structure	Plain photo diode. Area = 20 x 35 pixels.

Appendix B: User Manual

Sensor description

The STAR1000 is a CMOS image sensor with 1024 by 1024 pixels on a 15-µm pitch. It features on-chip Fixed Pattern Noise (FPN) correction, a programmable gain amplifier and a 10-bit Analog to Digital Converter (ADC).

All circuits are designed using the radiation tolerant design rules for CMOS image sensors to allow a high tolerance against total dose effects.

Registers that can be directly accessed by the external controller contain the X- and Y-addresses of the pixels to be read. This architecture provides flexible operation and allows different operation modes like (multiple) windowing, sub sampling, etc.

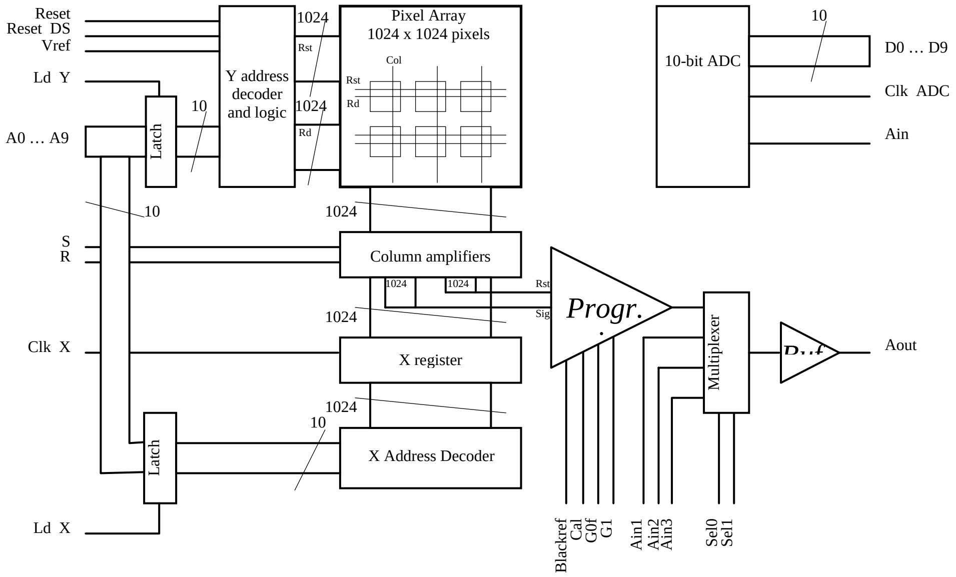


Figure 1: Image sensor outline diagram

The image sensor contains five sections: the pixel array, the X-and Y addressing logic, the column amplifiers, the output amplifier and the ADC. Figure 1 shows an outline diagram of the sensor, including an indication of the main control signals. The following paragraphs explain in more detail the function and operation of the different imager parts.

The pixel array

The pixel array contains 1024 by 1024 active pixels at 15µm pitch. Each pixel contains one photo diode and three transistors (Figure 2).

The photo diode is always in reverse bias. At the beginning of the integration cycle a pulse is applied to the reset line (gate of T1) bringing the cathode of D1 to the reset voltage level. During the integration period photon-generated electrons accumulate

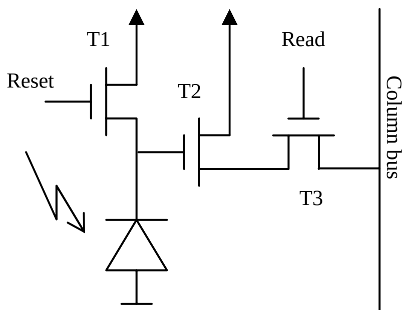


Figure 2: Active pixel electrical diagram

on the diode capacitance, reducing the voltage on the gate of T2. The real illumination-dependent signal is the different between the reset level and the output level after integration. This difference is made in the column amplifiers. T2 acts as a source follower and T3 allows connection of the pixel signal (reset level and output level) to the vertical output bus.

The reset-lines and the read-lines of the pixels in a row are connected together to the Y-decoder logic; the outputs of the pixels in a column are connected together to a column amplifier.

Addressing logic

The addressing logic allows direct addressing of rows and columns. Instead of the one-hot shift registers that are often used, address decoders are implemented. One can select a line by presenting the required address to the address input of the device and latching it to the Y-decoder logic. Presenting the X-address to the device address input and latching it to the X-address decoder can select a column.

A typical line read out sequence will first select a line by applying the Y-address to the Y-decoder. Activation of the “Select” input on the Y-logic will connect the pixel outputs of the selected line to the column amplifiers. The individual column amplifier outputs can be connected to the output amplifier by applying the respective X-addresses to the X address decoder. Applying the appropriate Y-address to the Y-decoder and activating the “Reset” input reset a line. The integration time of a row is the time between the last reset of this row and time when it is selected for read-out.

The Y-decoder logic has two different reset inputs: “Reset1” and “Reset2”. Activation of “Reset1” will reset the pixel to the Vdd level; activation of “Reset2” will reset the pixel to the voltage level on the “DS_ref” input. This feature allows the application of the so-called dual slope integration. If dual slope integration is not needed “DS_ref” can be tied to Vdd and “Reset2” must never be activated.

The column amplifiers

All outputs from the pixels in a column are connected in parallel to a column amplifier. This amplifier samples the output voltage and the reset level of the pixel whose row is selected at that moment and presents these voltage levels to the output amplifier. As a result the pixels are always reset immediately after read-out as part of the sample procedure and the maximum integration time of a pixel is the time between two read cycles.

The output amplifier and analog multiplexer

The output amplifier combines subtraction of pixel signal level from reset level with a programmable gain amplifier. Since the amplifier is AC coupled it also contains a provision to maintain and restore the proper DC level.

An analogue signal multiplexer feeds the pixel signal to the final unity gain buffer to provide the required drive capability. Apart from the pixel signal also three other external analogue signals can be fed to the output buffer. All these signals can be digitalised by the on-chip ADC if the output of this buffer is externally connected to the input of the ADC.

The purpose of the additional analogue inputs is to allow a possibility to process other analogue signals through the image sensors signal path. These signals can thus be converted by the ADC and processed by the image controller FPGA. The additional analogue inputs are intended for low frequency or DC signals and have a reduced bandwidth, compared with the image signal path.

AD Converter

The image sensor has a 10-bit ADC that is electrically separated from the rest of the image sensor circuits and can be powered down if an external ADC is used. The conversion takes place at the falling edge of the clock and the output pins can be disabled to allow operation of the device in a bus structure.

This design is an upgrade of an earlier rad-tolerant design, with a shorter delay time.

Timing and control signals

The pixels addressing is done by direct addressing of rows and columns. This approach has the advantage of full flexibility when accessing the pixel array: multiple windowing and sub-sampled read-out are possible by proper programming.

The following paragraphs clarify the timing for row- and column readout.

Row selection and reset timing

Figure 3 shows the timing of the line sequence control signals. The timing constraints are given in table 2.

The address, presented at the address IO pins is latched in with the LD-Y pulse. After latching the external controller can already produce a new address.

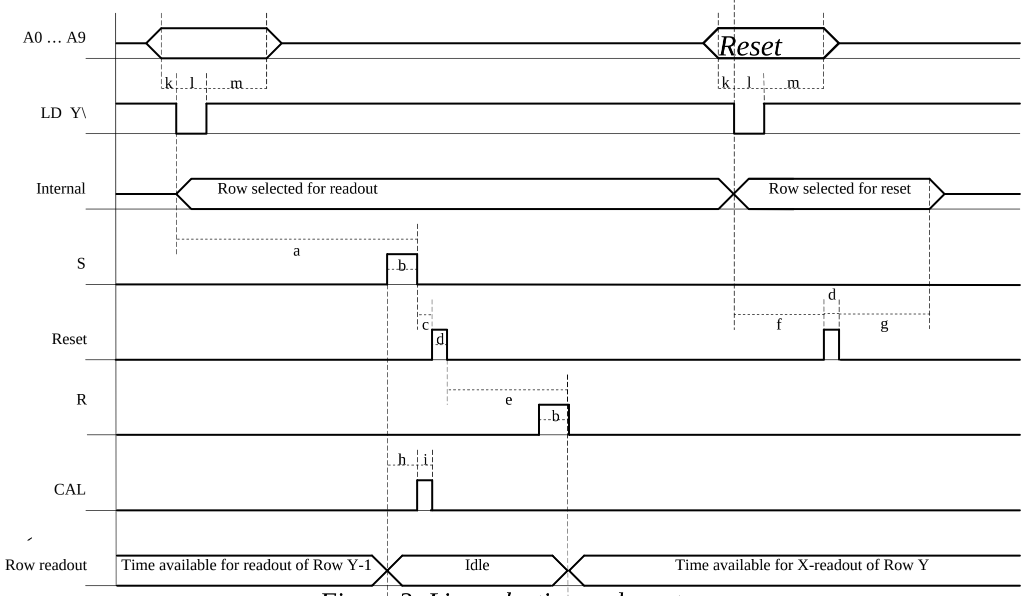


Figure 3: Line selection and reset sequence

Latching in a Y-address selects the addressed row and connects the pixel outputs of that row to the column amplifiers. Through the sequence of the S and R pulse and the Reset pulse in-between the pixel output signal and reset level are sampled and produced at the output of the column amplifier.

At this time horizontal read-out of the selected row can start and another row can be reset to effectuate reduced integration time.

Table 2 shows the timing constraints for the horizontal or line-select timing. The given data are based upon the results of simulations. These values will be fine-tuned when real devices are operational.

Table 1: Timing constraints of line sequence

Symbol	Min.	Typ.	Description
a	3.6 µs		Delay between selection of a new row and falling edge on S. Minimal value: For maximum speed a new row can already be selected during X-readout of the previous row.
b	0.4 µs		Duration of S and R pulse.
c	0	100 ns	Delay between falling edge of S and rising edge of Reset.
d	200 ns		Minimum duration of Reset pulse.
e	1.6 µs		Delay between falling edge of Reset and falling edge of R.
f	0	100 ns	Minimum delay between falling edge on R and rising edge of Reset.
g		100 ns	Minimum required extension of Y-address after falling edge of reset pulse.
h	100 ns	200 ns	Position of Cal pulse after rising edge of S. The cal pulse must only be given once per frame.
i	100 ns	1 µs	Duration of Cal pulse.
k	10 ns		Address set-up time.
l	20 ns		Load register value.
m	10 ns		Address stable after load.

Pixel read-out timing

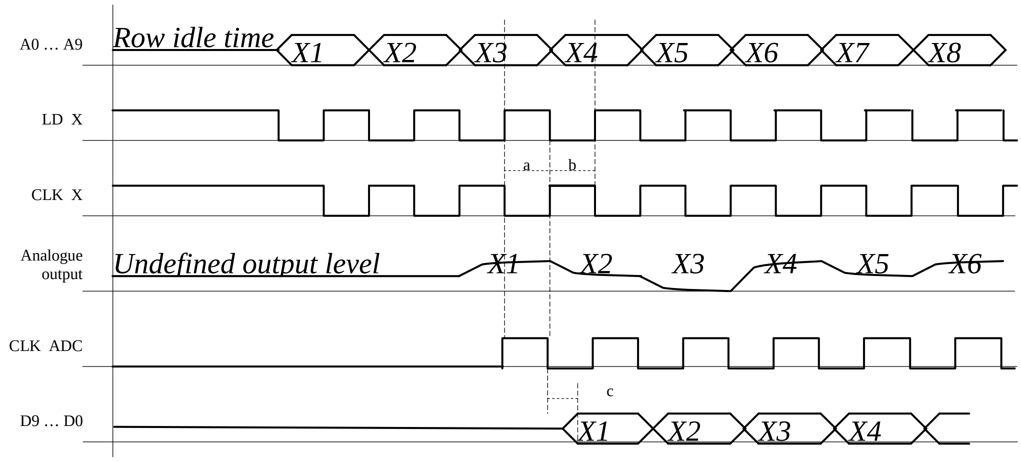


Figure 4 shows the timing of the pixel readout sequence. The external digital controller presents a column address that is latched in by the rising edge of the LD_X pulse. After decoding the X-address the column selection is clocked in the X-register by CLK-X. The output amplifier uses the same pulse to subtract the pixel output level from the pixel-reset level and to sample the signal. This causes a pipeline effect such that the analogue output of the first pixel is effectively present at the device output terminal at the third rising edge of the X-CLK signal.

The ADC conversion starts at the falling edge of the CLK-ADC signal and produces a valid digital output 20ns after this edge. The timing of these signals is given in table 3.

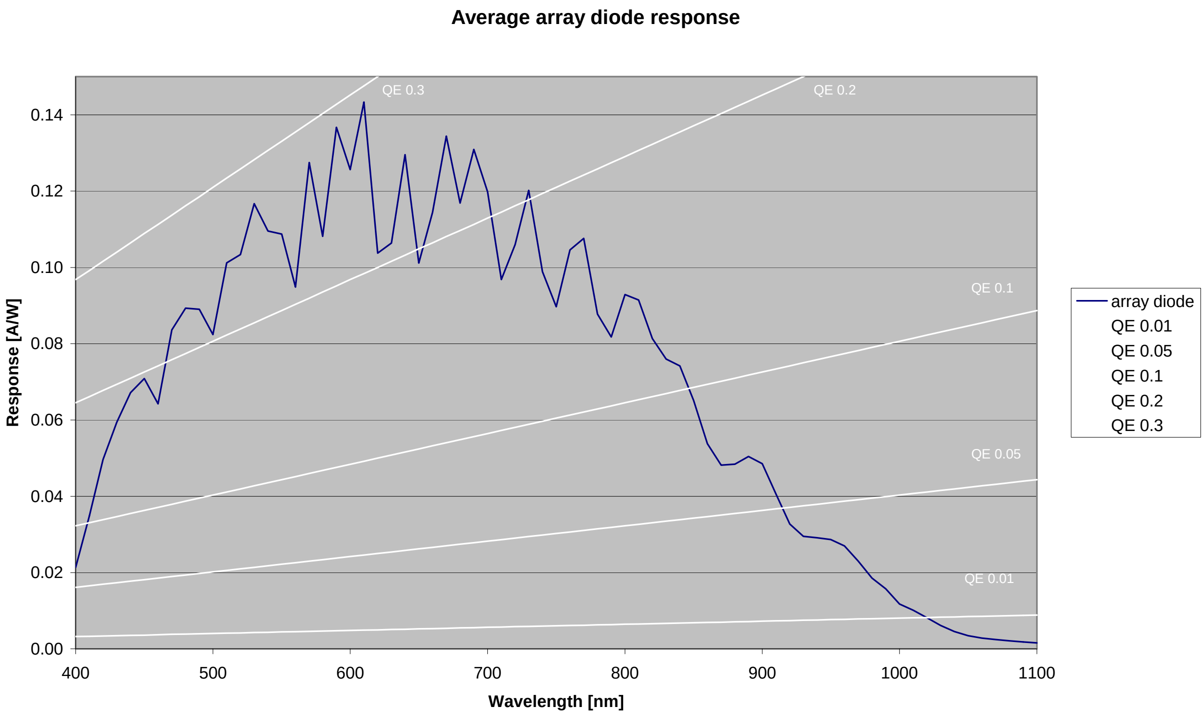
Table 2:Timing constraints of column read out

Symbol	Min	Typ	Description
a	40 ns		Address setup time
b	40 ns		Address valid time
c	0	60 ns	ADC output valid after falling edge of CLK_ADC

Figure 4: Column selection and read-out sequence

Appendix C: Typical spectral response data

The following figure shows a typical spectral response curve. The fringes in the curve result from optical interference in the top dielectric layers.

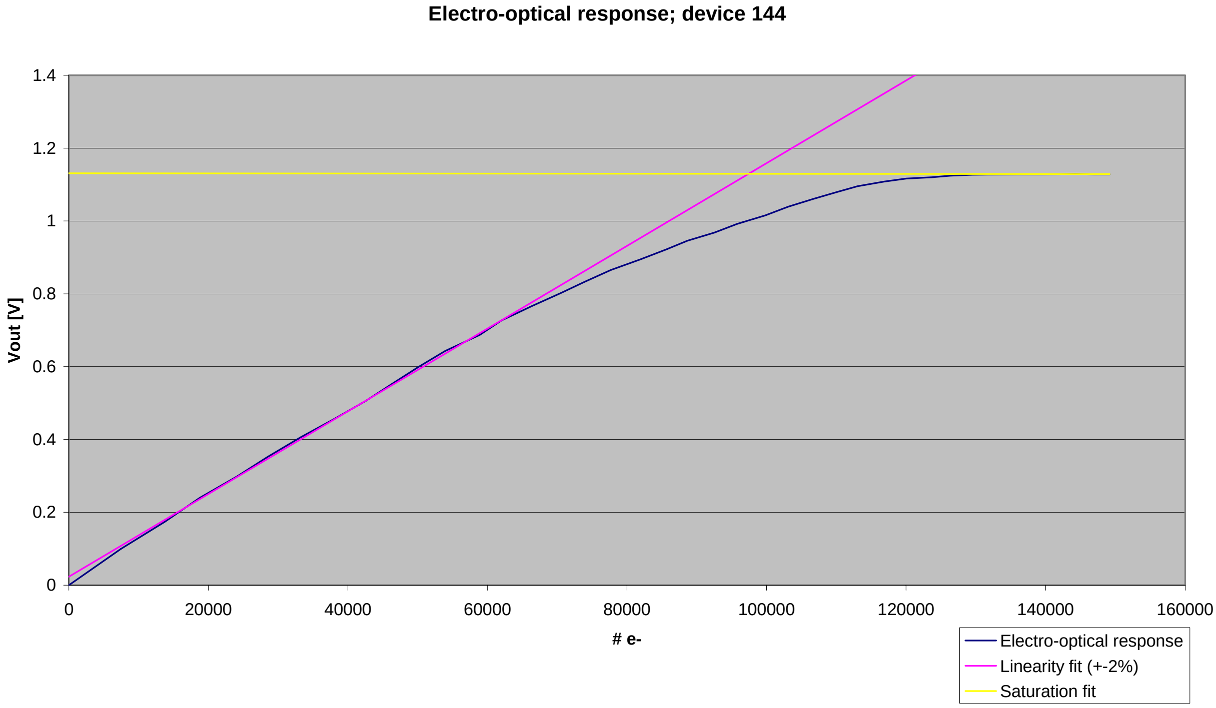


Typical spectral response curve, tabular data:

Wl [nm]	Pixel response [A/w]	Wl [nm]	Pixel response [A/w]
400	2.13E-02	760	1.05E-01
410	3.49E-02	770	1.08E-01
420	4.96E-02	780	8.77E-02
430	5.94E-02	790	8.17E-02
440	6.72E-02	800	9.29E-02
450	7.08E-02	810	9.14E-02
460	6.42E-02	820	8.13E-02
470	8.36E-02	830	7.60E-02
480	8.94E-02	840	7.42E-02
490	8.90E-02	850	6.51E-02
500	8.24E-02	860	5.38E-02
510	1.01E-01	870	4.82E-02
520	1.03E-01	880	4.84E-02
530	1.17E-01	890	5.04E-02
540	1.10E-01	900	4.86E-02
550	1.09E-01	910	4.06E-02
560	9.48E-02	920	3.28E-02
570	1.27E-01	930	2.95E-02
580	1.08E-01	940	2.91E-02
590	1.37E-01	950	2.87E-02
600	1.26E-01	960	2.70E-02
610	1.43E-01	970	2.30E-02
620	1.04E-01	980	1.85E-02
630	1.06E-01	990	1.57E-02
640	1.30E-01	1000	1.18E-02
650	1.01E-01	1010	1.01E-02
660	1.14E-01	1020	8.18E-03
670	1.34E-01	1030	6.16E-03
680	1.17E-01	1040	4.56E-03
690	1.31E-01	1050	3.44E-03
700	1.20E-01	1060	2.81E-03
710	9.68E-02	1070	2.44E-03
720	1.06E-01	1080	2.11E-03
730	1.20E-01	1090	1.78E-03
740	9.89E-02	1100	1.56E-03
750	8.97E-02		

Appendix D: Typical electro-optical response data

The following figure shows a typical electro-optical response curve. T
he saturation fit and +- 2% linearity fit are plotted on the curve.

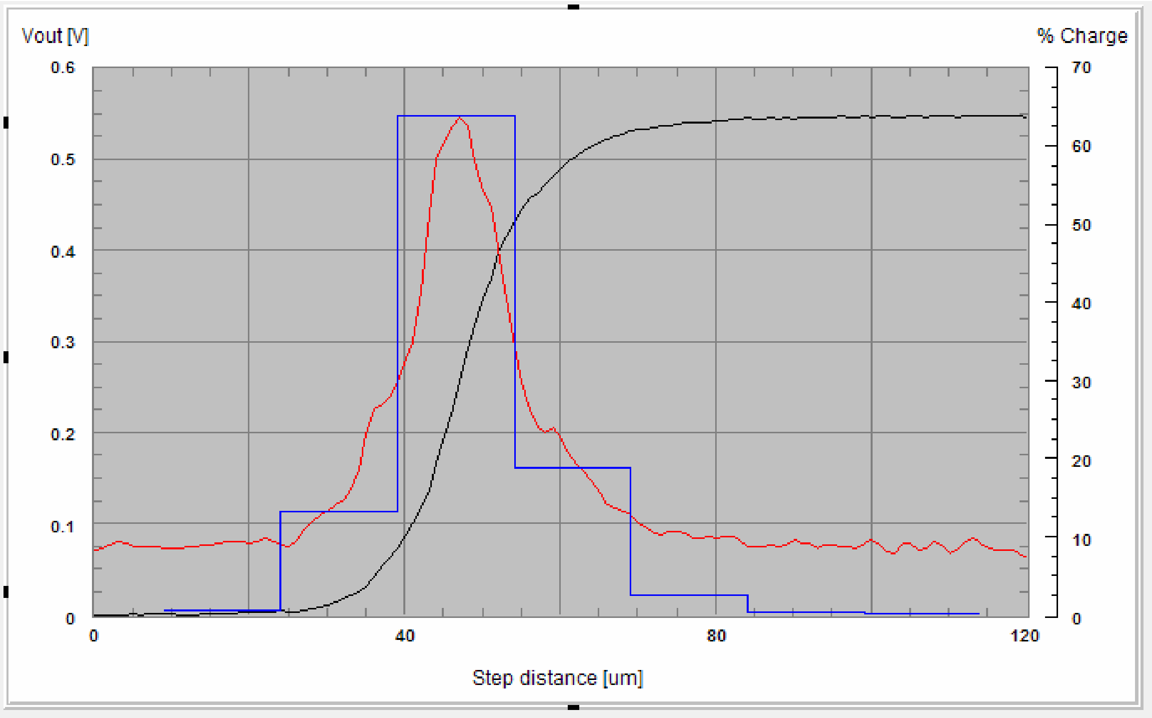


Typical electro-optical response, tabular data.

#e-	Vout
149160.3	1.1284
146989.9	1.1284
144244.6	1.1292
142051.4	1.1288
139290.3	1.1284
136141.2	1.128
133382	1.1276
129498.8	1.1268
126384.4	1.1244
123669.8	1.1196
120015.4	1.116
116854.8	1.1076
113027	1.0952
110014.8	1.0792
106711.6	1.0604
103084	1.0392
99854.21	1.0152
95749.88	0.9916
92540	0.968
88642.83	0.9452
85632.39	0.9216
81956.08	0.8944
77665.74	0.8652
73929.28	0.8328
70535.23	0.802
66398.8	0.7664
62040.82	0.7268
58868.76	0.6868
53964.82	0.6428
50125.61	0.5988
46290.97	0.552
42503.33	0.5052
38050.93	0.4564
33193.84	0.4056
28500.74	0.352
24107.02	0.2984
18773.12	0.2396
13767.18	0.1744
7459.663	0.0996
0	0

Appendix E: Typical pixel profile data

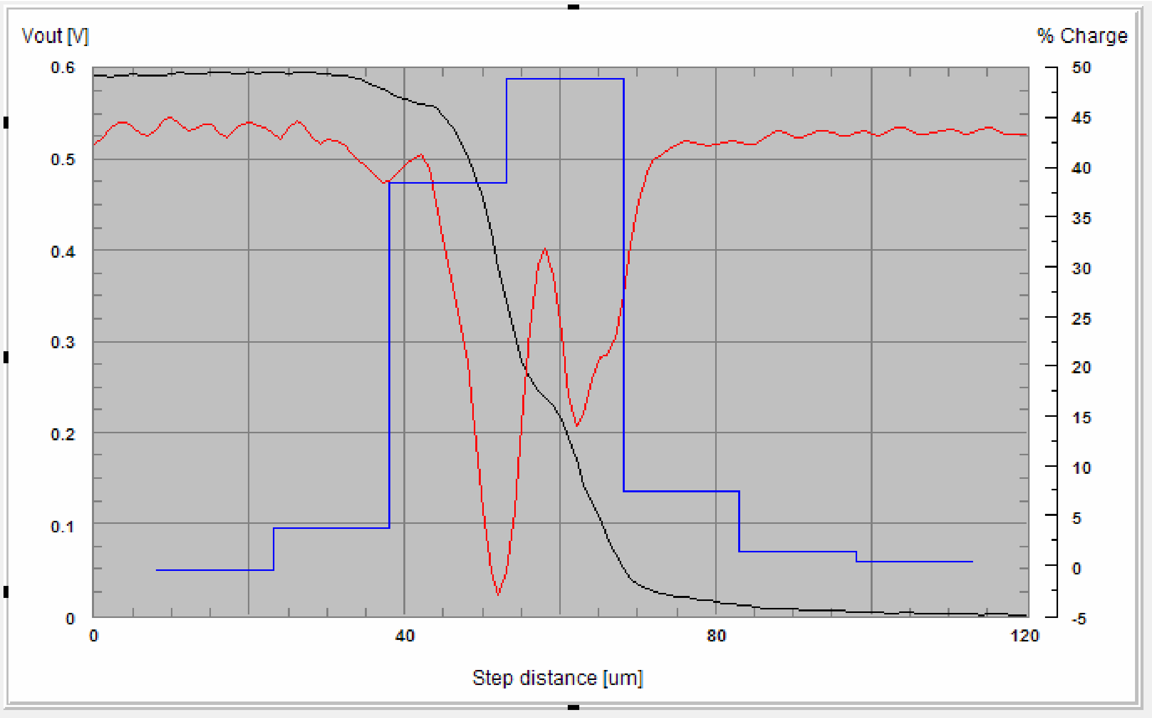
Vertical pixel profile measurement data at 600 nm



Vertical pixel profile measurement data at 600 nm, tabular data.

Distance [µm]	Pixel Vout [V]	Distance [µm]	Pixel Vout [V]	Distance [µm]	Pixel Vout [V]
0	0.5932	40	0.5666	80	0.0144
1	0.5918	41	0.5636	81	0.0138
2	0.5914	42	0.5614	82	0.0126
3	0.5924	43	0.559	83	0.0118
4	0.5926	44	0.5574	84	0.0108
5	0.5936	45	0.5472	85	0.0092
6	0.593	46	0.5362	86	0.0082
7	0.5928	47	0.5226	87	0.0074
8	0.5918	48	0.5048	88	0.0076
9	0.5926	49	0.484	89	0.0072
10	0.5936	50	0.4582	90	0.0072
11	0.5956	51	0.4208	91	0.0058
12	0.5944	52	0.3814	92	0.0054
13	0.5946	53	0.3452	93	0.0052
14	0.5944	54	0.3072	94	0.0052
15	0.5958	55	0.2792	95	0.005
16	0.5956	56	0.2608	96	0.0048
17	0.5954	57	0.2466	97	0.0038
18	0.5936	58	0.2388	98	0.0036
19	0.5946	59	0.2304	99	0.0036
20	0.5962	60	0.215	100	0.0036
21	0.595	61	0.196	101	0.003
22	0.5966	62	0.172	102	0.0022
23	0.5962	63	0.1444	103	0.0024
24	0.5954	64	0.1232	104	0.003
25	0.5938	65	0.1062	105	0.0028
26	0.5954	66	0.0864	106	0.0026
27	0.5972	67	0.0674	107	0.002
28	0.5958	68	0.0512	108	0.002
29	0.5948	69	0.0396	109	0.0014
30	0.5942	70	0.0328	110	0.002
31	0.5924	71	0.0286	111	0.0016
32	0.5928	72	0.0258	112	0.0018
33	0.5904	73	0.0242	113	0.001
34	0.5884	74	0.0216	114	0.0008
35	0.5856	75	0.0206	115	0.0012
36	0.5824	76	0.0196	116	0.0014
37	0.5784	77	0.0186	117	0.0014
38	0.5734	78	0.0174	118	0.0006
39	0.569	79	0.0164	119	0.0002

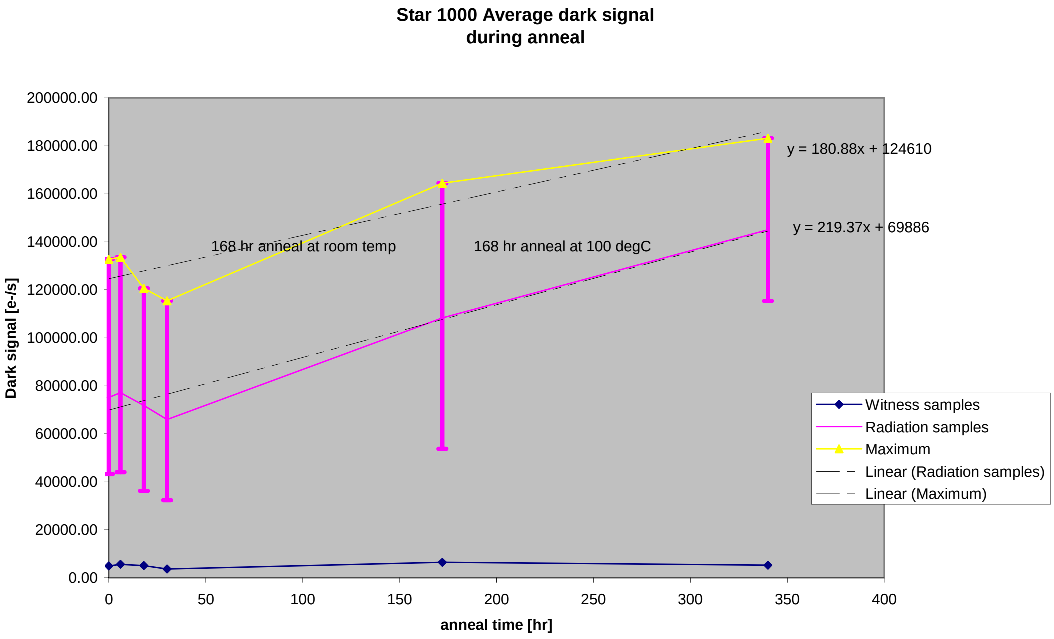
Horizontal pixel profile measurement data at 600 nm



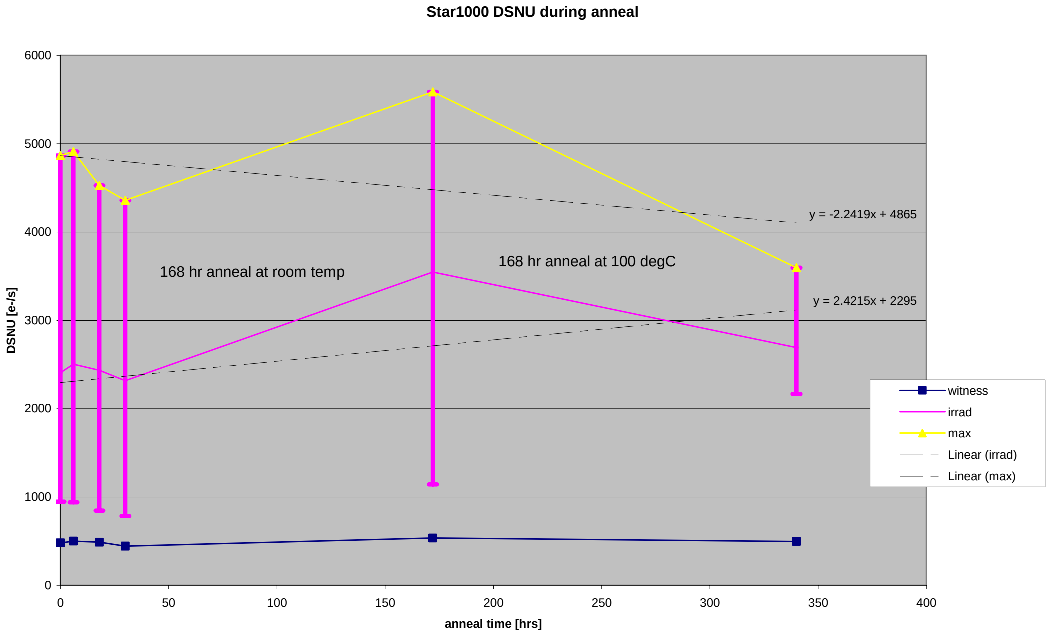
Horizontal pixel profile measurement data at 600 nm, tabular data.

Distance [µm]	Pixel Vout [V]	Distance [µm]	Pixel Vout [V]	Distance [µm]	Pixel Vout [V]
0	0.5932	40	0.5666	80	0.0144
1	0.5918	41	0.5636	81	0.0138
2	0.5914	42	0.5614	82	0.0126
3	0.5924	43	0.559	83	0.0118
4	0.5926	44	0.5574	84	0.0108
5	0.5936	45	0.5472	85	0.0092
6	0.593	46	0.5362	86	0.0082
7	0.5928	47	0.5226	87	0.0074
8	0.5918	48	0.5048	88	0.0076
9	0.5926	49	0.484	89	0.0072
10	0.5936	50	0.4582	90	0.0072
11	0.5956	51	0.4208	91	0.0058
12	0.5944	52	0.3814	92	0.0054
13	0.5946	53	0.3452	93	0.0052
14	0.5944	54	0.3072	94	0.0052
15	0.5958	55	0.2792	95	0.005
16	0.5956	56	0.2608	96	0.0048
17	0.5954	57	0.2466	97	0.0038
18	0.5936	58	0.2388	98	0.0036
19	0.5946	59	0.2304	99	0.0036
20	0.5962	60	0.215	100	0.0036
21	0.595	61	0.196	101	0.003
22	0.5966	62	0.172	102	0.0022
23	0.5962	63	0.1444	103	0.0024
24	0.5954	64	0.1232	104	0.003
25	0.5938	65	0.1062	105	0.0028
26	0.5954	66	0.0864	106	0.0026
27	0.5972	67	0.0674	107	0.002
28	0.5958	68	0.0512	108	0.002
29	0.5948	69	0.0396	109	0.0014
30	0.5942	70	0.0328	110	0.002
31	0.5924	71	0.0286	111	0.0016
32	0.5928	72	0.0258	112	0.0018
33	0.5904	73	0.0242	113	0.001
34	0.5884	74	0.0216	114	0.0008
35	0.5856	75	0.0206	115	0.0012
36	0.5824	76	0.0196	116	0.0014
37	0.5784	77	0.0186	117	0.0014
38	0.5734	78	0.0174	118	0.0006
39	0.569	79	0.0164	119	0.0002

Appendix F:
Observed effects during annealing after total dose irradiation



Star1000 Average Dark Current during annealing



STAR 1000 Dark Signal Non Uniformity during annealing

1. **Average dark current rise during annealing.**
   On the average, the dark current still increases during annealing. This observation is not in line with the conclusions of J. Bogaerts. However, during this test the samples were annealed under bias while in the first test the samples were annealed without bias.

	STAR 1000
Average dark current rise under annealing	221 e-/s per Krad
Maximum dark current rise under annealing	183 e-/s per Krad

2. **The average DSNU remains constant during annealing**
   It was observed that the average DSNU slightly rises during annealing at room temperature, immediately after irradiation but decreases at elevated temperature. The net effect is almost constant.

	STAR 1000
Average DSNU rise during annealing	2 e-/s per Krad
Maximum-DSNU rise during annealing	-2 e-/s per Krad See remark !

3. **The spread in DSNU between samples decreases during annealing at temperature.**