EVALUATION OF THE MANUFACTURE OF MIXED RF BOARDS

A. Fina[(1)], D. Nevo[(2)], P. Monfraix[(1)], N. Venet[(2)]

[(1)]Thales Alenia Space Italia S.p.a., Zona Industriale Campo di Pile – 67100 L'Aquila (AQ) - Italy,
Antonio.Fina@thalesaleniaspace.com, Philippe.Monfraix@thalesaleniaspace.com
[(2)]Thales Alenia Space France SaS, 26 avenue J.F. Champollion – BP 33787 – 31037 Toulouse Cedex 1 - France,
David.Nevo@thalesaleniaspace.com, Norbert.Venet@thalesaleniaspace.com

ABSTRACT

Most equipment designs for European space applications using Printed Circuit Board (PCB) technology are today based on separate boards for the radiofrequency (RF)/high speed digital and low frequency signals, the main reason being the lack of ESA space level qualification of mixed dielectric PCB technology. The disadvantages of such an approach come mainly from the higher complexity (and cost) deriving from the need to route signals from/to RF and low frequency (LF) sections of the equipment, not to mention the increase in bulk due to assembly and interconnection of different PCBs. Technological advancement in ESA projects, together with the need for miniaturisation, drive the running effort to prepare mixed PCB technology to meet the high reliability requirements for space applications. In the frame of an ESA ECI-3 contract granted to Thales Alenia Space (TAS), an activity aimed at evaluating mixed RF boards technologies is being carried out and will be the subject of this paper.
Keywords: *mixed dielectric, printed circuit boards, RF/Microwave, ENEPIG, IST*

1. ACRONYMS

CoC:	Certificate of Conformance
IST:	Interconnection Stress Testing
ENEPIG:	Electroless Nickel Electroless Palladium Immersion Gold
ENIG:	Electroless Nickel Immersion Gold
LF:	Low frequency
PCB:	Printed Circuit Board
PTH:	Plated Through Hole
RH:	Relative Humidity
RF:	Radiofrequency
TAS:	Thales Alenia Space
TAS-F:	Thales Alenia Space - France
TAS-I:	Thales Alenia Space - Italy

2. INTRODUCTION

The ESA contract activity that is the subject of this paper is organized in the following two phases:

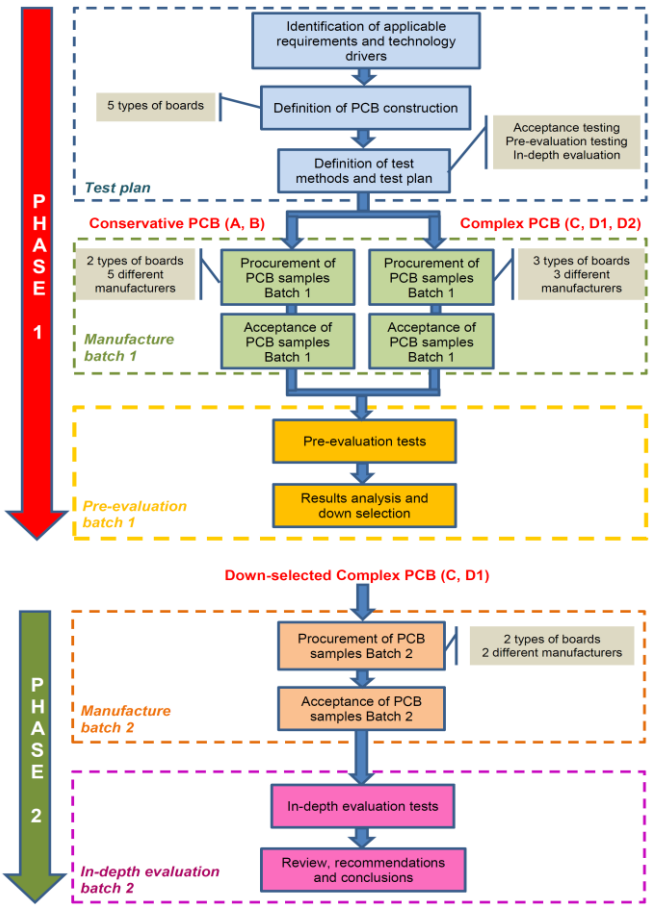

Figure 1. Study Logic

- Phase 1 encompasses the test plan definition, the manufacture of PCB samples Batch 1 and their pre-evaluation,
- Phase 2 is dedicated to the manufacture of PCB samples Batch 2 and their in-depth evaluation.

Phase 1 activities were jointly carried out by both Thales Alenia Space France (TAS-F) and Thales Alenia Space Italy (TAS-I) according to the study logic diagram shown in Figure 1.
Phase 2 shall start following ESA go-ahead upon successful Evaluation Review milestone achievement.

3. GOALS

The study has the following objectives:

- To establish test methods that allow acceptance testing and reliability assessment of mixed PCBs, including their RF performance;
- To evaluate mixed PCBs of various designs and PCB manufacturers;
- To establish best practices for mixed PCB design, manufacture and reliability testing.

ESA qualification of a specific technology/manufacturer is out of the scope of this activity.

4. ACCEPTANCE AND RELIABILITY TESTING METHODS OF MIXED RF PCBs

Batch acceptance test methods based on ECSS-Q-ST-70-11C were agreed with the involved PCB suppliers. Testing to be performed by the PCB manufacturers was established by the procurement specification. The chart in
Figure 2 shows the batch acceptance testing flow.
Pre-evaluation testing and in-depth evaluation testing plans were also defined. Environmental test methods based on ECSS-Q-ST-70-10C were adopted as standards. The pre-evaluation testing flow is shown in Figure 3.
In-depth evaluation testing flow is shown in Figure 4. Additional environmental tests w.r.t. those established to be performed at pre-evaluation testing were included. See also par. 9.

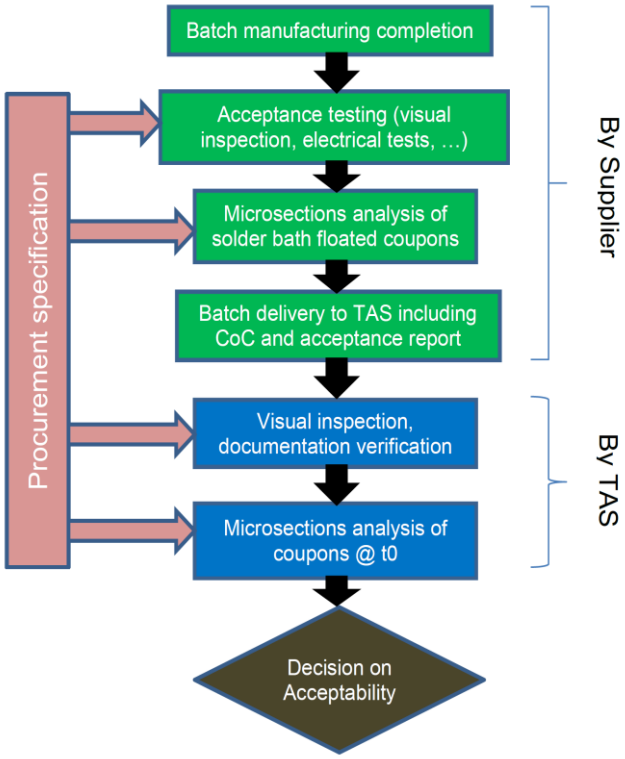

Figure 2. Batch acceptance testing

5. TEST VEHICLES DESIGN

The objective of this task was to describe precisely the different types of PCBs (two conservative versions plus three complex ones) to be manufactured and tested in the frame of this contract. Designs' built-ups and different integrated coupons were defined.
For each design version, a layout of the PCB was engineered including a detailed description of the technology building blocks required to evaluate the reliability of the final structure.
To define these built-ups, discussions with each of the involved manufacturers were held in order to converge towards structures and materials combinations that were achievable for everyone, allowing for some "personalization" coming from the fact that PCB shops do not all have the same manufacturing capabilities, heritage and/or preferences in terms of materials and processes.

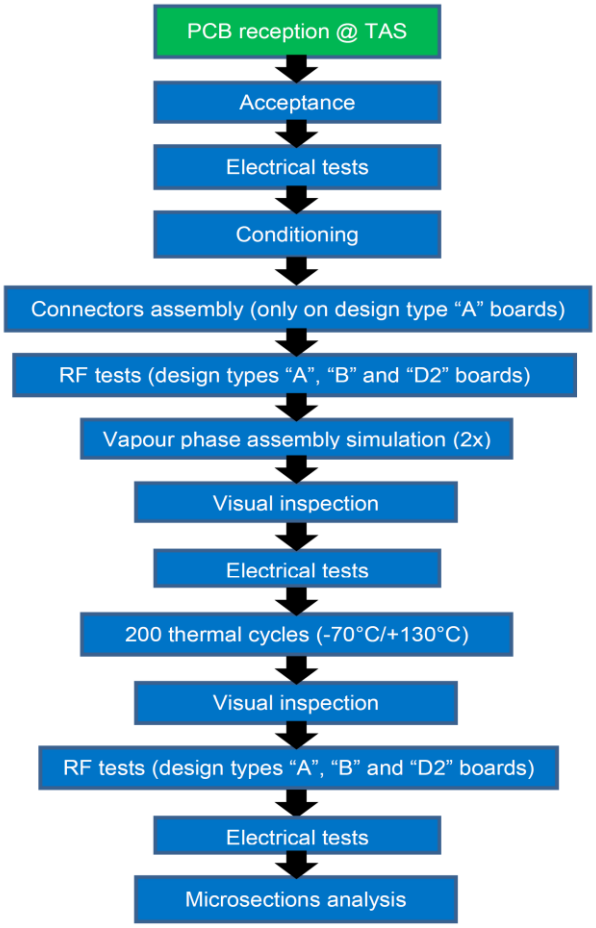

Figure 3. Pre-evaluation test plan

Two different design classes, based on complexity and on past experience of PCB shops, were established: a lower-risk *conservative* class, and a *complex*, more advanced and more challenging class of design.

Five different mixed PCB designs were defined:

- Type "A" of conservative class: based on a balanced combination of woven ceramic thermoset and polyimide laminates, designed by TAS-F.
- Type "B" of conservative class, based on a unbalanced combination of ceramic thermoplastic and polyimide laminates, with only one layer of thermoplastic material to implement the RF section of the PCB, designed by TAS-I.
- Type "C" of complex class: based on a balanced combination of woven ceramic thermoplastic and polyimide laminates, designed by TAS-F.
- Type "D1" of complex class: based on an unbalanced combination of woven ceramic thermoset and woven ceramic thermoplastic laminates, designed by TAS-I.
- Type "D2" of complex class: based on a balanced combination of woven ceramic thermoset and woven ceramic thermoplastic laminates, designed by TAS-I.

6. BATCH 1 PROCUREMENT AND ACCEPTANCE TESTING

Procurement and acceptance testing activities were carried out according to
Figure 2 on eight procured batches, as follows:

- conservative circuit of preferred type "A" was procured by TAS-F from 3 different manufacturers;
- conservative circuit of type "B" was procured by TAS-I from 2 different manufacturers;
- complex circuit of type "C" was procured by TAS-F from a single manufacturer;
- complex circuit of type "D1" was procured by TAS-I from a single manufacturer;
- complex circuit of type "D2" was procured by TAS-I from a single manufacturer.

Some issues were found by suppliers and during TAS acceptance testing of the procured batches. Apart from drilling parameters to be optimized for the specific combination of different laminate materials on two designs, and the adjustment of scaling sequence on one design, none of the detected problems were linked to the

Figure 4. In-depth evaluation testing plan

mixed nature of the PCBs: they were just board manufacturing typical defects.

7. PRE-EVALUATION TESTING RESULTS

Most of the anomalies found during pre-evaluation testing, and detected on microsections performed on environmentally tested coupons, were t_0 defects that "passed undetected" at acceptance testing done at TAS, in part due to those microsections been performed in an area of the board less prone to be affected by the observed defect (e.g. low PTH plating thickness), in part due to the probabilistic nature of defect screening through microsectional analysis (e.g. voids at blind via filling resin).
On one design, a crack close to the PTH/buried track interface was found affecting all PTH's. See Figure 5. Thermo-mechanical mismatch is being investigated as a possible cause.

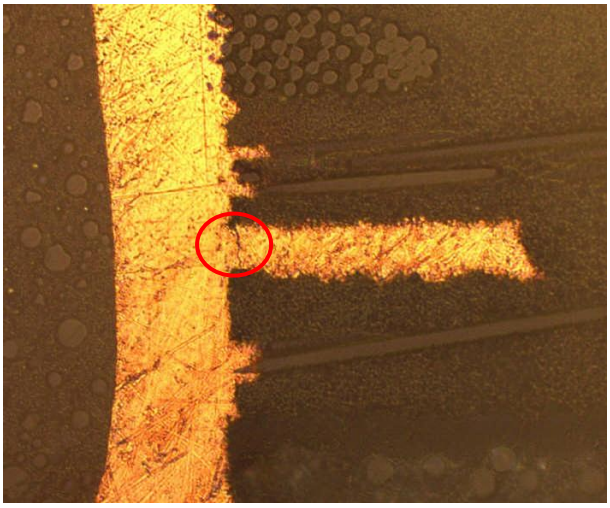

Figure 5. Crack close to PTH/buried track interface

Defects which cause cannot be excluded a priori to be linked to the mixed nature of the board are:

- Cracks in via filling resin
- Cracks along PTH walls

Cracks of filling resin were detected starting at the bottom of all the blind vias of a coupon of one of the evaluated designs, ending at the prepreg layer used to bond the two different material stack-ups of the mixed multilayer board. See Figure 6 and Figure 7, which show the crack propagating through a glass fiber of the preg and stopping at the weave intersection.
Cracks along PTH walls were observed on another design. See Figure 8. Thermomechanical behaviour of the stack-up is believed to be the cause for the observed anomaly. This design was not selected to proceed with phase 2 of the study, so it will not be possible to further investigate on the behaviour of the involved processes and materials in the frame of this contract.

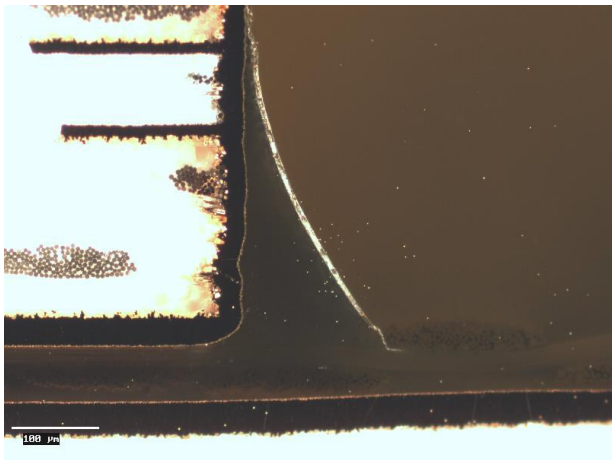

Figure 6. Cracks of filling resin

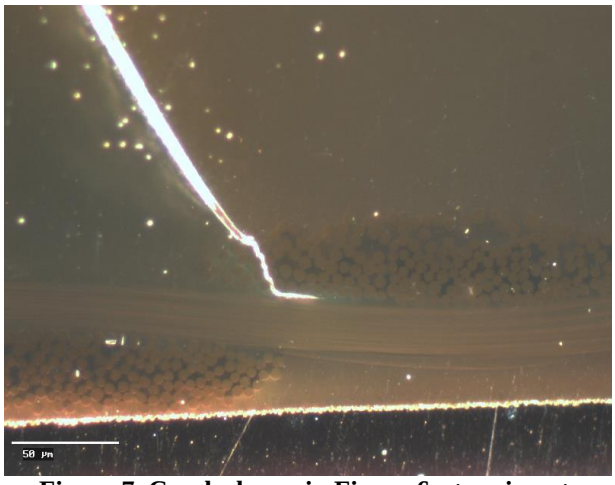

Figure 7. Crack shown in Figure 6, stopping at weave intersection between the 2 cross-linked fibers

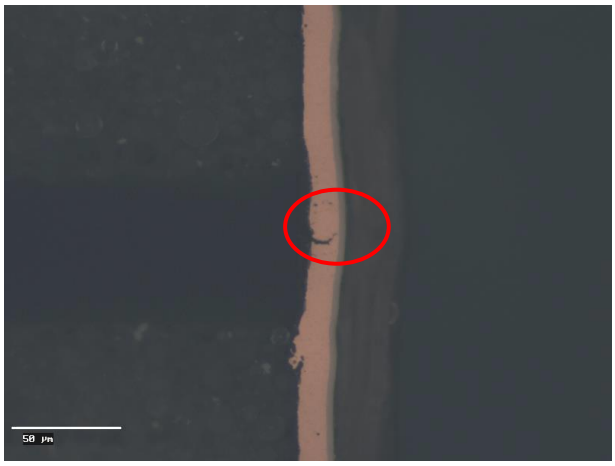

Figure 8. Crack along PTH wall

The results and analysis of pre-evaluation tests allowed proposing potential improvements to the designs and to the testing methods, before moving to the second

manufacturing batch procurement and in-depth evaluation testing steps of the study.

8. DOWN SELECTION OF PCB DESIGNS

Selection of the most promising candidate PCB types in terms of:

- Manufacturability,
- Reliability in environmental testing,
- Applicability to the space domain,

was performed.
Complex PCBs of types "C" and "D1" were selected to proceed with phase 2.
Design improvements were also implemented as follows:

- Materials were changed, based on additional experimental trials, to prevent the crack issues encountered during pre-evaluation testing.
- A filler epoxy paste was implemented in place of the prepreg for filling the via holes, following testing performed by the involved manufacturer showing this replacement to be an effective solution to prevent both cracking in filled holes and cap lifting issues.
- IST coupons were introduced on both down-selected designs; the recommended ESA guidelines were followed for the engineering of the coupons that were included in both complex design boards.

9. REVIEW OF TESTING METHODS

Based on the experience gained during phase 1 of the study, a review of initially defined test methods was performed.
Concerning acceptance testing, only minor modifications consisting in more complete testing of resistors on both down-selected designs, plus a higher number of microsections (to increase the probability of catching a higher number of t_0 defects) were done to the procurement specifications used during phase 1 procurement and acceptance activities.
In-depth evaluation testing will include, in addition to the tests performed at pre-evaluation, also the following:

- Damp heat: 10 days @ (40 ± 2) °C and 93% RH,
- High temperature storage: 1000h @ 125 °C,
- Thermal cycles: 1000 (instead of 200 cycles in the frame of pre-evaluation testing) from -70°C to +130°C,
- Interconnection Stress Testing (IST): on specific coupons defined according to ESA guidelines.

See the chart shown in Figure 1.

10. CONCLUSION

Results of acceptance and pre-evaluation testing carried out on the eight procured PCB batches belonging to five different designs (two conservative and three complex versions) were useful at highlighting weaknesses of implemented structures and capability level of the involved manufacturing lines.
Based on such results, it was possible to:

- Identify the most promising design candidates in terms of manufacturability, reliability in environmental testing, and applicability to the space domain,
- Define improvements to the selected PCB designs,
- Review acceptance testing methods,
- Define improvements to the in-depth evaluation testing flow defined at the beginning of the activity.

Phase 2 of the study will allow to make the necessary adjustments to the manufacturing processes to correct the identified weaknesses, and to find the limits of the selected mixed board technology designs and manufacturers as a result of in-depth environmental testing.
The improved acceptance methods should guarantee that only robust boards, manufactured according to the improved acceptance criteria, should be submitted to in-depth evaluation testing. This should increase the probability that such fittest boards will survive to the more severe environmental testing to be applied at phase 2.

11. NEXT STEP

Down selection of the most promising design candidates has been completed by both TAS-F and TAS-I.
Upon ESA approval following the Evaluation Review meeting (ER-1), next step is to proceed as shown in the logic diagram of the study for phase 2.