STACKING OF KNOWN GOOD REBUILT WAFERS FOR HIGH SPEED MEMORY AND SYSTEMS IN PACKAGE

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ABSTRACT

Based on Wire free Die on Die disruptive technology (WDoD™), high density memory and complex SiPs can be manufactured in a small factor package size. Stacking known good rebuilt wafers allows high yields while integrating high performance devices. With this new technology, 3D PLUS is highlighting the way to highly integrated System in Package (SiP) and demonstrates its know-how in the three dimensional integration. This technology is a potential candidate for space electronic applications which requires lighter, smaller, faster, reliable solutions; as digital payload processing.

KeyWords / topics: HDI, Wirefree, Non hermetic packaging technologies, Reliability challenges, RoHS, 3D packaging, vertical interconnect, RDL, rebuilt wafer, electrical simulation

1. INTRODUCTION

More and more applications are requiring electronics shrinkage in order to integrate high performance devices in a limited volume. Consumer market is driving 3D technology as smartphones, tablets and many handheld devices need advanced features in light and thin products.
Those requirements are being fulfilled by fan-in or package on package (PoP) technologies but real 3D low profile components are just being introduced for specific applications. Through silicon vias (TSV) is the main driving technology even if several drawbacks are still slowing-down its introduction such as:

- Highly specific design making multi-sourcing difficult to achieve
- Final 3D component yield drastically decreased as wafer level yield is good enough
- TSV yield
- TSV cost

Alternative technologies are being developed to get through those issues mainly for highly heterogeneous systems in package for which multi-sourcing is a must. 3D PLUS proposes a unique solution that overcomes many TSV issues:

- High yield as known good rebuilt wafers are stacked
- Multi-sourcing is very much compatible with this technology

Wafer level package manufacturers include double face redistribution layer (RDL) in their roadmaps as a first step for 3D integration with PoP solutions. 3D PLUS is a step ahead with stacking several rebuilt wafers with its patented bus metal interconnect.

2. WDoD™ TECHNOLOGY

Wire-free Die on Die technology (WDoD™) is based on stacking known good rebuilt wafers to meet high yield which is a must for 3D process [1]. Polymer bonding is used to stack each level and sidewall metallization allows interconnect between each level. Metallization can be chosen according to the electrical requirements and varnishing can be used to avoid any degradation during manual handling. Moreover, integrating dies allows choosing the right set of materials like mold compound and soldering materials if low alpha emission materials or RoHS compliant products are required.

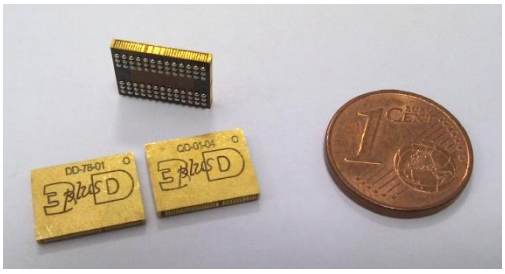


Figure 1: Dual Die and Quad die components

When needed, WDoD™ technology can be mixed with PCB levels if high density routing is required at the interconnect level. Such flexibility allows a very broad range of applications with die and PCB based levels. This alternative overcomes die sourcing as well when these are not available.

3. HIGH PERFORMANCE MEMORY STACK

3.1. Design with RDL BGA level

In order to demonstrate WDoD™ capabilities, DDR3 memory has been selected for its high working frequencies. Stacks of 2 or 4 dies have been used to benchmark our technology using fan-out (FO) embedded wafer level BGA (e-WLB) process. 300 mm rebuilt wafers are manufactured and thinned down to 200 µm before stacking and polymer bonding. Stacking alignment is within ± 15 µm allowing small lateral pitches demonstrating WDoD™ versatility with denser IO products such as FPGA.
Embedded DDR3 dies are 8 bits 1Gb known good dies and the stack increases the total memory space keeping an 8 bits memory bus. Final package sizes are 8.5x11x1.2 mm and 8.5x11x1.6 mm for the dual and quad die configurations respectively. And balling is JEDEC compatible.

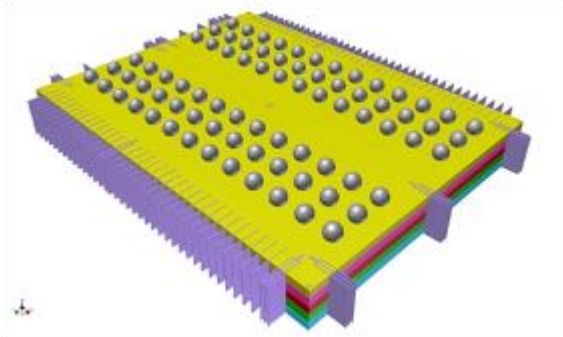


Figure 2: 3D view of a Quad Die component

One layer RDL is not compatible with BGA and bus metal routing thus an additional level is used for interconnect purpose. This additional level is not functional and embeds a dummy silicon die, see Fig. 3.
An additional capping layer is also used to protect the last rebuilt wafer level as FO e-WLB technology thins down both the molding compound and the die. With no capping layer, the back side of the component would be fragile as the last DDR3 die backside would be exposed. A heat sink could also be used to protect and dissipate. The total stack is shown in Fig. 3.

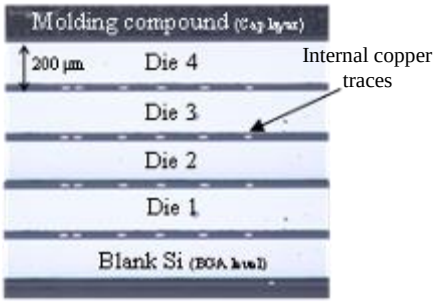


Figure 3: Cross-section of a Quad Die component

Special care was taken to match impedances for critical signals as DDR3 is operating at high frequencies, see Fig. 4. Electromagnetic field simulation was performed to characterize package before launching the manufacturing.

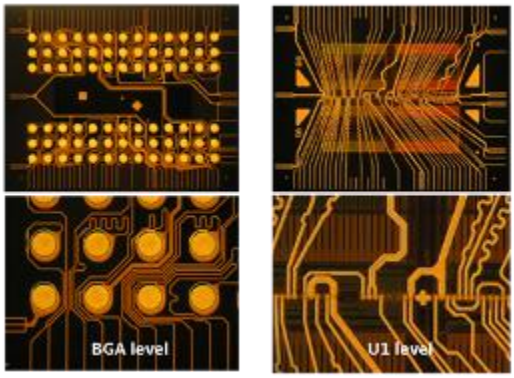


Figure 4: RDL levels BGA and DDR3

Critical traces are 20 µm width with a 40 µm pitch. Average pitch between traces at the bus metal interconnects is 250 µm, see Fig. 4.

- **Electrical simulation**

Package parasitic extraction was done using a 3D and 2D electromagnetic field simulation tool to characterize 3D stack package. Results of dual die and quad die configurations were compared while dual die results were compared to conventional wirebond technology. Dual and quad die results are similar excepted for parasitic capacitance which is higher for the four levels stack.

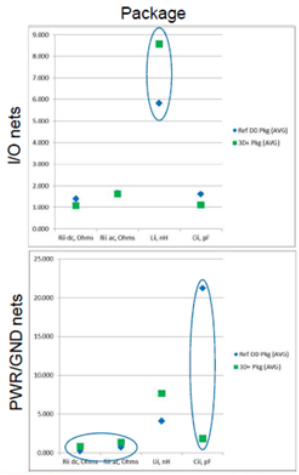


Figure 5: Comparison between wirebond and WDoD technologies for dual die configuration

Compared to wirebond technology, capacitances are lower and inductances are slightly higher, see Fig. 5. However looking at the challenge of routing the BGA level with one layer RDL only, the results are good.
Nevertheless, using a multilayer PCB or two layers RDL based BGA would significantly improve these parasitics.

- **Electrical performance**

Electrical test was performed at 2 frequencies and 3 temperatures: 533 MHz and 667 MHz and -10°C, 25°C and 95°C. A standard DDR3 test flow was used, comprising:

- Contact
- Leakage
- IDD at different operating conditions, according to specifications
- Test of the memory cell array: basic functionality (mrs5), t_{RCD} and retention (96 ms)
- ODT test
- At-speed test with tight CL, t_{RP}, t_{RCD} and duty-cycle
- Interface timings: command and data Setup & Hold, t_{QH}, t_{DQSQ}, t_{DQSCK}, t_{LZ}.

Dual die units are fully functional at 533 MHz and 667 MHz. 800 MHz has not been tested yet as the main objective was to reach 667 MHz with this first demonstrator. Quad die units do not achieve 667 MHz due to the parasitic capacitance increase that was forecasted during the electrical simulation. However, they do reach 533 MHz. This is expected to be improved with a PCB based level.

3.2. Design with PCB BGA level

In order to improve the electrical performances and also the mechanical robustness of the QD modules, a new design has been done by replacing the RDL based BGA level with a PCB. Both versions are shown in Fig. 6.

Figure 6: QD structures with RDL based version and PCB based

Cross-section in Fig. 7 shows the PCB BGA level (to be compared with Fig. 3).

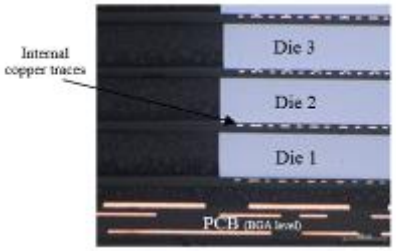
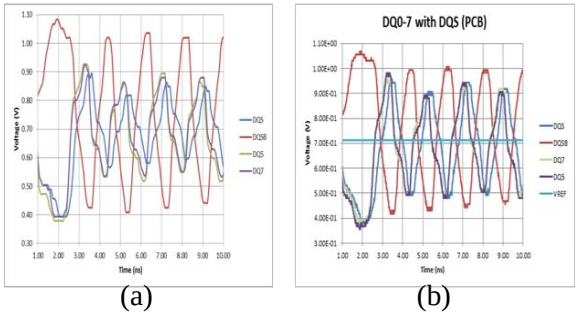


Figure 7: Cross-section of a QD die with PCB BGA level

Electrical results were very much improved with larger signal excursion and better slew rate which allowed all QD units to pass 667MHz tests, see Fig. 8.



(a) (b)

Figure 8: DQ vs DQS coupling for QD with RDL BGA level (a) and QD with PCB BGA level (b)

3.3 Reliability results

Reliability is key with such a 3D stack. Preliminary results after pre-conditioning (moisture level sensitive 5) and thermal cycling did show issues at the overmold layer between the PCB substrate and the first RDL level in Fig. 9.

Figure 9: Internal failure after preconditioning and TC

The use of the right set of materials allowed solving this issue and pass the reliability plan described in Fig. 10.

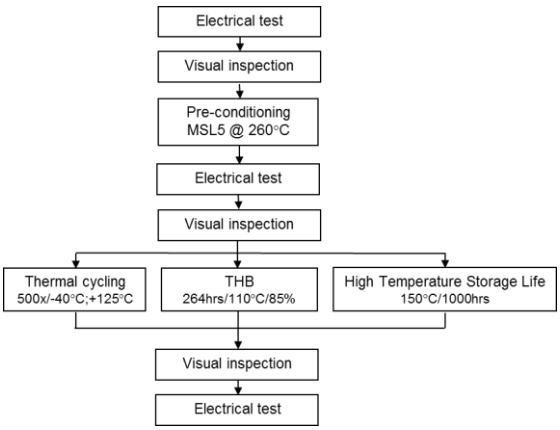


Figure 10: First level reliability plan

Board level reliability passed as well with 500 thermal cycles at -40°C/+125°C.

4. SiP FOR MEDICAL APPLICATIONS

3D PLUS has designed and manufactured for a major Cardiac Rhythm Management solutions manufacturer, a leadless pacemaker implanted inside the heart, see Fig. 11. This has been achieved thanks to a 16 times shrinkage of the volume when compared to conventional pacemakers.

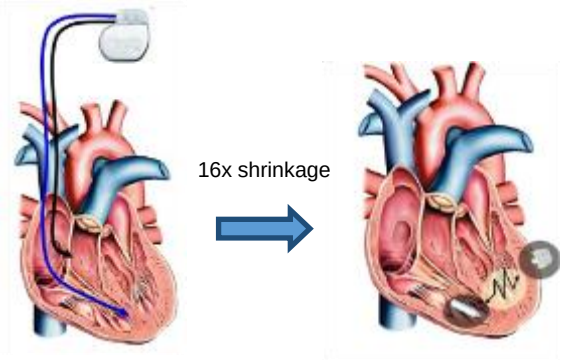
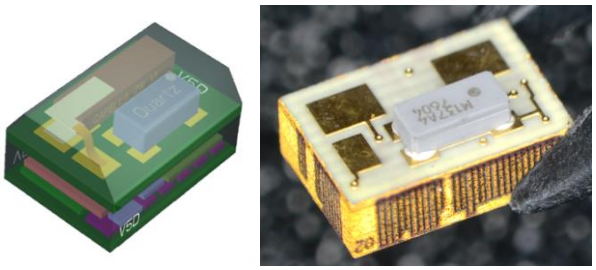


Figure 11: Conventional and leadless pacemakers

This challenge has been fulfilled thanks to the versatility of 3D PLUS stacking technology, allowing the stack of WDoD™ rebuilt wafers together with PCB levels on which SMD components can be soldered.



a) b)

Figure 12: 3D concept a) and real picture of the leadless pacemaker b)

External sides of this module may be also populated by additional components allowing interconnects with other sub-assemblies.
Dimensions of the module are: 2.3 x 5.2 x 7.3 mm^3 and volume is less than 1 cm^3, see Fig. 12. Bus metal laser pitch is 250 µm. Embedded dies are ASICs and silicon based capacitors. SMD components are mainly capacitors.
This example highlights capabilities of 3D PLUS technology for challenging dimensions. Moreover, more conventional pacemakers and defibrillators may take benefits of this technology compared with hybrid technology and/or folded technology.

5. SiP FOR INDUSTRIAL AND/OR DEFENSE APPLICATIONS

3D PLUS has designed and manufactured, in collaboration with an industrial end-user, a calculation node.

The module integrates 2 PCBs with more than 100 decoupling capacitors, one FPGA, two DDR dies and one FLASH, see Fig. 14. It has the same footprint and ball-out than the FPGA plastic package and 4 GTP transceivers working at 2.5GBps.

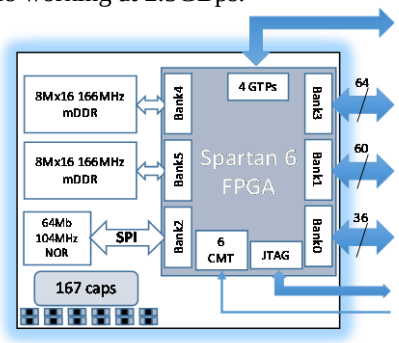


Figure 13: system block diagram

The gain is twofold:

- The two dimensional area gain on a board is about 30 %
- Designers are relieved from the tedious task of compact layout, testing and validation of a generic bloc and can therefore focus their work to optimize the interface with analog or digital peripheral with a much simplified layout area

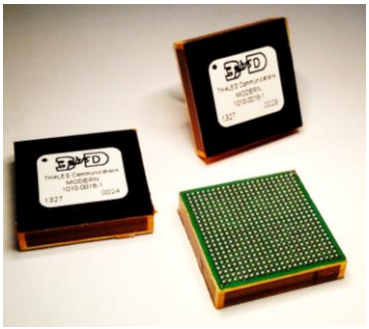


Figure 14: FUSIO-II modules

The embedded technology of this product is very advanced as this stack is made of:

- 8 layers HDI PCBs with fan-out of 100µm pitch and traces of 40 µm wide are stacked, see Fig. 15
- WDoD™ levels with 2 levels RDL requiring pitches of 51 µm at the FPGA aluminium pad level, see Fig. 16
- Lateral 3D interconnect with a pitch of 100 µm

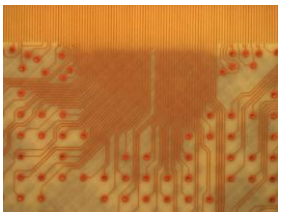


Figure 15: Top view of multilayer PCB with 40 µm wide traces and microvias

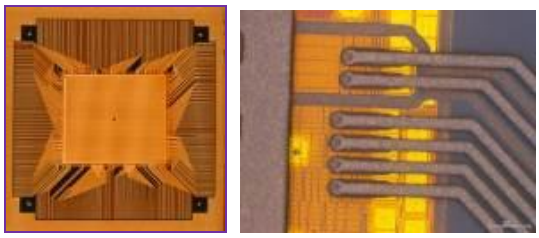


Figure 16: General and local view of double RDL on FPGA die with a pad pitch of 51 µm

6. CONCLUSIONS

Consumer memory market is not 3D PLUS commercial target however, extended temperature range or wide bus memories for industrial and military applications are clearly rising up a lot of interest. Known good die sourcing is key as one failing or poorly performing die jeopardize the final component.

These products shows that high performance SiP can be built with WDoD™ technology. Integrating a FPGA with DDR3 memory in a small form factor component is promising and is a true alternative to silicon interposers.
In the near future, space application requiring high numbers of I/Os in a small form factor product could be fulfilled with this new technology. Apart from a 0.8 mm pitch, the FUSIO-II product is highlighting the type of complex units that can be achieved while keeping standard footprints.

Acknowledgements
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